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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la84adfa-v0

1.2 Product Lists

Tables 1.9 to 1.12 list product information for each group. Figures 1.1 to 1.4 show the Correspondence of Part No., with Memory Size and Package for each group.

Table 1.9 Product List for R8C/LA3A Group **Current of Oct 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA32ANFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	N Version
R5F2LA34ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	
R5F2LA32ADFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	D Version
R5F2LA34ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	

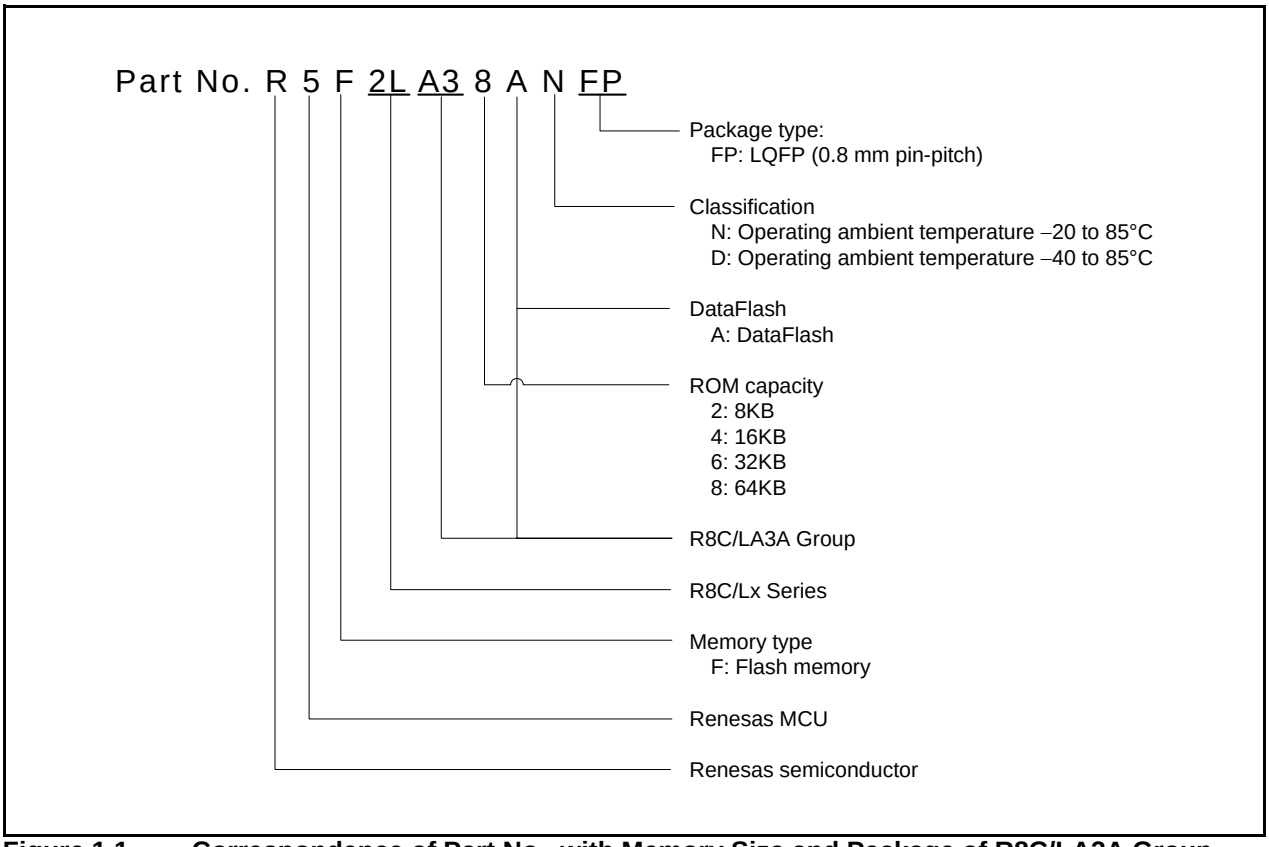
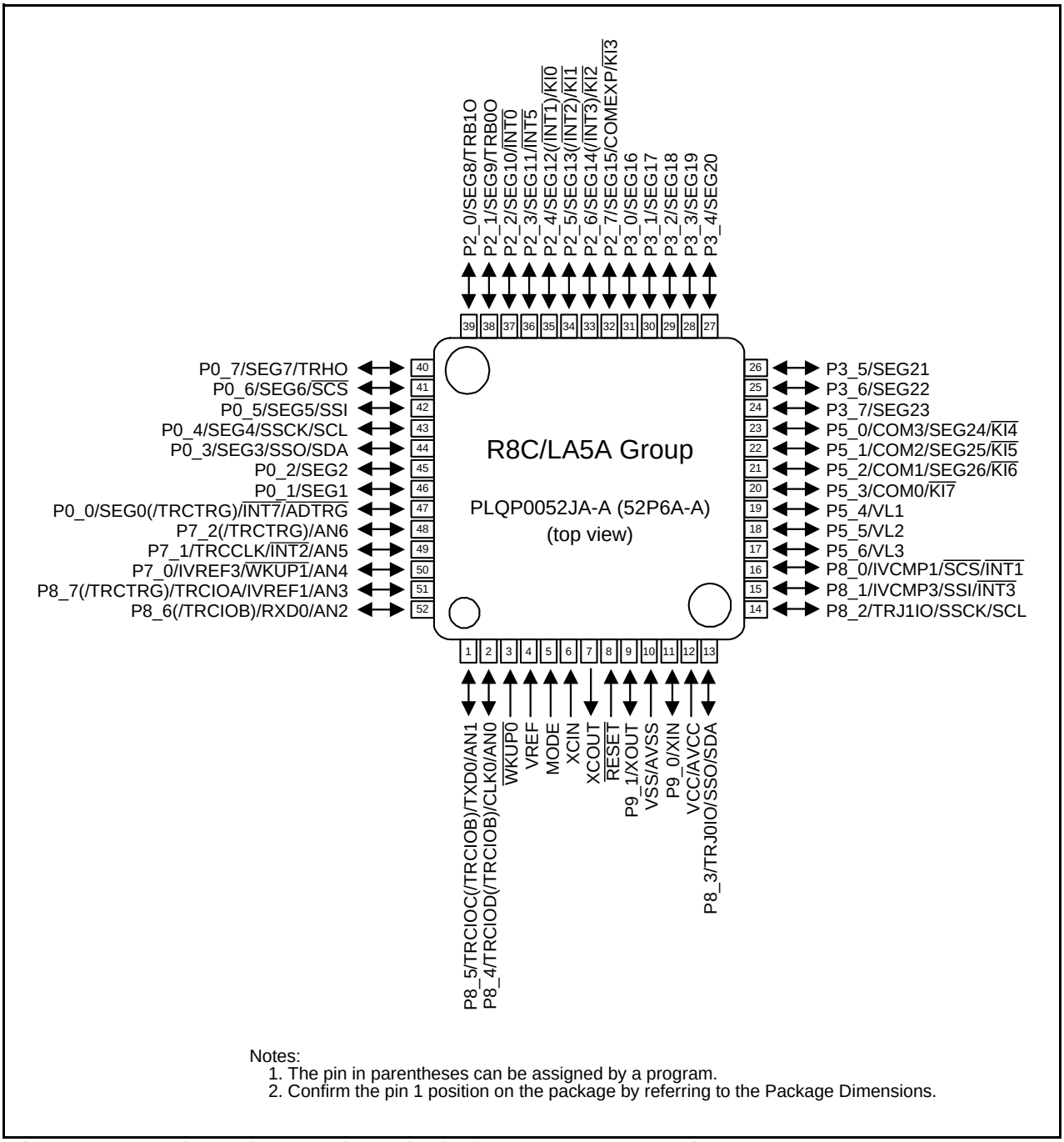


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/LA3A Group



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the Package Dimensions.

Figure 1.10 Pin Assignment (Top View) of PLQP0052JA-A Package

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

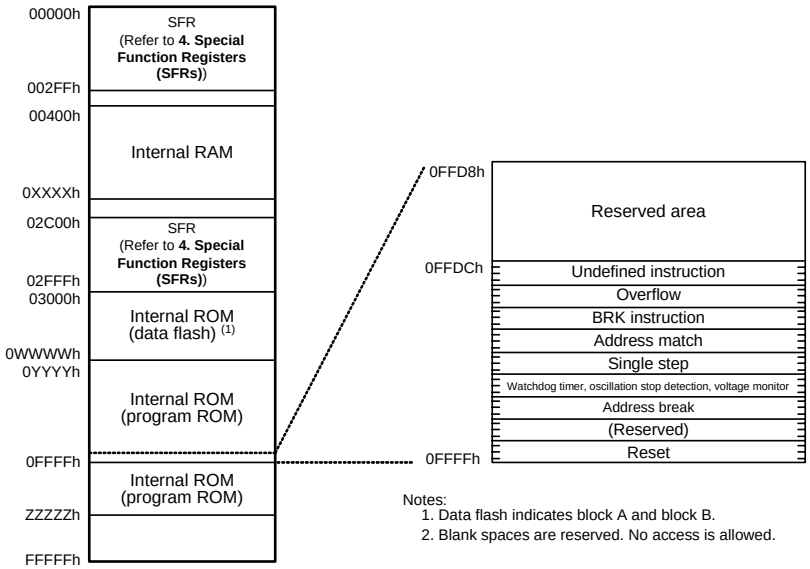
Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3. Memory

Figure 3.1 shows a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated higher addresses, beginning with address 03000h.
For example, two 1-Kbyte internal ROM (data flash) areas are allocated addresses 03000h to 037FFh. Two 2-Kbyte internal RAM (data flash) areas are allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 3.5-Kbyte internal RAM area is allocated addresses 00400h to 011FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A and block B.
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM		Data Flash	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh	Capacity	Address 0WWWWh
R5F2LA32ANFP, R5F2LA32ADFP, R5F2LA52ANFP, R5F2LA52ADFP	8 Kbytes	0E000h	0FFFFh	2 Kbytes	00BFFh	1 Kbyte × 2	037FFh
R5F2LA34ANFP, R5F2LA34ADFP, R5F2LA54ANFP, R5F2LA54ADFP, R5F2LA64ANFP, R5F2LA64ANFA, R5F2LA64ADFP, R5F2LA64ADFA, R5F2LA84ANFP, R5F2LA84ANFA, R5F2LA84ADFP, R5F2LA84ADFA	16 Kbytes	0C000h	0FFFFh	2 Kbytes	00BFFh		
R5F2LA36ANFP, R5F2LA36ADFP, R5F2LA56ANFP, R5F2LA56ADFP, R5F2LA66ANFP, R5F2LA66ANFA, R5F2LA66ADFP, R5F2LA66ADFA, R5F2LA86ANFP, R5F2LA86ANFA, R5F2LA86ADFP, R5F2LA86ADFA	32 Kbytes	08000h	0FFFFh	2 Kbytes	00BFFh		
R5F2LA67ANFP, R5F2LA67ANFA, R5F2LA67ADFP, R5F2LA67ADFA, R5F2LA87ANFP, R5F2LA87ANFA, R5F2LA87ADFP, R5F2LA87ADFA	48 Kbytes	04000h	0FFFFh	3.5 Kbytes	011FFh		
R5F2LA38ANFP, R5F2LA38ADFP, R5F2LA58ANFP, R5F2LA58ADFP, R5F2LA68ANFP, R5F2LA68ANFA, R5F2LA68ADFP, R5F2LA68ADFA, R5F2LA88ANFP, R5F2LA88ANFA, R5F2LA88ADFP, R5F2LA88ADFA	64 Kbytes	04000h	13FFFh	3.5 Kbytes	011FFh		
R5F2LA6AANFP, R5F2LA6AANFA, R5F2LA6CADFP, R5F2LA6CADFA, R5F2LA8AANFP, R5F2LA8AANFA, R5F2LA8CADFP, R5F2LA8CADFA	96 Kbytes	04000h	1BFFFh	5.5 Kbytes	019FFh	2 Kbytes × 2	03FFFh
R5F2LA6AANFP, R5F2LA6AANFA, R5F2LA6CADFP, R5F2LA6CADFA, R5F2LA8AANFP, R5F2LA8AANFA, R5F2LA8CADFP, R5F2LA8CADFA	128 Kbytes	04000h	23FFFh	5.5 Kbytes	019FFh		

Figure 3.1 Memory Map

Table 4.4 SFR Information for R8C/LA5A Group (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh	A/D Control Register 2	ADCON2	00h
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h			
00E2h	Port P0 Direction Register	PD0	00h
00E3h			
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h			
00E9h	Port P5 Register	P5	XXh
00EAh			
00EBh	Port P5 Direction Register	PD5	00h
00ECh			
00EDh	Port P7 Register	P7	XXh
00EEh			
00EFh	Port P7 Direction Register	PD7	00h
00F0h	Port P8 Register	P8	XXh
00F1h	Port P9 Register	P9	XXh
00F2h	Port P8 Direction Register	PD8	00h
00F3h	Port P9 Direction Register	PD9	00h
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.5 SFR Information for R8C/LA5A Group (5) (1)

Address	Register	Symbol	After Reset
0100h			
0101h			
0102h			
0103h			
0104h			
0105h			
0106h			
0107h			
0108h	Timer RB0 Control Register	TRB0CR	00h
0109h	Timer RB0 One-Shot Control Register	TRB0OCR	00h
010Ah	Timer RB0 I/O Control Register	TRB0IOC	00h
010Bh	Timer RB0 Mode Register	TRB0MR	00h
010Ch	Timer RB0 Prescaler Register	TRB0PRE	FFh
010Dh	Timer RB0 Secondary Register	TRB0SC	FFh
010Eh	Timer RB0 Primary Register	TRB0PR	FFh
010Fh			
0110h	Timer RH Second Data Register / Counter Data Register	TRHSEC	XXh 00h (2)
0111h	Timer RH Minute Data Register / Compare Data Register	TRHMIN	XXh 00h (2)
0112h	Timer RH Hour Data Register	TRHHR	00XXXXXXb 00h (2)
0113h	Timer RH Day-of-the-Week Data Register	TRHWK	00000XXXb 00h (2)
0114h	Timer RH Date Data Register	TRHDY	00XXXXXXb 00000001b (2)
0115h	Timer RH Month Data Register	TRHMON	000XXXXXb 00000001b (2)
0116h	Timer RH Year Data Register	TRHYR	XXh 00h (2)
0117h	Timer RH Control Register	TRHCR	XXX00X0Xb 000XX1X0b (2)
0118h	Timer RH Count Source Select Register	TRHCSR	X0001000b 0XXXXXXXb (2)
0119h	Timer RH Clock Error Correction Register	TRHADJ	XXh 00h (2)
011Ah	Timer RH Interrupt Flag Register	TRHIFR	00000XXXb 000XX000b (2)
011Bh	Timer RH Interrupt Enable Register	TRHIER	XXh 00h (2)
011Ch	Timer RH Alarm Minute Register	TRHAMN	XXh 00h (2)
011Dh	Timer RH Alarm Hour Register	TRHAHR	XXh 00h (2)
011Eh	Timer RH Alarm Day-of-the-Week Register	TRHAWK	X0000XXXb 00h (2)
011Fh	Timer RH Protect Register	TRHPRC	00h X0000000b (2)
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.6 SFR Information for R8C/LA5A Group (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.9 SFR Information for R8C/LA5A Group (9) (1)

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h			
0202h	LCD Option Clock Control Register	LCR2	00h
0203h	LCD Clock Control Register	LCR3	00h
0204h	LCD Display Control Register	LCR4	00h
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h			
020Ah			
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch			
020Dh			
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
:			
2FFFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.13 SFR Information for R8C/LA8A Group (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh	A/D Control Register 2	ADCON2	00h
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h	Port P8 Register	P8	XXh
00F1h	Port P9 Register	P9	XXh
00F2h	Port P8 Direction Register	PD8	00h
00F3h	Port P9 Direction Register	PD9	00h
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.17 SFR Information for R8C/LA8A Group (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h	Port P1 Pull-Up Control Register	P1PUR	00h
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h	Port P4 Pull-Up Control Register	P4PUR	00h
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h	Port P6 Pull-Up Control Register	P6PUR	00h
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h	Port P8 Pull-Up Control Register	P8PUR	00h
01E9h	Port P9 Pull-Up Control Register	P9PUR	00h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P7 Drive Capacity Control Register	P7DRR	00h
01F1h	Port P8 Drive Capacity Control Register	P8DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

5.1.3 Peripheral Function Characteristics

Table 5.3 A/D Converter Characteristics
(Vcc/AVcc = Vref = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVcc		–	–	10	Bit
–	Absolute accuracy (2)	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	–	–	±3	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	–	–	±5	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	–	–	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	–	–	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	–	–	±2	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	20	MHz
			3.2 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	16	MHz
			2.7 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	10	MHz
			1.8 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	8	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	ms
tSAMP	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
IVref	Vref current		Vcc = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
Vref	Reference voltage				1.8	–	AVcc	V
VIA	Analog input voltage (3)				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:
1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Temperature Sensor Characteristics
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
VTMP	Temperature sensor output voltage	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz Ambient temperature = 25 °C	550	600	650	mV
–	Temperature coefficient	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz Ambient temperature = 25 °C	–	–2.1	–	mV/°C
–	Start-up time	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz	–	–	200	µs
ITMP	Operating current	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz	–	100	–	µA

5.1.5 AC Characteristics

Table 5.24 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)

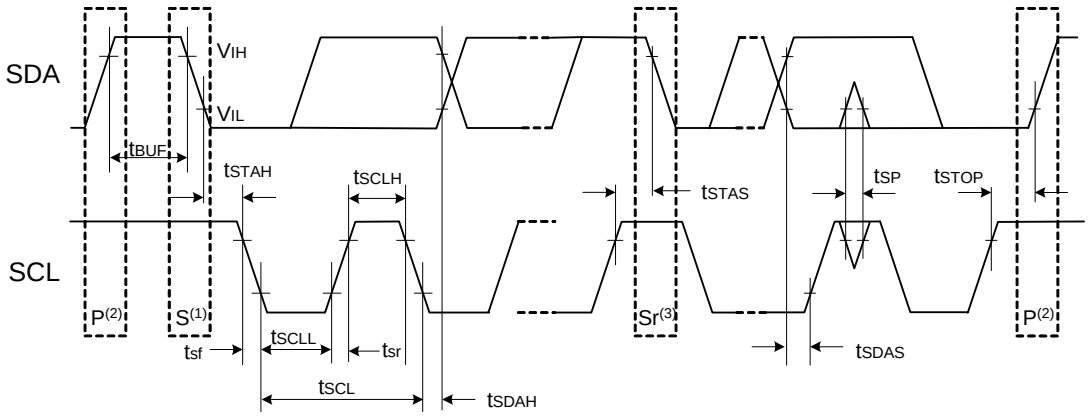
Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	-	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1t_{CYC} + 20	ns
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

Table 5.25 Timing Requirements of I²C bus Interface (1)
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tCYC + 600 (1)	–	–	ns
tSCLH	SCL input “H” width		3tCYC + 300 (1)	–	–	ns
tSCLL	SCL input “L” width		5tCYC + 500 (1)	–	–	ns
tsf	SCL, SDA input fall time		–	–	300	ns
tSP	SCL, SDA input spike pulse rejection time		–	–	1tCYC (1)	ns
tBUF	SDA input bus-free time		5tCYC (1)	–	–	ns
tSTAH	Start condition input hold time		3tCYC (1)	–	–	ns
tSTAS	Retransmit start condition input setup time		3tCYC (1)	–	–	ns
tSTOP	Stop condition input setup time		3tCYC (1)	–	–	ns
tSDAS	Data input setup time		1tCYC + 40 (1)	–	–	ns
tSDAH	Data input hold time		10	–	–	ns

Note:
1. 1tCYC = 1/f1(s)



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.7 I/O Timing of I²C bus Interface

Table 5.26 Timing Requirements of External Clock Input (XIN, XCIN)
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	50	–	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	24	–	24	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	24	–	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	20	–	20	–	20	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	10	–	10	–	10	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	10	–	10	–	10	–	µs

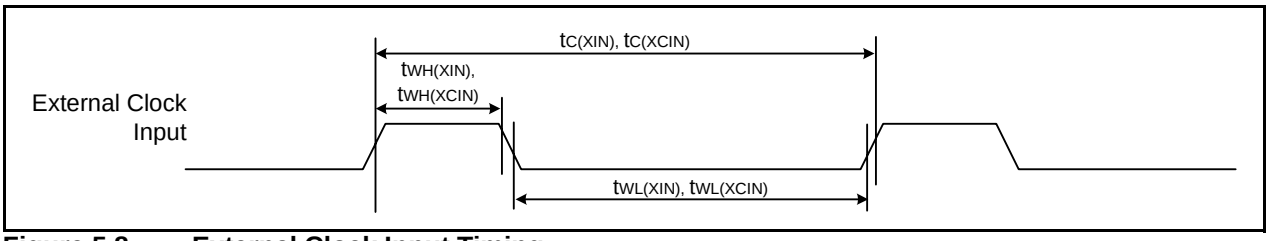


Figure 5.8 External Clock Input Timing

Table 5.27 Timing Requirements of TRJiIO (i = 0 or 1)
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJiIO input cycle time	500	–	300	–	100	–	ns
$t_{WH(TRJIO)}$	TRJiIO input “H” width	200	–	120	–	40	–	ns
$t_{WL(TRJIO)}$	TRJiIO input “L” width	200	–	120	–	40	–	ns

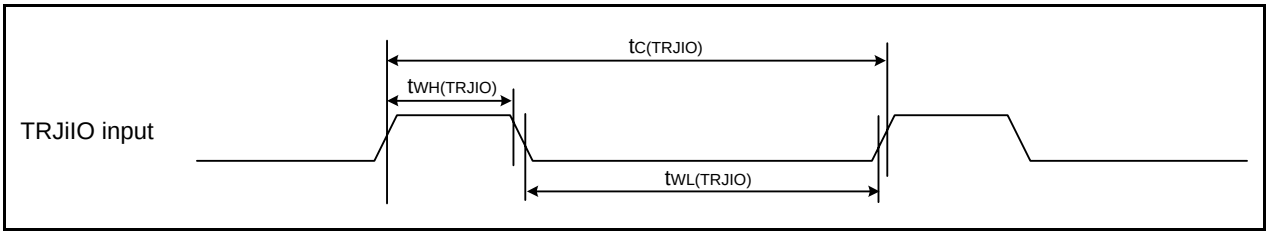


Figure 5.9 Input Timing of TRJiIO

5.2 Electrical Characteristics (R8C/LA6A Group and R8C/LA8A Group)

5.2.1 Absolute Maximum Ratings

Table 5.30 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		P5_4/VL1		–0.3 to VL2 (2)	V
		P5_5/VL2		VL1 to VL3	V
		P5_6/VL3		VL2 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		COM0 to COM3		–0.3 to VL3	V
		SEG0 to SEG39		–0.3 to VL3	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version)/ –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

Table 5.42 High-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	VCC = 1.8 V to 5.5 V – 20°C ≤ Topr ≤ 85°C	19.2	20	20.8	MHz
		VCC = 1.8 V to 5.5 V – 40°C ≤ Topr ≤ 85°C	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (1)	VCC = 1.8 V to 5.5 V – 20°C ≤ Topr ≤ 85°C	17.694	18.432	19.169	MHz
		VCC = 1.8 V to 5.5 V – 40°C ≤ Topr ≤ 85°C	17.510	18.432	19.353	MHz
–	Oscillation stability time		–	5	30	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	530	–	µA

Note:
1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.43 Low-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time		–	–	35	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	2	–	µA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
–	Oscillation stability time		–	–	35	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	2	–	µA

Table 5.44 Power Supply Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on (1)		–	–	2000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.48 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			16 MHz	Off	Off	125 kHz	No division	–		–	3.9	8	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	–	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	3.1	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.5	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	110	320	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	63	220	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	60	220	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	46	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.8	33	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	4.6	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	2.4	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.03	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.8	6.4	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2.7	–	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

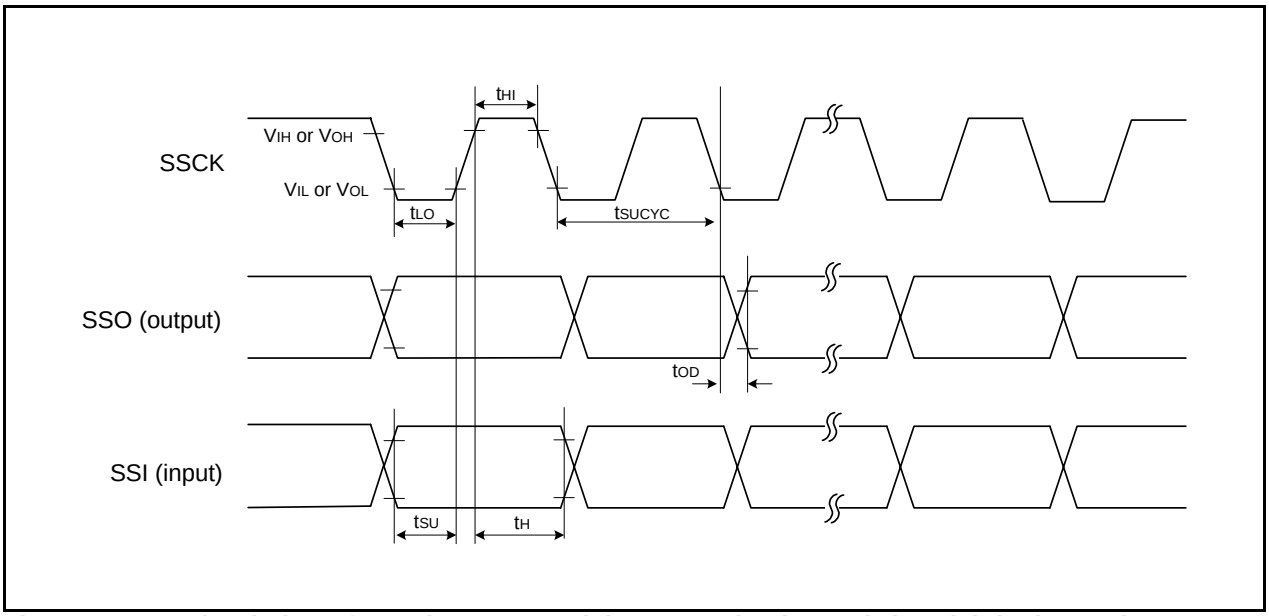
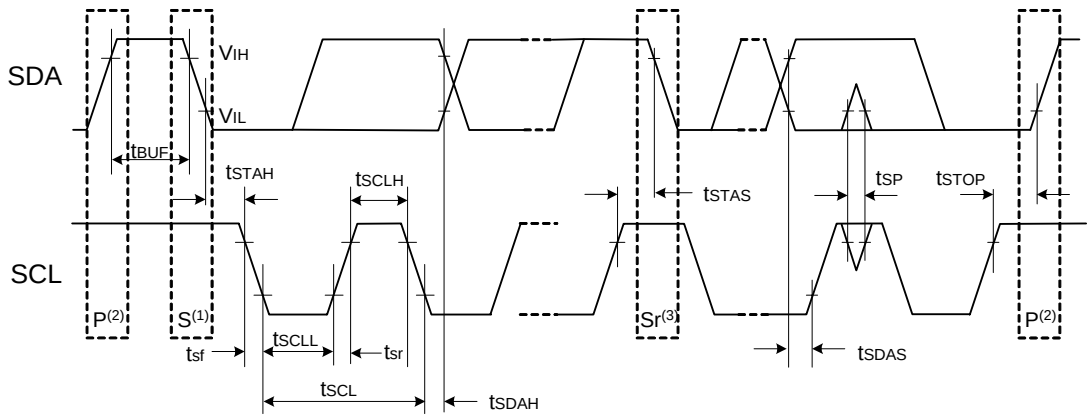


Figure 5.17 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.54 Timing Requirements of I²C bus Interface (1)
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tCYC + 600 (1)	–	–	ns
tSCLH	SCL input “H” width		3tCYC + 300 (1)	–	–	ns
tSCLL	SCL input “L” width		5tCYC + 500 (1)	–	–	ns
tsf	SCL, SDA input fall time		–	–	300	ns
tSP	SCL, SDA input spike pulse rejection time		–	–	1tCYC (1)	ns
tBUF	SDA input bus-free time		5tCYC (1)	–	–	ns
tSTAH	Start condition input hold time		3tCYC (1)	–	–	ns
tSTAS	Retransmit start condition input setup time		3tCYC (1)	–	–	ns
tSTOP	Stop condition input setup time		3tCYC (1)	–	–	ns
tSDAS	Data input setup time		1tCYC + 40 (1)	–	–	ns
tSDAH	Data input hold time		10	–	–	ns

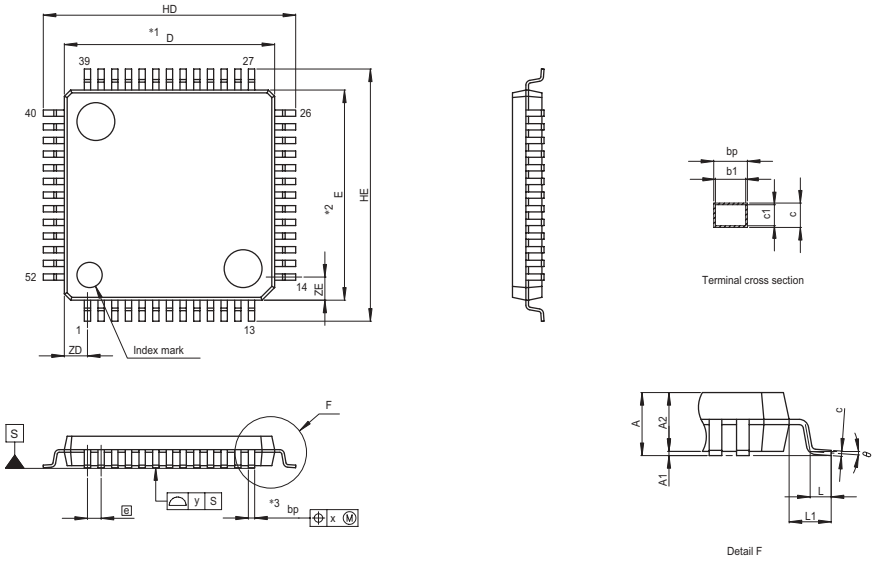
Note:
1. 1tCYC = 1/f1(s)



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.18 I/O Timing of I²C bus Interface

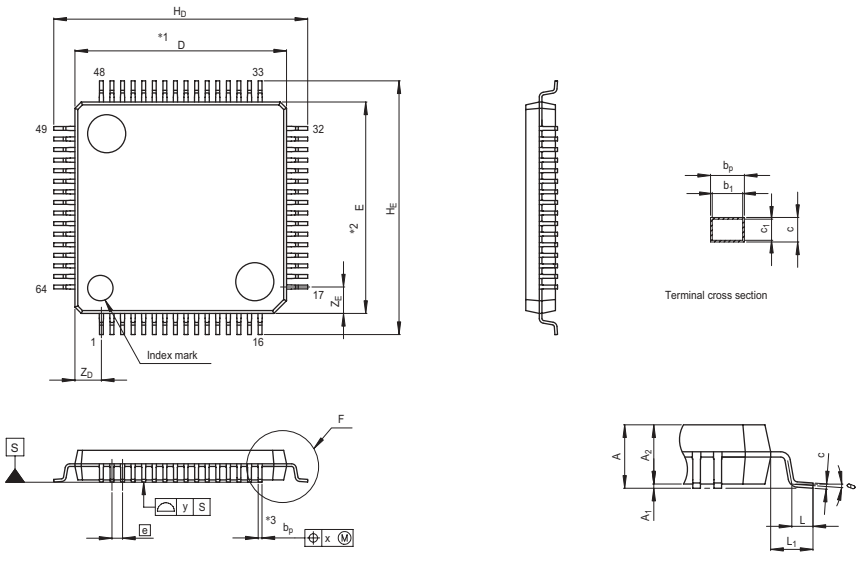
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—