Renesas Electronics America Inc - R5F2LA86ADFA#V0 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la86adfa-v0

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Tables 1.2 and 1.3 list the Programmable I/O Ports Provided for Each Group, and Tables 1.4 and 1.5 list the LCD Display Function Pins Provided for Each Group.
Figures 1.9 to 1.12 show the pin assignment for each group, and Tables 1.9 to 1.12 list product information.
The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/LA3A Group	R8C/LA5A Group	R8C/LA6A Group	R8C/LA8A Group
I/O Ports	Programmable I/O ports	26 pins	44 pins	56 pins	72 pins
	High current drive ports	8 pins	8 pins	8 pins	10 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	6 pins	8 pins	8 pins
Timer RJ	Timer RJ0 output pin	None	None	None	1 pin
	Timer RJ1 output pin	None	None	None	1 pin
	Timer RJ2 I/O pin	None	None	None	1 pin
	Timer RJ2 output pin	None	None	None	1 pin
Timer RH	Timer RH output pin	None	1 pin	1 pin	1 pin
Serial interface	UART2	None	None	1 pin	1 pin
A/D Converter	Analog input pins	5 pins	7 pins	8 pins	12 pins
LCD Drive Control Circuit	Segment output pins	Max. 11 pins	Max. 27 pins	Max. 32 pins	Max. 40 pins
Comparator B	Analog input voltage	1 pin	2 pins	2 pins	2 pins
	Reference input voltage	1 pin	2 pins	2 pins	2 pins
Clock	XCIN pin	Shared with XIN pin	Dedicated pin	Dedicated pin	Dedicated pin
	XCOUT pin	Shared with XOUT pin	Dedicated pin	Dedicated pin	Dedicated pin
Packages		32-pin LQFP	52-pin LQFP	64-pin LQFP	80-pin LQFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
   Refer to Tables 1.13 to 1.17, Pin Name Information by Pin Number, for details.

Table 1.11 Product List for R8C/LA6A Group **Current of Oct 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA64ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	N Version
R5F2LA64ANFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA66ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	
R5F2LA66ANFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA67ANFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA67ANFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA68ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA68ANFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA6AANFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6AANFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	
R5F2LA6CANFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6CANFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	
R5F2LA64ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	D Version
R5F2LA64ADFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA66ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064KB-A	
R5F2LA66ADFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0064GA-A	
R5F2LA67ADFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA67ADFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA68ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064KB-A	
R5F2LA68ADFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0064GA-A	
R5F2LA6AADFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6AADFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	
R5F2LA6CADFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064KB-A	
R5F2LA6CADFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0064GA-A	

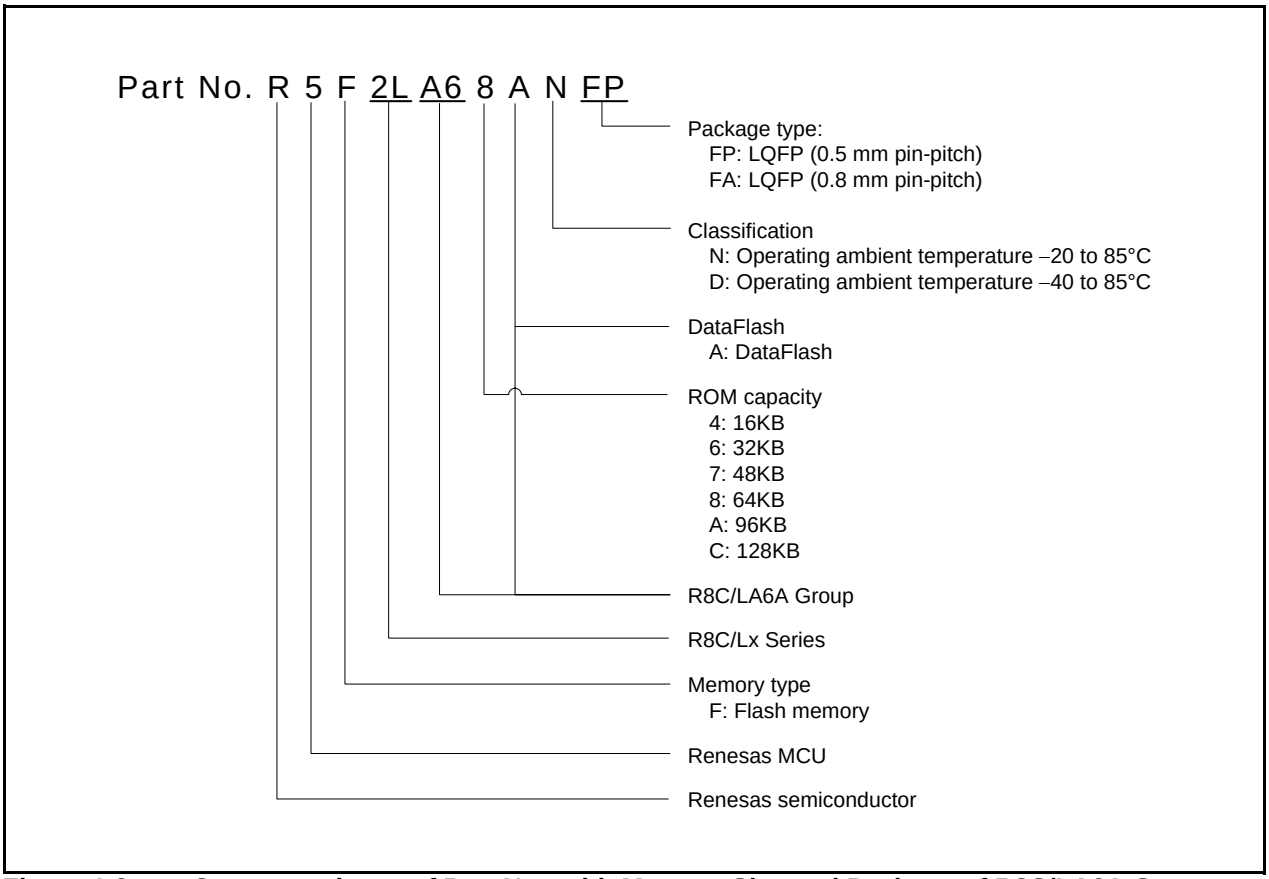
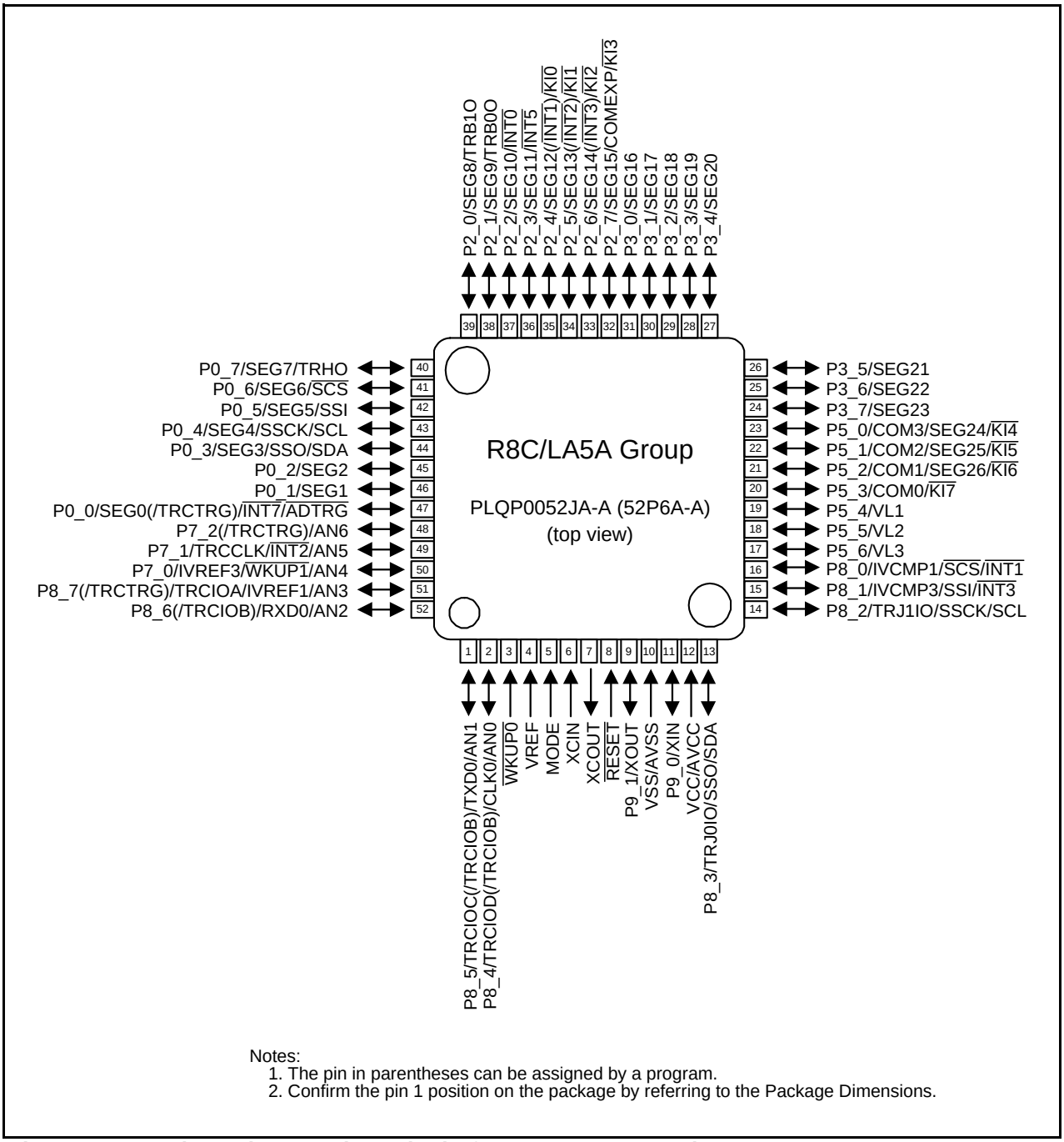


Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/LA6A Group



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the Package Dimensions.

Figure 1.10 Pin Assignment (Top View) of PLQP0052JA-A Package

Table 1.13 Pin Name Information by Pin Number (R8C/LA3A Group, R8C/LA5A Group)(1)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA5A	LA3A			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, Comparator B	LCD drive Control Circuit
1	30		P8_5		TRCIOC/ (TRCIOB)	TXD0			AN1	
2	31		P8_4		TRCIOD/ (TRCIOB)	CLK0			AN0	
3	32	$\overline{\text{WKUP0}}$								
4	1	VREF								
5	2	MODE								
6		XCIN								
7		XCOUT								
8	3	$\overline{\text{RESET}}$								
9	4	XOUT (XCOUT) (2)	P9_1							
10	5	VSS/AVSS								
11	6	XIN (XCIN) (2)	P9_0							
12	7	VCC/AVCC								
13	8		P8_3		TRJ0IO		SSO	SDA		
14	9		P8_2		TRJ1IO		SSCK	SCL		
15	10		P8_1	$\overline{\text{INT3}}$			SSI		IVCMP3 (3)	
16	11		P8_0	$\overline{\text{INT1}}$			$\overline{\text{SCS}}$		IVCMP1	
17	12		P5_6							VL3
18	13		P5_5							VL2
19	14		P5_4							VL1
20	15		P5_3	$\overline{\text{KI7}}$						COM0
21	16		P5_2	$\overline{\text{KI6}}$						SEG26/ COM1
22	17		P5_1	$\overline{\text{KI5}}$						SEG25/ COM2
23	18		P5_0	$\overline{\text{KI4}}$						SEG24/ COM3
24			P3_7							SEG23
25			P3_6							SEG22
26			P3_5							SEG21
27			P3_4							SEG20
28			P3_3							SEG19
29			P3_2							SEG18
30			P3_1							SEG17

Note:
1. The pin in parentheses can be assigned by a program.
2. Pins (XCOUT) and (XCIN) are not available in the R8C/LA5A Group.
3. The IVCMP3 pin is not available in the R8C/LA3A Group.

Table 1.20 Pin Functions for R8C/LA8A Group (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off 0 mode exit input	$\overline{\text{WKUP0}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.
	$\overline{\text{WKUP1}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RB	TRB0O, TRB1O	O	Timer RB output pins.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RH	TRHO	O	Timer RH output pin.
Timer RJ	TRJ0IO, TRJ1IO, TRJ2IO	I/O	Timer RJ I/O pins.
	TRJ0IO, TRJ1IO, TRJ2IO	O	Timer RJ output pins.
Serial interface	CLK0, CLK2	I/O	Transfer clock I/O pin.
	RXD0, RXD2	I	Serial data input pin.
	TXD0, TXD2	O	Serial data output pin.
	$\overline{\text{CTS2}}$	I	Transmission control input pin.
	$\overline{\text{RTS2}}$	O	Reception control output pin.
	SCL2	I/O	I^2C mode clock I/O pin.
	SDA2	I/O	I^2C mode data I/O pin.

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

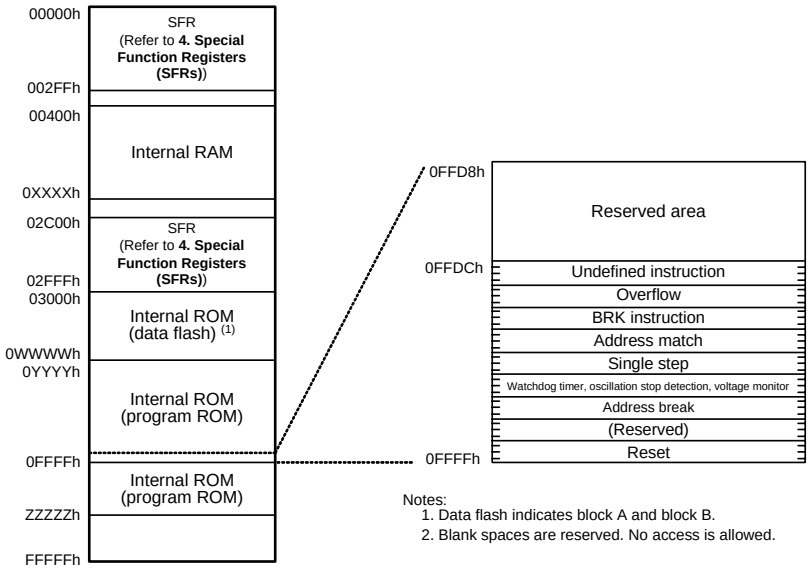
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

Figure 3.1 shows a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated higher addresses, beginning with address 03000h.
For example, two 1-Kbyte internal ROM (data flash) areas are allocated addresses 03000h to 037FFh. Two 2-Kbyte internal RAM (data flash) areas are allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 3.5-Kbyte internal RAM area is allocated addresses 00400h to 011FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A and block B.
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM		Data Flash	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh	Capacity	Address 0WWWWh
R5F2LA32ANFP, R5F2LA32ADFP, R5F2LA52ANFP, R5F2LA52ADFP	8 Kbytes	0E000h	0FFFFh	2 Kbytes	00BFFh	1 Kbyte × 2	037FFh
R5F2LA34ANFP, R5F2LA34ADFP, R5F2LA54ANFP, R5F2LA54ADFP, R5F2LA64ANFP, R5F2LA64ANFA, R5F2LA64ADFP, R5F2LA64ADFA, R5F2LA84ANFP, R5F2LA84ANFA, R5F2LA84ADFP, R5F2LA84ADFA	16 Kbytes	0C000h	0FFFFh	2 Kbytes	00BFFh		
R5F2LA36ANFP, R5F2LA36ADFP, R5F2LA56ANFP, R5F2LA56ADFP, R5F2LA66ANFP, R5F2LA66ANFA, R5F2LA66ADFP, R5F2LA66ADFA, R5F2LA86ANFP, R5F2LA86ANFA, R5F2LA86ADFP, R5F2LA86ADFA	32 Kbytes	08000h	0FFFFh	2 Kbytes	00BFFh		
R5F2LA67ANFP, R5F2LA67ANFA, R5F2LA67ADFP, R5F2LA67ADFA, R5F2LA87ANFP, R5F2LA87ANFA, R5F2LA87ADFP, R5F2LA87ADFA	48 Kbytes	04000h	0FFFFh	3.5 Kbytes	011FFh		
R5F2LA38ANFP, R5F2LA38ADFP, R5F2LA58ANFP, R5F2LA58ADFP, R5F2LA68ANFP, R5F2LA68ANFA, R5F2LA68ADFP, R5F2LA68ADFA, R5F2LA88ANFP, R5F2LA88ANFA, R5F2LA88ADFP, R5F2LA88ADFA	64 Kbytes	04000h	13FFFh	3.5 Kbytes	011FFh		
R5F2LA6AANFP, R5F2LA6AANFA, R5F2LA6CADFP, R5F2LA6CADFA, R5F2LA8AANFP, R5F2LA8AANFA, R5F2LA8CADFP, R5F2LA8CADFA	96 Kbytes	04000h	1BFFFh	5.5 Kbytes	019FFh	2 Kbytes × 2	03FFFh
R5F2LA6AANFP, R5F2LA6AANFA, R5F2LA6CADFP, R5F2LA6CADFA, R5F2LA8AANFP, R5F2LA8AANFA, R5F2LA8CADFP, R5F2LA8CADFA	128 Kbytes	04000h	23FFFh	5.5 Kbytes	019FFh		

Figure 3.1 Memory Map

Table 4.3 SFR Information for R8C/LA5A Group (3) (1)

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.10 SFR Information for R8C/LA8A Group (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h 00000100b (2)
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register 0	MSTCR0	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh (3)
000Ch	Oscillation Stop Detection Register	OCD	00000100b (4) 00h (4)
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h	Module Standby Control Register 1	MSTCR1	00h
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (5)
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	XXXXXX00b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Frequency Control Register 0	FRC0	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator 18 MHz Set Value Register 0	FR18S0	XXh
002Ah	High-Speed On-Chip Oscillator 18 MHz Set Value Register 1	FR18S1	XXh
002Bh			
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Frequency Control Register 1	FRC1	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (6) 00100000b (7)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (6) 1100X011b (7)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:
1. Blank spaces are reserved. No access is allowed.
2. The CSPRO bit in the CSPR register is set to 1.
3. The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
4. The reset value differs depending on the mode.
5. The CSPROINI bit in the OFS register is set to 0.
6. The LVDAS bit in the OFS register is set to 1.
7. The LVDAS bit in the OFS register is set to 0.

Table 4.12 SFR Information for R8C/LA8A Group (3) (1)

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h	Timer RJ2 Control Register	TRJ2CR	00h
0091h	Timer RJ2 I/O Control Register	TRJ2IOC	00h
0092h	Timer RJ2 Mode Register	TRJ2MR	00h
0093h	Timer RJ2 Event Pin Select Register	TRJ2ISR	00h
0094h	Timer RJ2 Register	TRJ2	FFh
0095h			FFh
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 5.7 Flash Memory (Program ROM) Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time		–	80	–	µs
–	Block erase time		–	0.12	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (6)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

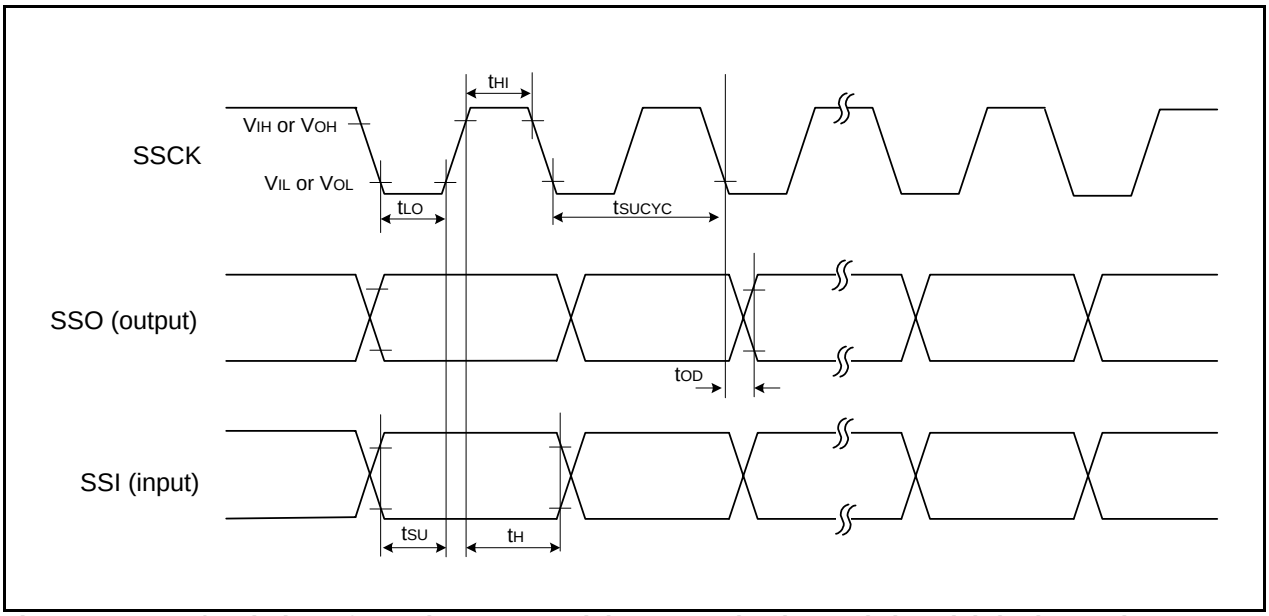


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.26 Timing Requirements of External Clock Input (XIN, XCIN)
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	50	–	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	24	–	24	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	24	–	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	20	–	20	–	20	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	10	–	10	–	10	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	10	–	10	–	10	–	µs

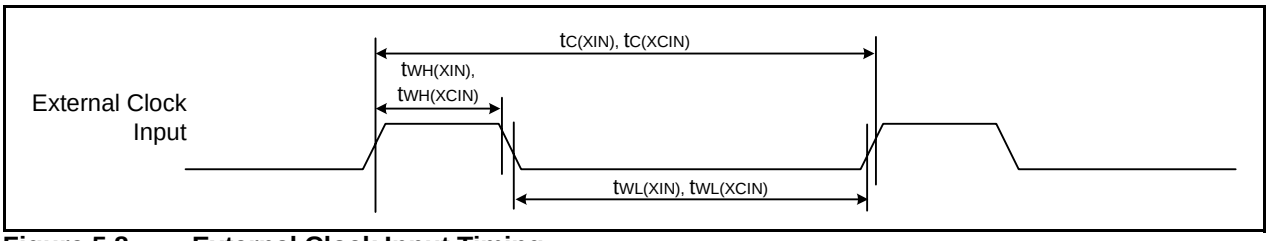


Figure 5.8 External Clock Input Timing

Table 5.27 Timing Requirements of TRJiIO (i = 0 or 1)
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJiIO input cycle time	500	–	300	–	100	–	ns
$t_{WH(TRJIO)}$	TRJiIO input “H” width	200	–	120	–	40	–	ns
$t_{WL(TRJIO)}$	TRJiIO input “L” width	200	–	120	–	40	–	ns

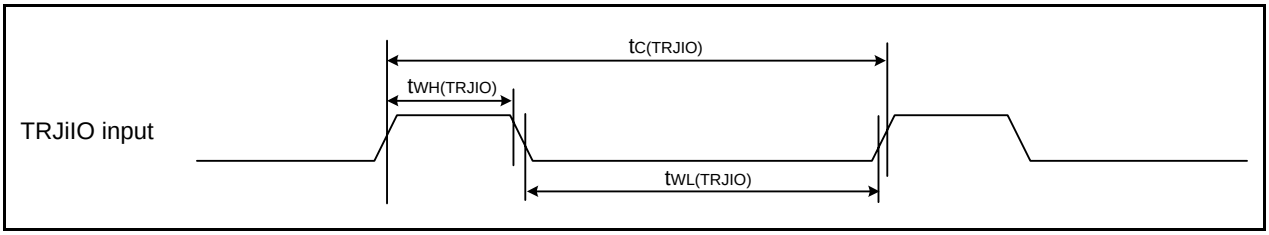


Figure 5.9 Input Timing of TRJiIO

Table 5.34 Gain Amplifier Characteristics
(VSS = 0 V and Topr = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
VGAIN	Gain amplifier operating range		0.4	–	AVCC – 1.0	V
ϕAD	A/D conversion clock		1	–	5	MHz

Table 5.35 Comparator B Characteristics
(VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	VCC – 1.4	V
VI	IVCMP1, IVCMP3 input voltage		-0.3	–	VCC + 0.3	V
–	Offset		–	5	100	mV
td	Comparator output delay time (1)	VI = Vref ± 100 mV	–	–	1	µs
ICMP	Comparator operating current	VCC = 5.0 V	–	12	–	µA

Note:
1. When the digital filter is disabled.

Table 5.36 Flash Memory (Program ROM) Characteristics
(VCC = 1.8 to 5.5 V and Topr = 0 to 60°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time		–	80	–	µs
–	Block erase time	Internal ROM Capacity: 16 KB, 32 KB, 48 KB, 64 KB	–	0.12	–	s
		Internal ROM Capacity: 96 KB, 128 KB	–	0.2	–	s
td(SR-SUS)	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
td(CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (6)	Ambient temperature = 85°C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.50 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	6	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	2.9	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	10 MHz	125 kHz	No division	–		–	2.9	–	mA
			Off	Off	10 MHz	125 kHz	Divide-by-8	–		–	1.5	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	54	200	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	36	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	3.1	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	1.7	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.02	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.3	4.5	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2.2	–	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 3.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 5.51 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P7_0, P7_1, P8 (1)	I_{OH} = –2 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P7_0, P7_1, P8 (1)	I_{OL} = 2 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 1.8 V, V_{CC} = 1.8 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 1.8 V		–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 1.8 V		85	220	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

5.2.5 AC Characteristics

Table 5.53 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	-	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1t_{CYC} + 20	ns
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

Table 5.55 Timing Requirements of External Clock Input (XIN, XCIN)
(Vss = 0 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	50	–	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	24	–	24	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	24	–	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	20	–	20	–	20	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	10	–	10	–	10	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	10	–	10	–	10	–	µs

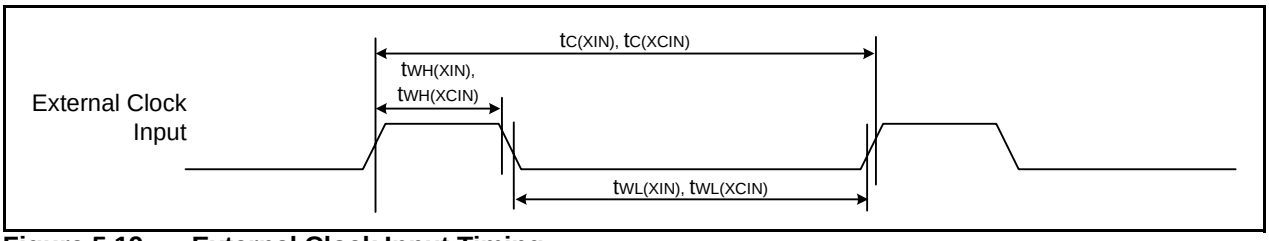


Figure 5.19 External Clock Input Timing

Table 5.56 Timing Requirements of TRJiIO (i = 0 to 2)
(Vss = 0 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJiIO input cycle time	500	–	300	–	100	–	ns
$t_{WH(TRJIO)}$	TRJiIO input “H” width	200	–	120	–	40	–	ns
$t_{WL(TRJIO)}$	TRJiIO input “L” width	200	–	120	–	40	–	ns

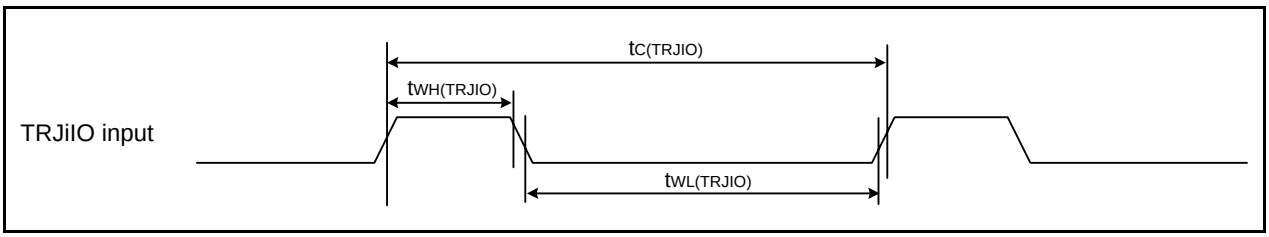
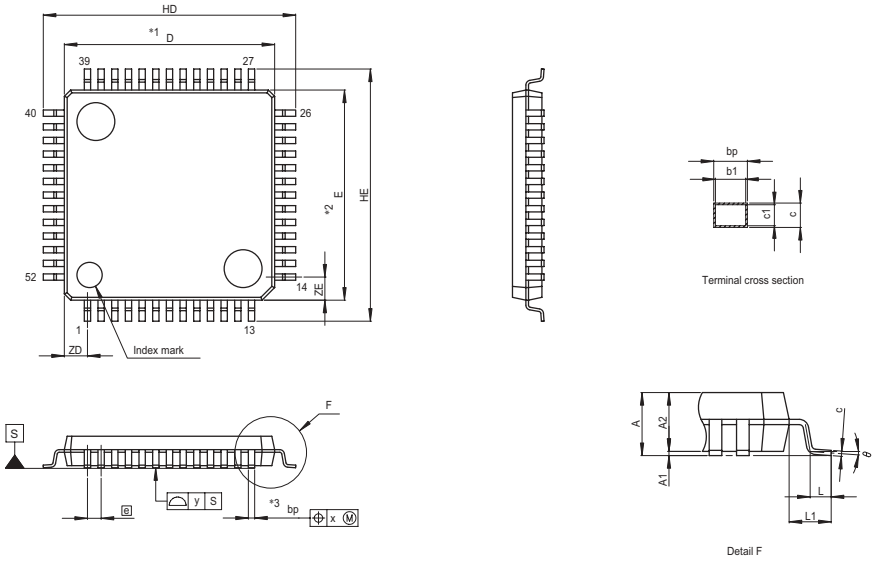


Figure 5.20 Input Timing of TRJiIO

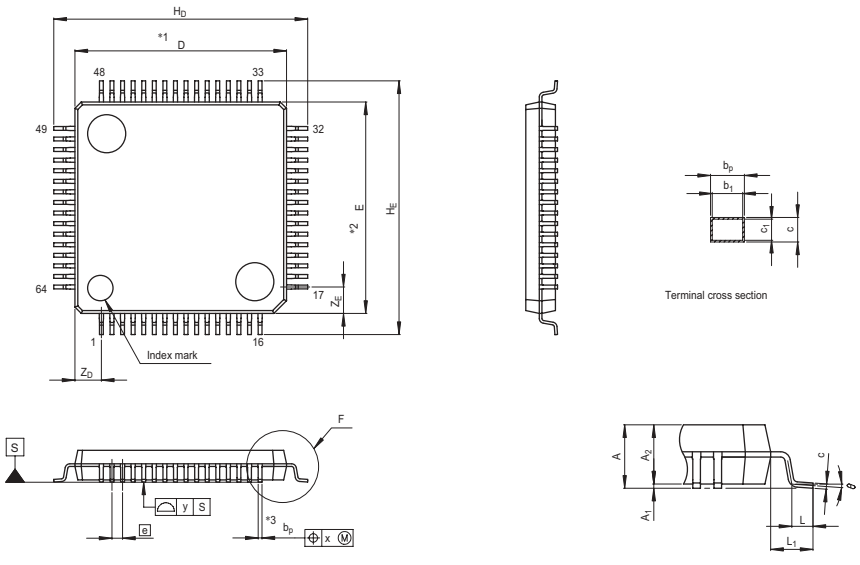
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.1