



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la86anfp-30

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Tables 1.2 and 1.3 list the Programmable I/O Ports Provided for Each Group, and Tables 1.4 and 1.5 list the LCD Display Function Pins Provided for Each Group.

Figures 1.9 to 1.12 show the pin assignment for each group, and Tables 1.9 to 1.12 list product information.

The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/LA3A Group	R8C/LA5A Group	R8C/LA6A Group	R8C/LA8A Group
I/O Ports	Programmable I/O ports	26 pins	44 pins	56 pins	72 pins
	High current drive ports	8 pins	8 pins	8 pins	10 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	6 pins	8 pins	8 pins
Timer RJ	Timer RJ0 output pin	None	None	None	1 pin
	Timer RJ1 output pin	None	None	None	1 pin
	Timer RJ2 I/O pin	None	None	None	1 pin
	Timer RJ2 output pin	None	None	None	1 pin
Timer RH	Timer RH output pin	None	1 pin	1 pin	1 pin
Serial interface	UART2	None	None	1 pin	1 pin
A/D Converter	Analog input pins	5 pins	7 pins	8 pins	12 pins
LCD Drive Control Circuit	Segment output pins	Max. 11 pins	Max. 27 pins	Max. 32 pins	Max. 40 pins
Comparator B	Analog input voltage	1 pin	2 pins	2 pins	2 pins
	Reference input voltage	1 pin	2 pins	2 pins	2 pins
Clock	XCIN pin	Shared with XIN pin	Dedicated pin	Dedicated pin	Dedicated pin
	XCOUT pin	Shared with XOUT pin	Dedicated pin	Dedicated pin	Dedicated pin
Packages		32-pin LQFP	52-pin LQFP	64-pin LQFP	80-pin LQFP

Note:

1. I/O ports are shared with I/O functions, such as interrupts or timers.
Refer to Tables 1.13 to 1.17, Pin Name Information by Pin Number, for details.

1.2 Product Lists

Tables 1.9 to 1.12 list product information for each group. Figures 1.1 to 1.4 show the Correspondence of Part No., with Memory Size and Package for each group.

Table 1.9 Product List for R8C/LA3A Group

Current of Oct 2011

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA32ANFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	N Version
R5F2LA34ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	
R5F2LA32ADFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	D Version
R5F2LA34ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	

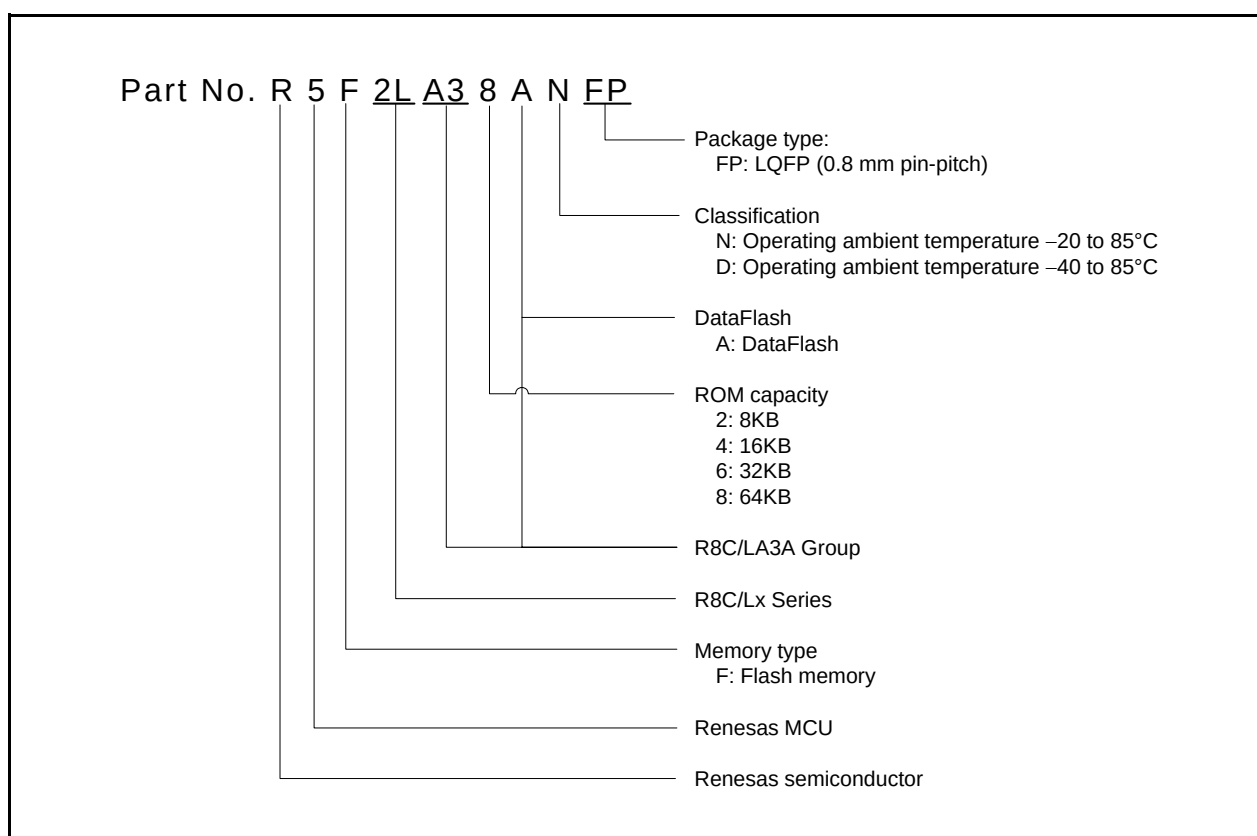


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/LA3A Group

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/LA3A Group. Figure 1.6 shows a Block Diagram of R8C/LA5A Group. Figure 1.7 shows a Block Diagram of R8C/LA6A Group. Figure 1.8 shows a Block Diagram of R8C/LA8A Group.

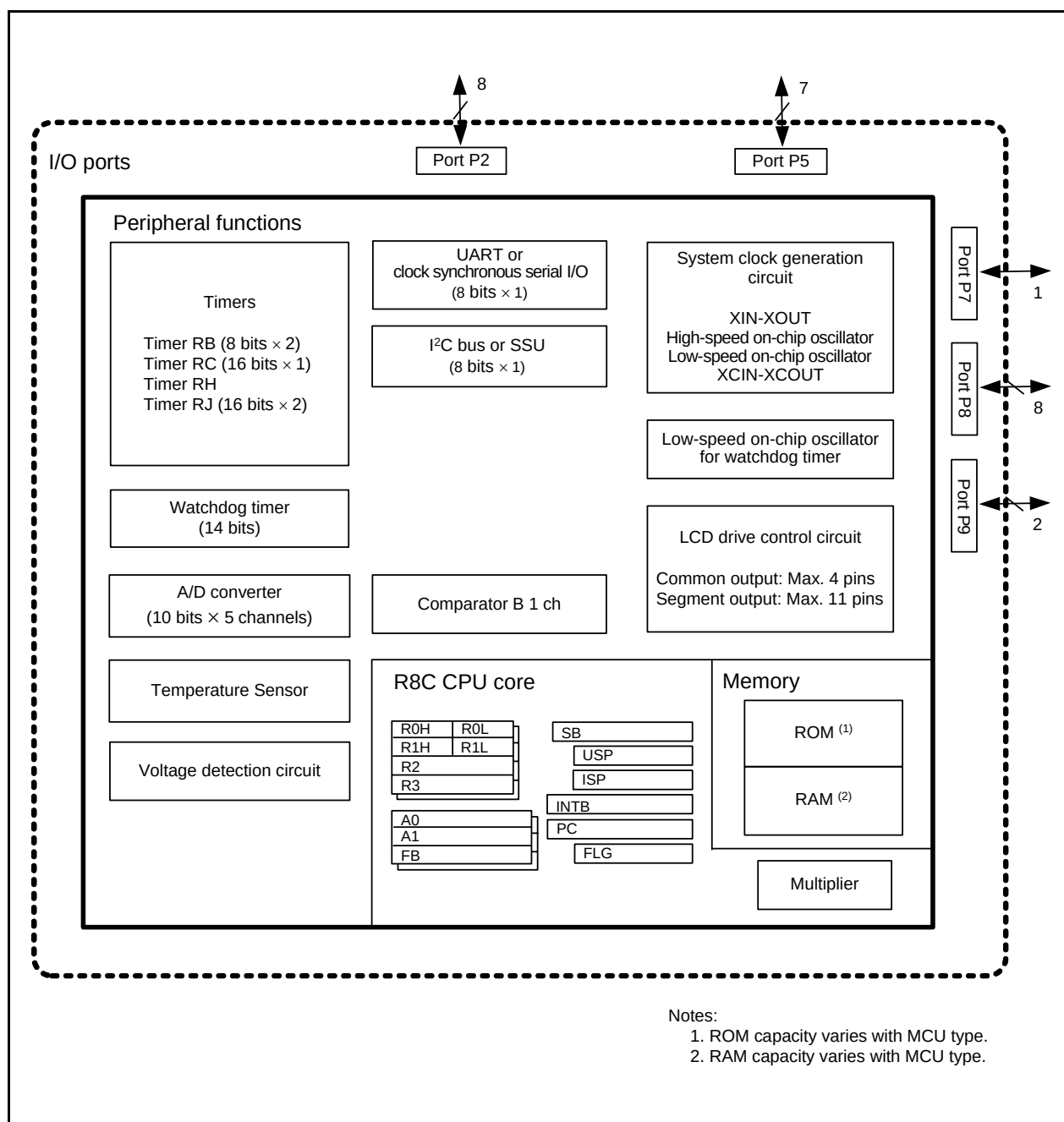


Figure 1.5 Block Diagram of R8C/LA3A Group

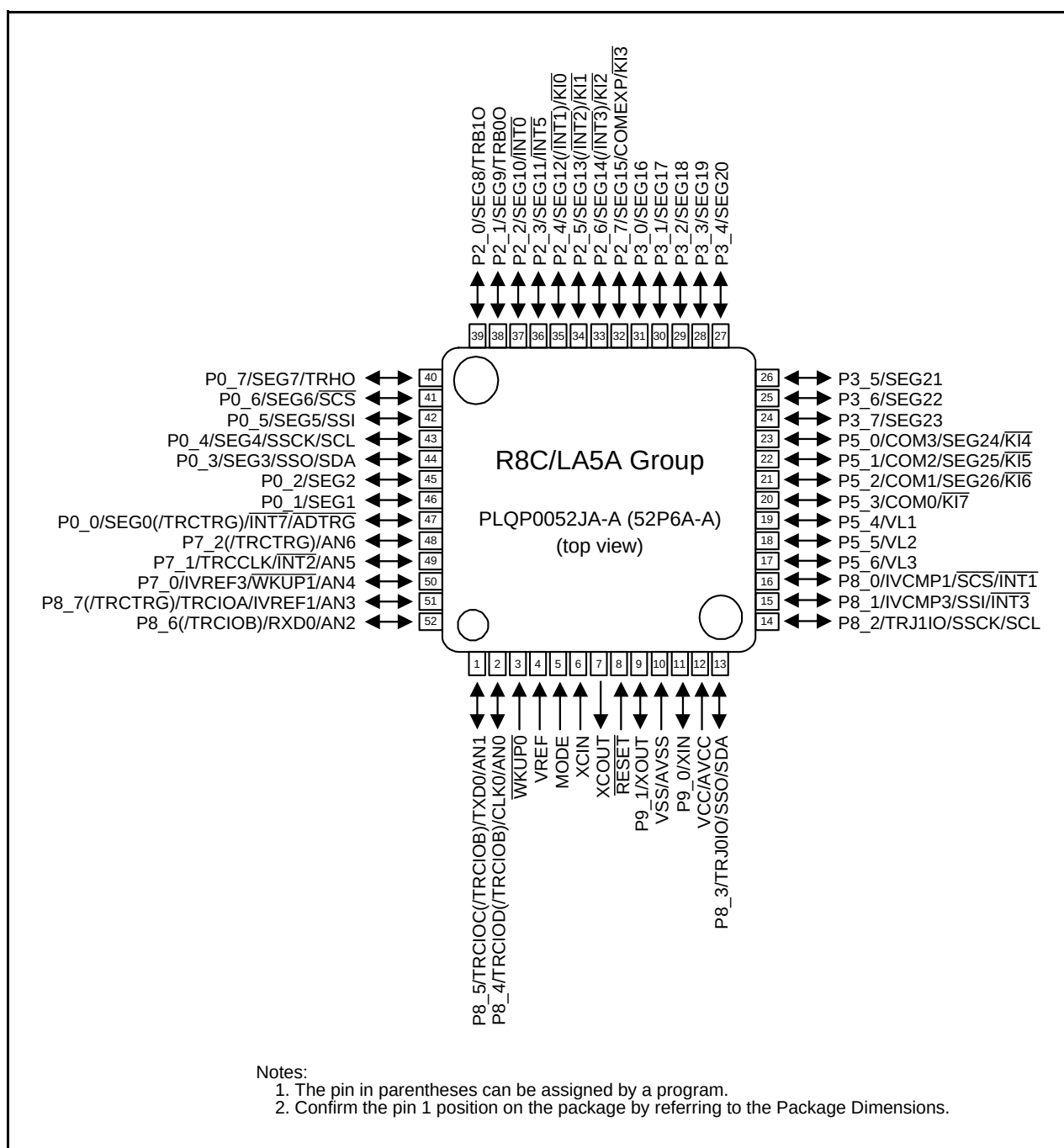


Figure 1.10 Pin Assignment (Top View) of PLQP0052JA-A Package

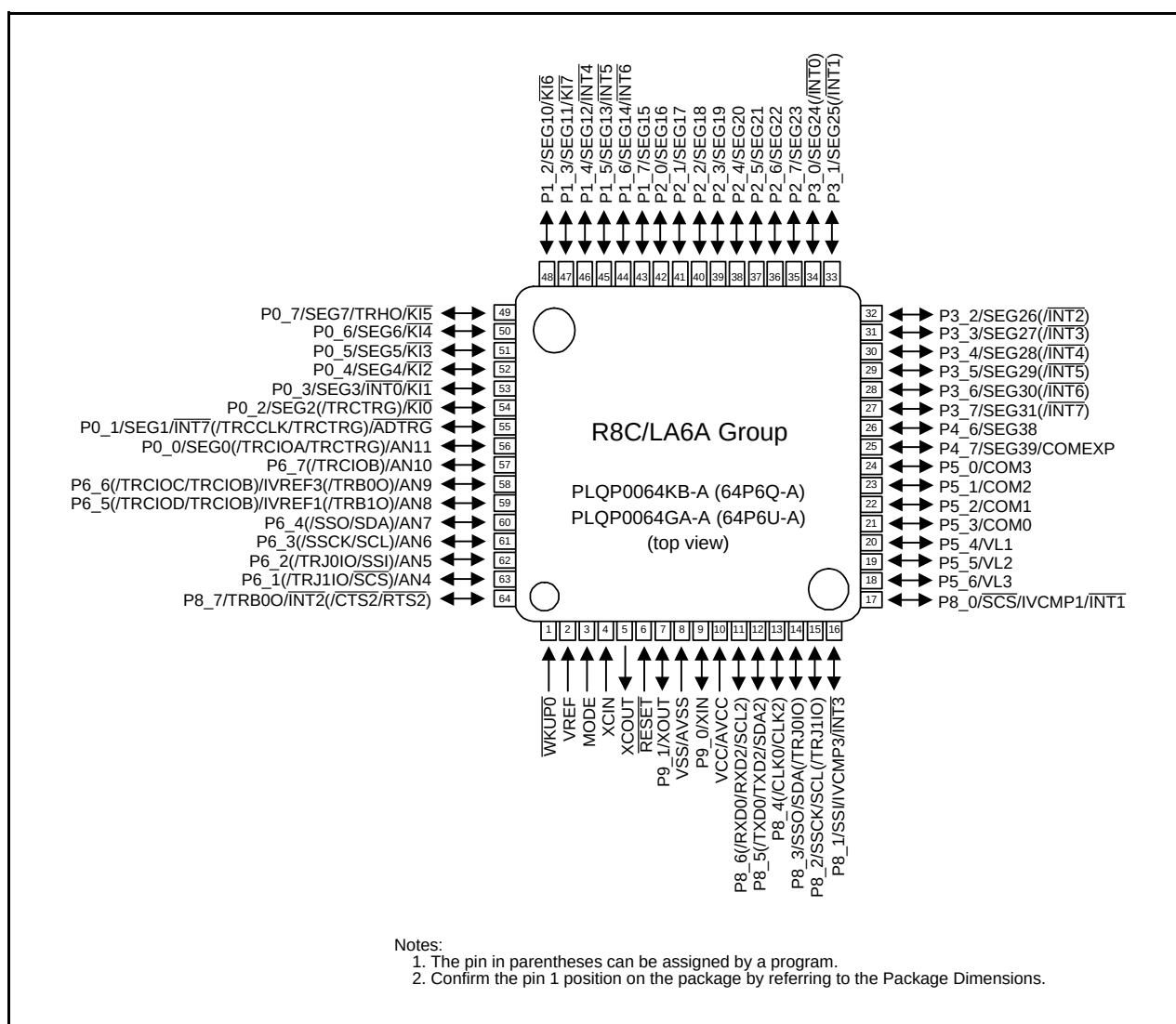


Figure 1.11 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages

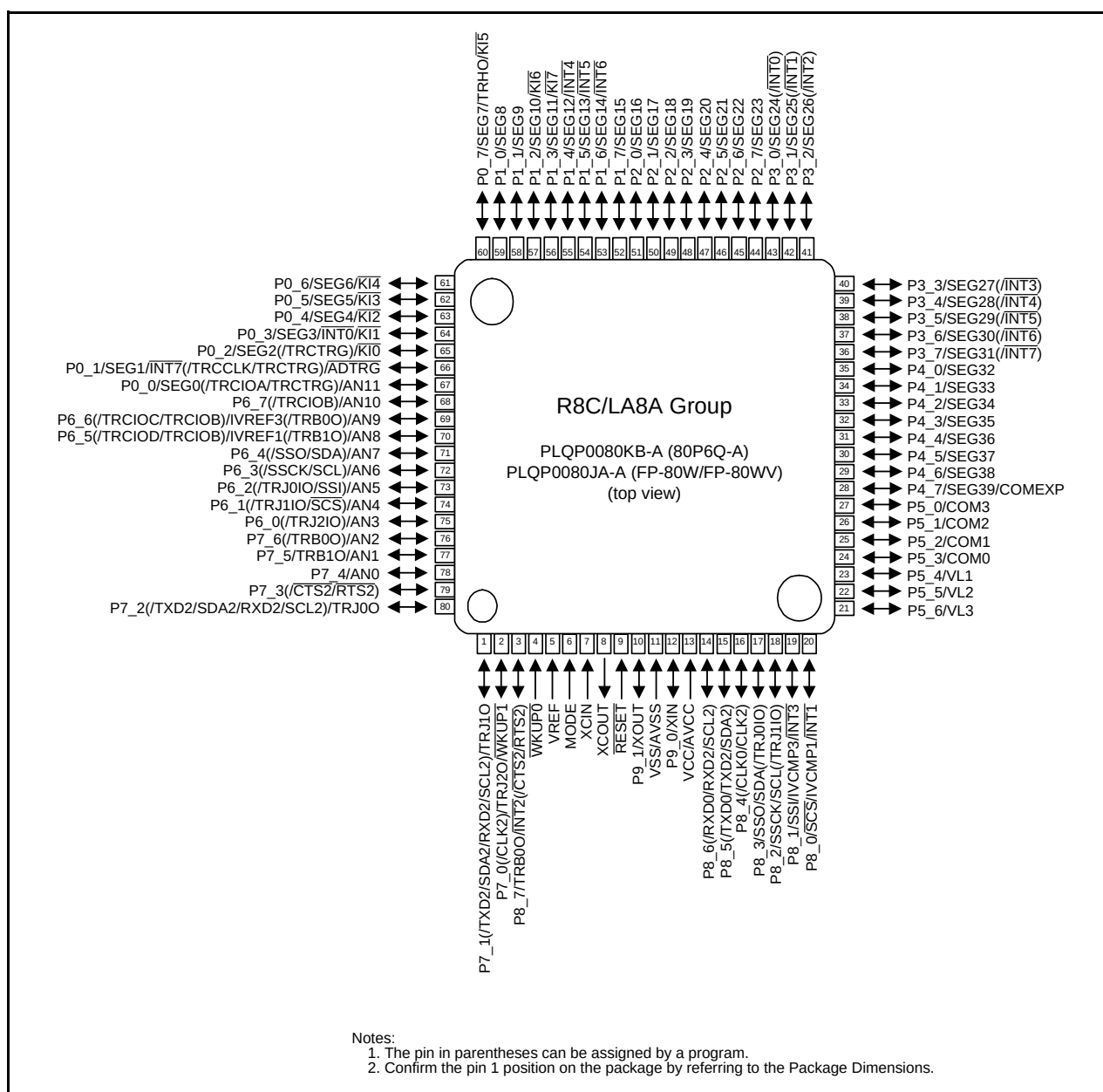


Figure 1.12 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

Table 1.17 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(3)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, Comparator B	LCD drive Control Circuit
69	58		P6_6		(TRB00/ TRCIOB/ TRCIOB)				AN9/IVREF3	
70	59		P6_5		(TRB10/ TRCIOB/ TRCIOD)				AN8/IVREF1	
71	60		P6_4				(SSO)	(SDA)	AN7	
72	61		P6_3				(SSCK)	(SCL)	AN6	
73	62		P6_2		(TRJ0IO)		(SSI)		AN5	
74	63		P6_1		(TRJ1IO)		(SCS)		AN4	
75			P6_0		(TRJ2IO)				AN3	
76			P7_6		(TRB00)				AN2	
77			P7_5		TRB10				AN1	
78			P7_4						AN0	
79			P7_3			(CTS2/RTS2)				
80			P7_2		TRJ0O	(RXD2/SCL2/ TXD2/SDA2)				

Note:

1. The pin in parentheses can be assigned by a program.

3. Memory

Figure 3.1 shows a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated higher addresses, beginning with address 03000h.

For example, two 1-Kbyte internal ROM (data flash) areas are allocated addresses 03000h to 037FFh. Two 2-Kbyte internal RAM (data flash) areas are allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 3.5-Kbyte internal RAM area is allocated addresses 00400h to 011FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

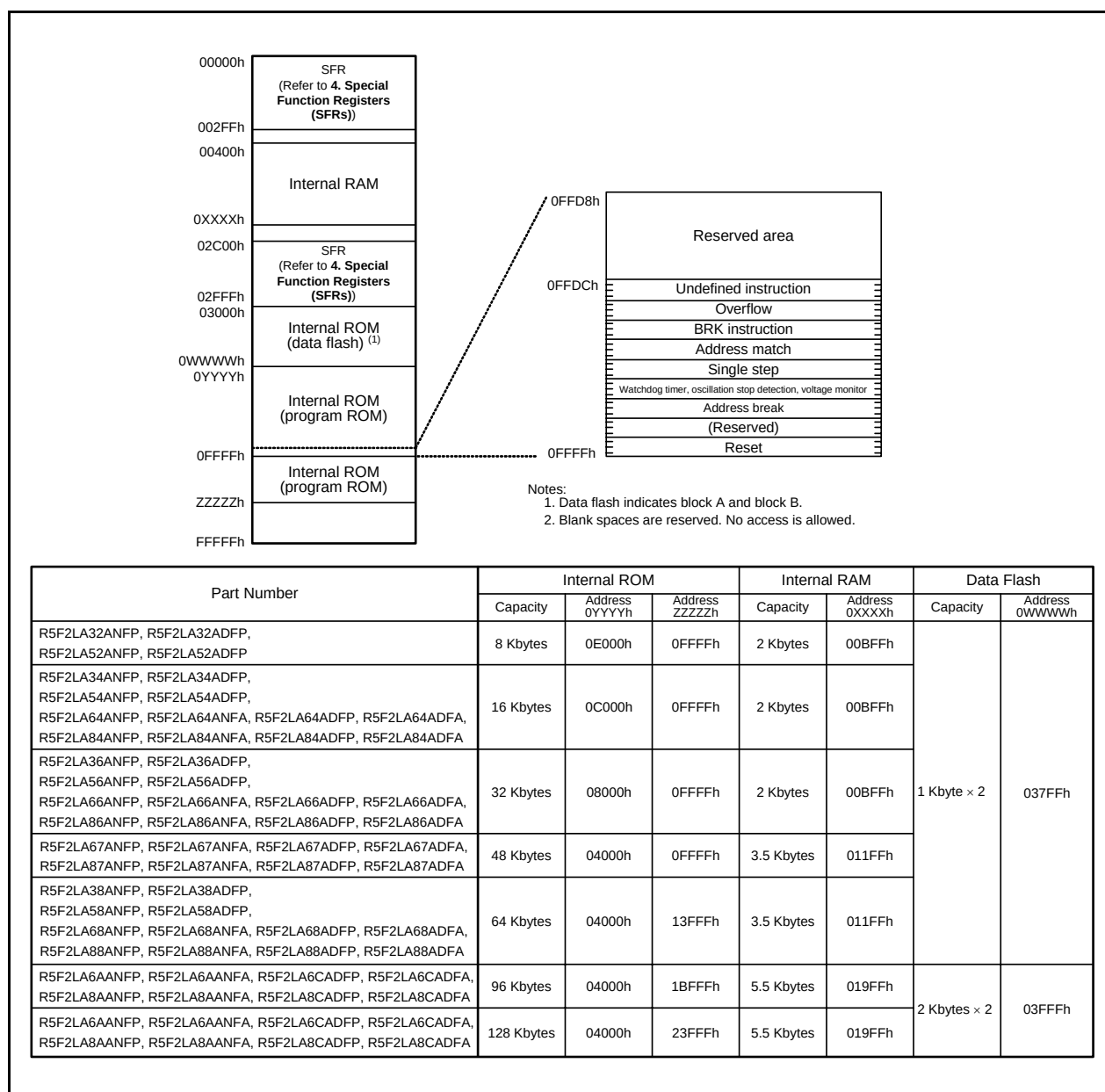


Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.9 list SFR information for R8C/LA5A Group, Tables 4.10 to 4.18 list SFR information for R8C/LA8A Group, and Table 4.19 lists the ID Code Areas and Option Function Select Area. The description offered in this chapter is based on the R8C/LA8A Group.

Table 4.1 SFR Information for R8C/LA5A Group (1) ⁽¹⁾

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h 00000100b ⁽²⁾
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register 0	MSTCR0	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh ⁽³⁾
000Ch	Oscillation Stop Detection Register	OCD	00000100b ⁽⁴⁾ 00h ⁽⁴⁾
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTs	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h	Module Standby Control Register 1	MSTCR1	00h
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽⁵⁾
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	XXXXXX00b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Frequency Control Register 0	FRC0	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator 18 MHz Set Value Register 0	FR18S0	XXh
002Ah	High-Speed On-Chip Oscillator 18 MHz Set Value Register 1	FR18S1	XXh
002Bh			
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Frequency Control Register 1	FRC1	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁶⁾ 00100000b ⁽⁷⁾
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b ⁽⁶⁾ 1100X011b ⁽⁷⁾
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- The CSPRO bit in the CSPR register is set to 1.
- The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
- The reset value differs depending on the mode.
- The CSPROINI bit in the OFS register is set to 0.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.

Table 4.7 SFR Information for R8C/LA5A Group (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RJ Pin Select Register	TRJSR	00h
0181h			
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUICSR	00h
018Dh	Timer RH Second Interrupt Control Register	TRHICR	X0XXXXXXb 00000001b ⁽³⁾
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H ⁽²⁾	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H ⁽²⁾	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	000000X0b
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.
- This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.8 SFR Information for R8C/LA5A Group (8) ⁽¹⁾

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h			
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h			
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h			
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h	Port P8 Pull-Up Control Register	P8PUR	00h
01E9h	Port P9 Pull-Up Control Register	P9PUR	00h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h	Port P8 Drive Capacity Control Register	P8DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.11 SFR Information for R8C/LA8A Group (2) ⁽¹⁾

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h	INT7 Interrupt Control Register	INT7IC	XX00X000b
0044h	INT6 Interrupt Control Register	INT6IC	XX00X000b
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RH Interrupt Control Register	TRHIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register ⁽²⁾	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RJ0 Interrupt Control Register	TRJ0IC	XXXXX000b
0057h	Timer RB1 Interrupt Control Register	TRB1IC	XXXXX000b
0058h	Timer RB0 Interrupt Control Register	TRB0IC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RJ1 Interrupt Control Register	TRJ1IC	XXXXX000b
005Ch	Timer RJ2 Interrupt Control Register	TRJ2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	LCD Interrupt Control Register	LCDIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUIICSR register.

Table 5.13 High-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8$ V to 5.5 V -20 °C $\leq T_{opr} \leq 85$ °C	19.2	20	20.8	MHz
		$V_{CC} = 1.8$ V to 5.5 V -40 °C $\leq T_{opr} \leq 85$ °C	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽¹⁾	$V_{CC} = 1.8$ V to 5.5 V -20 °C $\leq T_{opr} \leq 85$ °C	17.694	18.432	19.169	MHz
		$V_{CC} = 1.8$ V to 5.5 V -40 °C $\leq T_{opr} \leq 85$ °C	17.510	18.432	19.353	MHz
—	Oscillation stability time		—	5	30	μ s
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	530	—	μ A

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.14 Low-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	—	35	μ s
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	2	—	μ A
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time		—	—	35	μ s
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	2	—	μ A

Table 5.15 Power Supply Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = 25$ °C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽¹⁾		—	—	2000	μ s

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

5.1.4 DC Characteristics

Table 5.18 DC Characteristics (1) [4.0 V ≤ V_{CC} ≤ 5.5 V]
(T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition			Standard			Unit
						Min.	Typ.	Max.	
V _{OH}	Output "H" voltage		Port P8 ⁽¹⁾	V _{CC} = 5V	I _{OH} = −20 mA	V _{CC} − 2.0	−	V _{CC}	V
			Other pins	V _{CC} = 5V	I _{OH} = −5 mA	V _{CC} − 2.0	−	V _{CC}	V
V _{OL}	Output "L" voltage		Port P8 ⁽¹⁾	V _{CC} = 5V	I _{OL} = 20 mA	−	−	2.0	V
			Other pins	V _{CC} = 5V	I _{OL} = 5 mA	−	−	2.0	V
V _{T+} −V _{T−}	Hysteresis	INT0, INT1, INT2, INT3, INT5, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOA, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, ADTRG, RXD0, CLK0, SSI, SCL, SDA, SSO				0.05	0.5	−	V
		RESET, WKUP0				0.1	0.8	−	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5 V			−	−	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5 V			−	−	−5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5 V			20	40	80	kΩ
R _{FXIN}	Feedback resistance	XIN				−	2.0	−	MΩ
R _{FXCIN}	Feedback resistance	XCIN				−	14	−	MΩ
V _{RAM}	RAM hold voltage		During stop mode			1.8	−	−	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.21 DC Characteristics (4) [2.7 V ≤ V_{CC} < 4.0 V]**(T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)**

Symbol	Parameter		Condition							Standard			Unit	
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)		Max .
			XIN (2)	XCIN	High-Speed	Low-Speed								
Icc	Power supply current ⁽¹⁾	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	4.7	10	mA	
			10 MHz	Off	Off	125 kHz	No division	—		—	2.3	6	mA	
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	—	2.9	—	mA	
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.8	—	mA	
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.0	—	mA	
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—		—	5.0	11	mA	
			Off	Off	20 MHz	125 kHz	Divide-by-8	—		—	2.1	—	mA	
			Off	Off	10 MHz	125 kHz	No division	—		—	2.9	—	mA	
			Off	Off	10 MHz	125 kHz	Divide-by-8	—		—	1.5	—	mA	
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		—	0.9	—	mA	
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		—	106	300	μA	
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		—	54	200	μA	
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		—	54	200	μA	
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	—	36	—	μA	
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	—	9.0	50	μA	
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	—	2.5	31	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit ⁽⁴⁾ When external division resistors are used	—	3.1	—	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	—	1.7	—	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM10 = 1	While a WAIT instruction is executed Peripheral clock off	—	0.5	2.2	μA	
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25 °C Peripheral clock off	—	0.5	2.2	μA	
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off	—	1.2	—	μA	
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25 °C	—	0.01	0.1	μA	
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85 °C	—	0.02	—	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25 °C	—	1.3	4.5	μA	
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85 °C	—	2.2	—	μA	

Notes:

1. V_{CC} = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are V_{SS}.
2. XIN is set to square wave input.
3. V_{CC} = 3.0 V
4. VLCD = V_{CC}, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

Table 5.22 DC Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage		Port P8 (1)	IOH = -2 mA	VCC - 0.5	—	VCC	V
			Other pins	IOH = -1 mA	VCC - 0.5	—	VCC	V
VOL	Output "L" voltage		Port P8 (1)	IOL = 2 mA	—	—	0.5	V
			Other pins	IOL = 1 mA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT5, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, ADTRG, RXD0, CLK0, SSI, SCL, SDA, SSO			0.05	0.4	—	V
		RESET, WKUP0			0.1	0.8	—	V
IiH	Input "H" current		VI = 1.8 V, VCC = 1.8 V		—	—	4.0	μA
IiL	Input "L" current		VI = 0 V, VCC = 1.8 V		—	—	-4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, VCC = 1.8 V		85	220	500	kΩ
RfXIN	Feedback resistance	XIN			—	2.0	—	MΩ
RfXCIN	Feedback resistance	XCIN			—	14	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

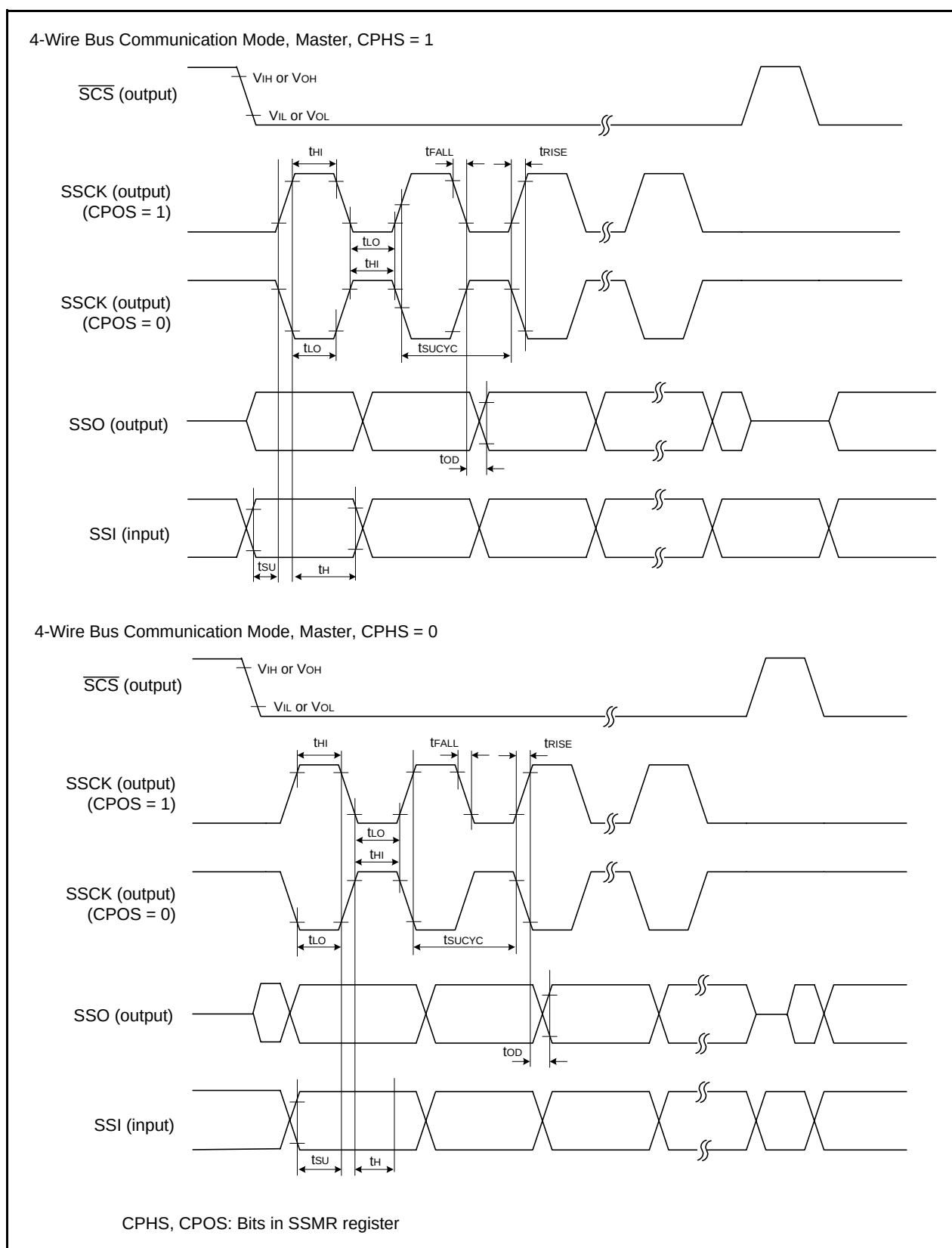


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.54 Timing Requirements of I²C bus Interface ⁽¹⁾
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cyC} + 600 ⁽¹⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{cyC} + 300 ⁽¹⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{cyC} + 500 ⁽¹⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{cyC} ⁽¹⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cyC} ⁽¹⁾	–	–	ns
t _{STAH}	Start condition input hold time		3t _{cyC} ⁽¹⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cyC} ⁽¹⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{cyC} ⁽¹⁾	–	–	ns
t _{SDAS}	Data input setup time		1t _{cyC} + 40 ⁽¹⁾	–	–	ns
t _{SDAH}	Data input hold time		10	–	–	ns

Note:

1. 1t_{cyC} = 1/f₁(s)

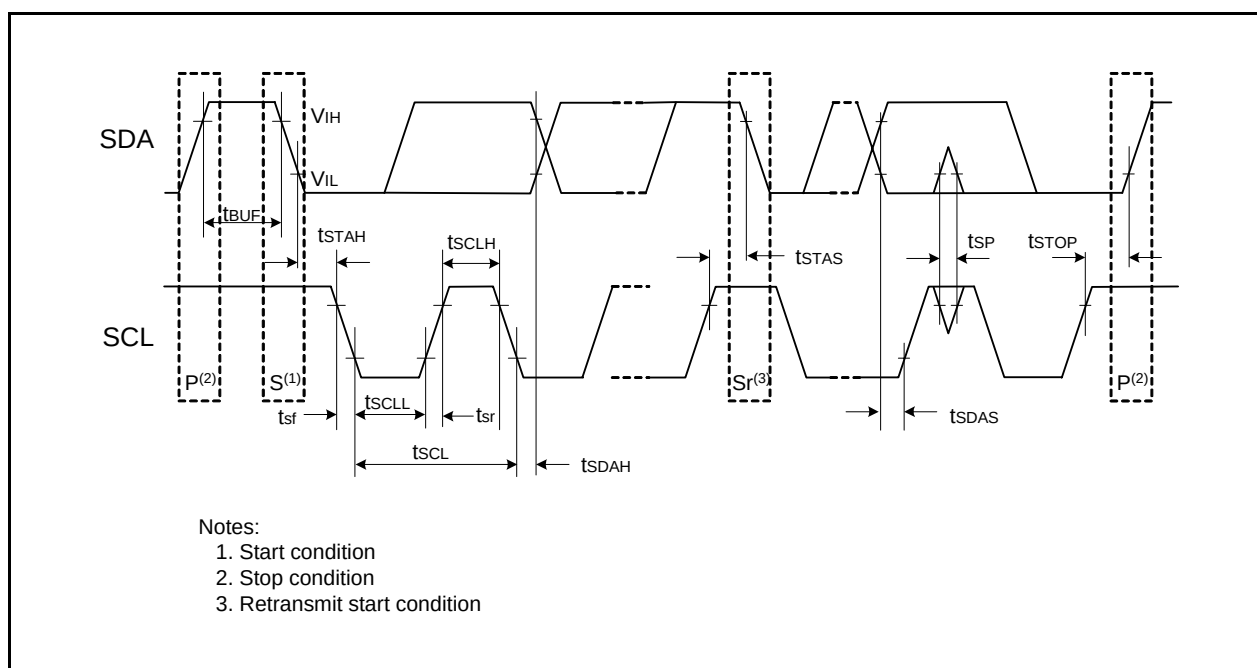
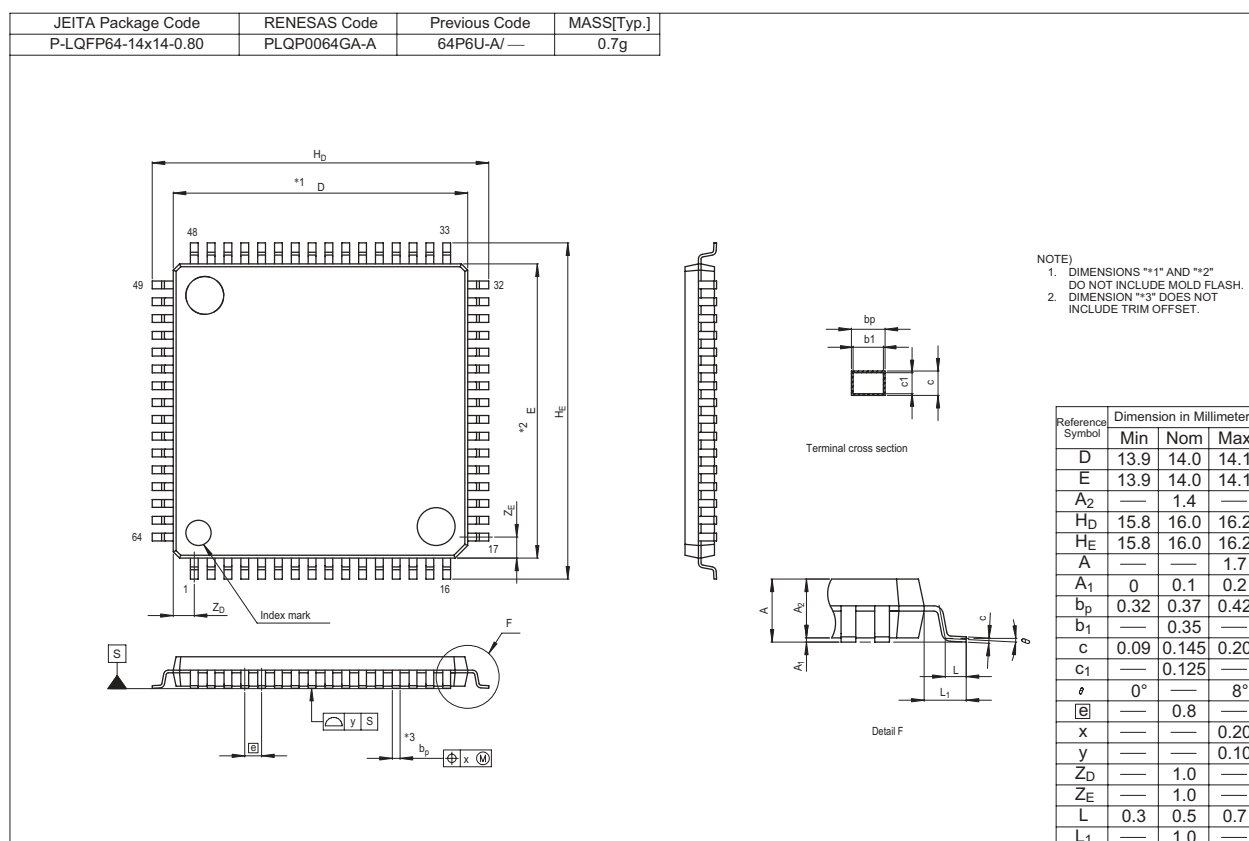


Figure 5.18 I/O Timing of I²C bus Interface



REVISION HISTORY

R8C/LA3A Group, R8C/LA5A Group, R8C/LA6A Group, R8C/LA8A Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Jan 18, 2010	—	First Edition issued
0.02	Jul 16, 2010	2	Table 1.1 revised
		3	Table 1.2 revised
		4	Tables 1.4 and 1.5 revised
		5	Table 1.6 revised
		6	Table 1.7 revised
		7	Table 1.8 revised
		8	Table 1.9 and Figure 1.1 revised
		9	Table 1.10 and Figure 1.2 revised
		10	Table 1.11 and Figure 1.3 revised
		11	Table 1.12 revised
		12	Figure 1.5 revised
		13	Figure 1.6 revised
		14	Figure 1.7 revised
		16	Figure 1.9 revised
		17	Figure 1.10 revised
		18	Table 1.13 revised
		19	Table 1.14 revised
		20	Figure 1.11 revised
		21	Figure 1.12 revised
		25	Table 1.18 revised
		26	Table 1.19 revised
		30	Figure 3.1 revised
		31	Table 4.1, Note 3 revised
		35	Table 4.5 revised
		41 to 44	Package Dimensions revised
1.00	Dec 21, 2010	All	“Preliminary” and “Under development” deleted
		2	Table 1.1 revised
		3	Tables 1.2 and 1.3 Note 2 revised
		4	Tables 1.4 and 1.5 Note 1 revised
		6	Table 1.7 revised
		7	Table 1.8 revised
		10	Table 1.11 and Figure 1.3 revised
		12	Figure 1.5 revised
		13	Figure 1.6 revised
		14	Figure 1.7 revised
		15	Figure 1.8 revised
		16	Figure 1.9 revised
		18	Table 1.13 revised
		19	Table 1.14 revised
		20	Figure 1.11 revised
		22	Table 1.15 revised
		23	Table 1.16 revised
		24	Table 1.17 revised
		25, 26	Tables 1.18 and 1.19 Pin Functions for R8C/LA5A Group added