Renesas Electronics America Inc - R5F2LA87ADFA#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	3.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la87adfa-v0

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Tables 1.2 and 1.3 list the Programmable I/O Ports Provided for Each Group, and Tables 1.4 and 1.5 list the LCD Display Function Pins Provided for Each Group.
Figures 1.9 to 1.12 show the pin assignment for each group, and Tables 1.9 to 1.12 list product information.
The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/LA3A Group	R8C/LA5A Group	R8C/LA6A Group	R8C/LA8A Group
I/O Ports	Programmable I/O ports	26 pins	44 pins	56 pins	72 pins
	High current drive ports	8 pins	8 pins	8 pins	10 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	6 pins	8 pins	8 pins
Timer RJ	Timer RJ0 output pin	None	None	None	1 pin
	Timer RJ1 output pin	None	None	None	1 pin
	Timer RJ2 I/O pin	None	None	None	1 pin
	Timer RJ2 output pin	None	None	None	1 pin
Timer RH	Timer RH output pin	None	1 pin	1 pin	1 pin
Serial interface	UART2	None	None	1 pin	1 pin
A/D Converter	Analog input pins	5 pins	7 pins	8 pins	12 pins
LCD Drive Control Circuit	Segment output pins	Max. 11 pins	Max. 27 pins	Max. 32 pins	Max. 40 pins
Comparator B	Analog input voltage	1 pin	2 pins	2 pins	2 pins
	Reference input voltage	1 pin	2 pins	2 pins	2 pins
Clock	XCIN pin	Shared with XIN pin	Dedicated pin	Dedicated pin	Dedicated pin
	XCOUT pin	Shared with XOUT pin	Dedicated pin	Dedicated pin	Dedicated pin
Packages		32-pin LQFP	52-pin LQFP	64-pin LQFP	80-pin LQFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
   Refer to Tables 1.13 to 1.17, Pin Name Information by Pin Number, for details.

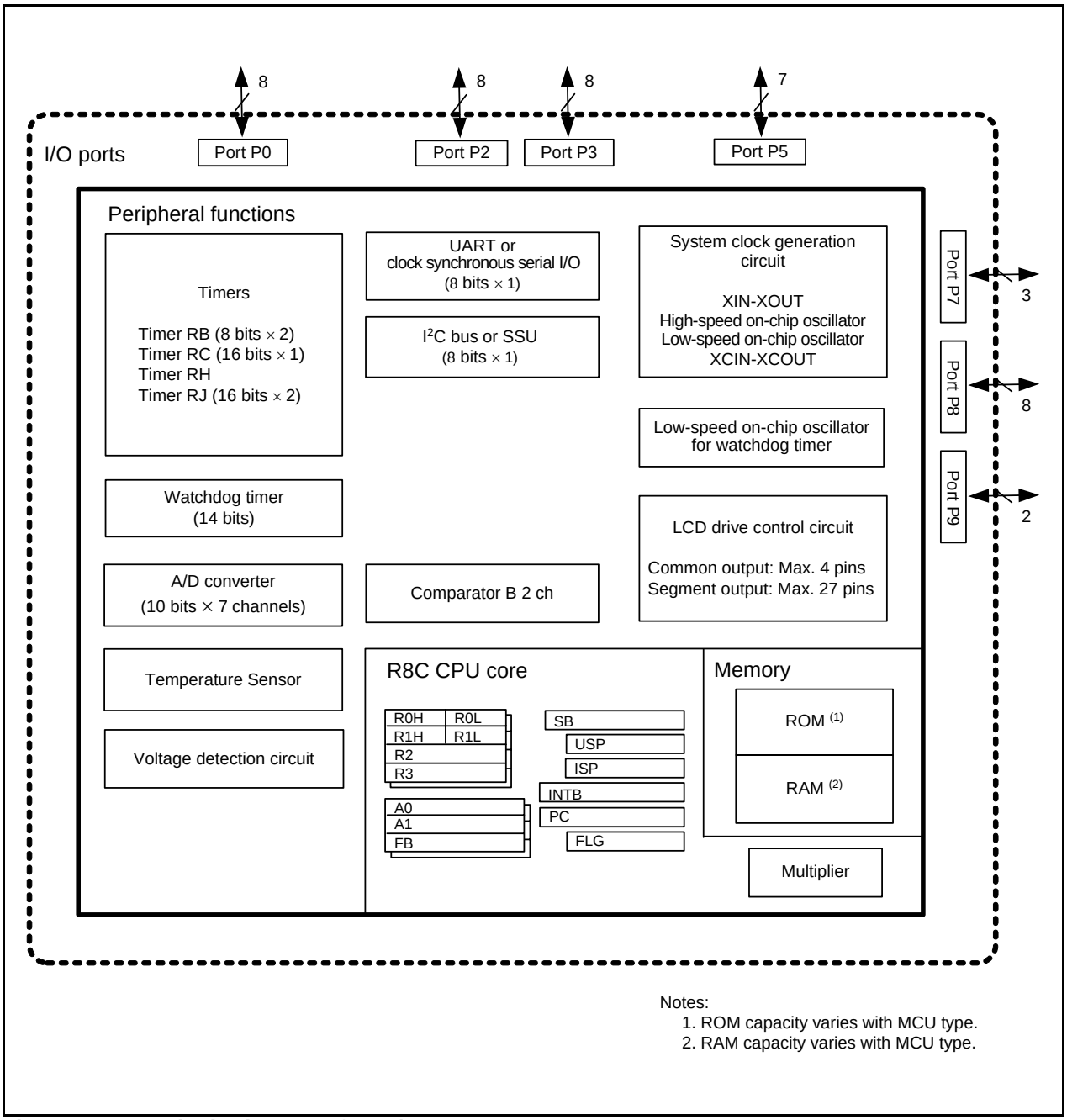


Figure 1.6 Block Diagram of R8C/LA5A Group

Table 1.21 Pin Functions for R8C/LA8A Group (2)

Item	Pin Name	I/O Type	Description
I^2C bus	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{SCS}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter.
A/D converter	AN0 to AN11	I	A/D converter analog input pins.
	$\overline{ADTRG}$	I	AD external trigger input pin.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_6, P6_0 to P6_7 P7_0 to P7_6, P8_0 to P8_7, P9_0, P9_1	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Ports P7_0, P7_1 and P8 can be used as LED drive ports.
Segment output	SEG0 to SEG39	O	LCD segment output pins.
Common output	COM0 to COM3, COMEXP	O	LCD common output pins.
LCD power supply	VL1	I	Apply the following voltage: 1 V ≤ VL1 ≤ VCC and VL1 ≤ VL2.
	VL2	I	Apply the following voltage: VL2 ≤ 5.5 V and VL1 ≤ VL2 ≤ VL3.
	VL3	I	Apply the following voltage: VL3 ≤ 5.5 V and VL2 ≤ VL3.

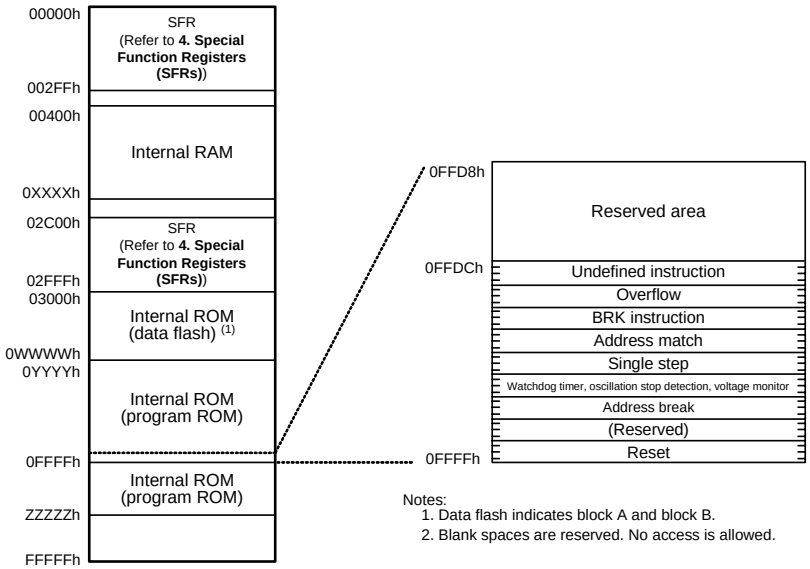
I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

3. Memory

Figure 3.1 shows a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated higher addresses, beginning with address 03000h.
For example, two 1-Kbyte internal ROM (data flash) areas are allocated addresses 03000h to 037FFh. Two 2-Kbyte internal RAM (data flash) areas are allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 3.5-Kbyte internal RAM area is allocated addresses 00400h to 011FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A and block B.
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM		Data Flash	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh	Capacity	Address 0WWWWh
R5F2LA32ANFP, R5F2LA32ADFP, R5F2LA52ANFP, R5F2LA52ADFP	8 Kbytes	0E000h	0FFFFh	2 Kbytes	00BFFh	1 Kbyte × 2	037FFh
R5F2LA34ANFP, R5F2LA34ADFP, R5F2LA54ANFP, R5F2LA54ADFP, R5F2LA64ANFP, R5F2LA64ANFA, R5F2LA64ADFP, R5F2LA64ADFA, R5F2LA84ANFP, R5F2LA84ANFA, R5F2LA84ADFP, R5F2LA84ADFA	16 Kbytes	0C000h	0FFFFh	2 Kbytes	00BFFh		
R5F2LA36ANFP, R5F2LA36ADFP, R5F2LA56ANFP, R5F2LA56ADFP, R5F2LA66ANFP, R5F2LA66ANFA, R5F2LA66ADFP, R5F2LA66ADFA, R5F2LA86ANFP, R5F2LA86ANFA, R5F2LA86ADFP, R5F2LA86ADFA	32 Kbytes	08000h	0FFFFh	2 Kbytes	00BFFh		
R5F2LA67ANFP, R5F2LA67ANFA, R5F2LA67ADFP, R5F2LA67ADFA, R5F2LA87ANFP, R5F2LA87ANFA, R5F2LA87ADFP, R5F2LA87ADFA	48 Kbytes	04000h	0FFFFh	3.5 Kbytes	011FFh		
R5F2LA38ANFP, R5F2LA38ADFP, R5F2LA58ANFP, R5F2LA58ADFP, R5F2LA68ANFP, R5F2LA68ANFA, R5F2LA68ADFP, R5F2LA68ADFA, R5F2LA88ANFP, R5F2LA88ANFA, R5F2LA88ADFP, R5F2LA88ADFA	64 Kbytes	04000h	13FFFh	3.5 Kbytes	011FFh		
R5F2LA6AANFP, R5F2LA6AANFA, R5F2LA6CADFP, R5F2LA6CADFA, R5F2LA8AANFP, R5F2LA8AANFA, R5F2LA8CADFP, R5F2LA8CADFA	96 Kbytes	04000h	1BFFFh	5.5 Kbytes	019FFh	2 Kbytes × 2	03FFFh
R5F2LA6AANFP, R5F2LA6AANFA, R5F2LA6CADFP, R5F2LA6CADFA, R5F2LA8AANFP, R5F2LA8AANFA, R5F2LA8CADFP, R5F2LA8CADFA	128 Kbytes	04000h	23FFFh	5.5 Kbytes	019FFh		

Figure 3.1 Memory Map

5.1.3 Peripheral Function Characteristics

Table 5.3 A/D Converter Characteristics
(Vcc/AVcc = Vref = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVcc		–	–	10	Bit
–	Absolute accuracy (2)	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	–	–	±3	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	–	–	±5	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	–	–	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	–	–	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	–	–	±2	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	20	MHz
			3.2 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	16	MHz
			2.7 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	10	MHz
			1.8 ≤ Vref = AVcc ≤ 5.5 V (1)		1	–	8	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	–	–	ms
tSAMP	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
IVref	Vref current		Vcc = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
Vref	Reference voltage				1.8	–	AVcc	V
VIA	Analog input voltage (3)				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:
1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Temperature Sensor Characteristics
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
VTMP	Temperature sensor output voltage	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz Ambient temperature = 25 °C	550	600	650	mV
–	Temperature coefficient	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz Ambient temperature = 25 °C	–	–2.1	–	mV/°C
–	Start-up time	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz	–	–	200	µs
ITMP	Operating current	1.8 V ≤ Vref = AVcc ≤ 5.5 V ϕAD = 1.0 MHz to 5.0 MHz	–	100	–	µA

Table 5.5 Gain Amplifier Characteristics
(V_{SS} = 0 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{GAIN}	Gain amplifier operating range		0.4	—	AV_{CC} – 1.0	V
ϕAD	A/D conversion clock		1	—	5	MHz

Table 5.6 Comparator B Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	–	V_{CC} + 0.3	V
–	Offset		–	5	100	mV
t_d	Comparator output delay time (1)	V_I = Vref ± 100 mV	–	–	1	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	–	12	–	µA

Note:
1. When the digital filter is disabled.

Table 5.11 Voltage Detection 2 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

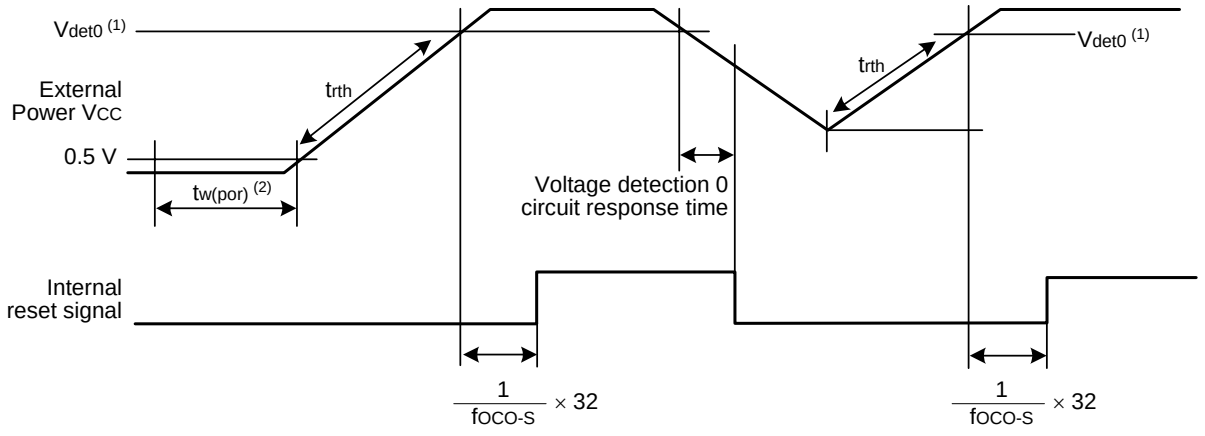
Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0 (1)	At the falling of V_{CC}		3.70	4.0	4.30	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit			–	0.10	–	V
–	Voltage detection 2 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	20	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	200	500	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.12 Power-on Reset Circuit Characteristics (1)
(T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		0	–	50000	mV/ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** in the User's Manual: Hardware for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Characteristics

5.1.4 DC Characteristics

Table 5.18 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition			Standard			Unit
						Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P8 (1)	V_{CC} = 5V	I_{OH} = –20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Other pins	V_{CC} = 5V	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P8 (1)	V_{CC} = 5V	I_{OL} = 20 mA	–	–	2.0	V
			Other pins	V_{CC} = 5V	I_{OL} = 5 mA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT5}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, CLK0, SSI, SCL, SDA, SSO				0.05	0.5	–	V
		$\overline{RESET}$, $\overline{WKUP0}$				0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V			–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V			–	–	–5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5 V			20	40	80	kΩ
R_{fXIN}	Feedback resistance	XIN				–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN				–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode			1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.21 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition							Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	6	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	2.9	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	10 MHz	125 kHz	No division	–		–	2.9	–	mA
			Off	Off	10 MHz	125 kHz	Divide-by-8	–		–	1.5	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	54	200	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	36	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	3.1	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	1.7	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25 °C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25 °C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85 °C	–	0.02	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25 °C	–	1.3	4.5	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85 °C	–	2.2	–	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 3.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

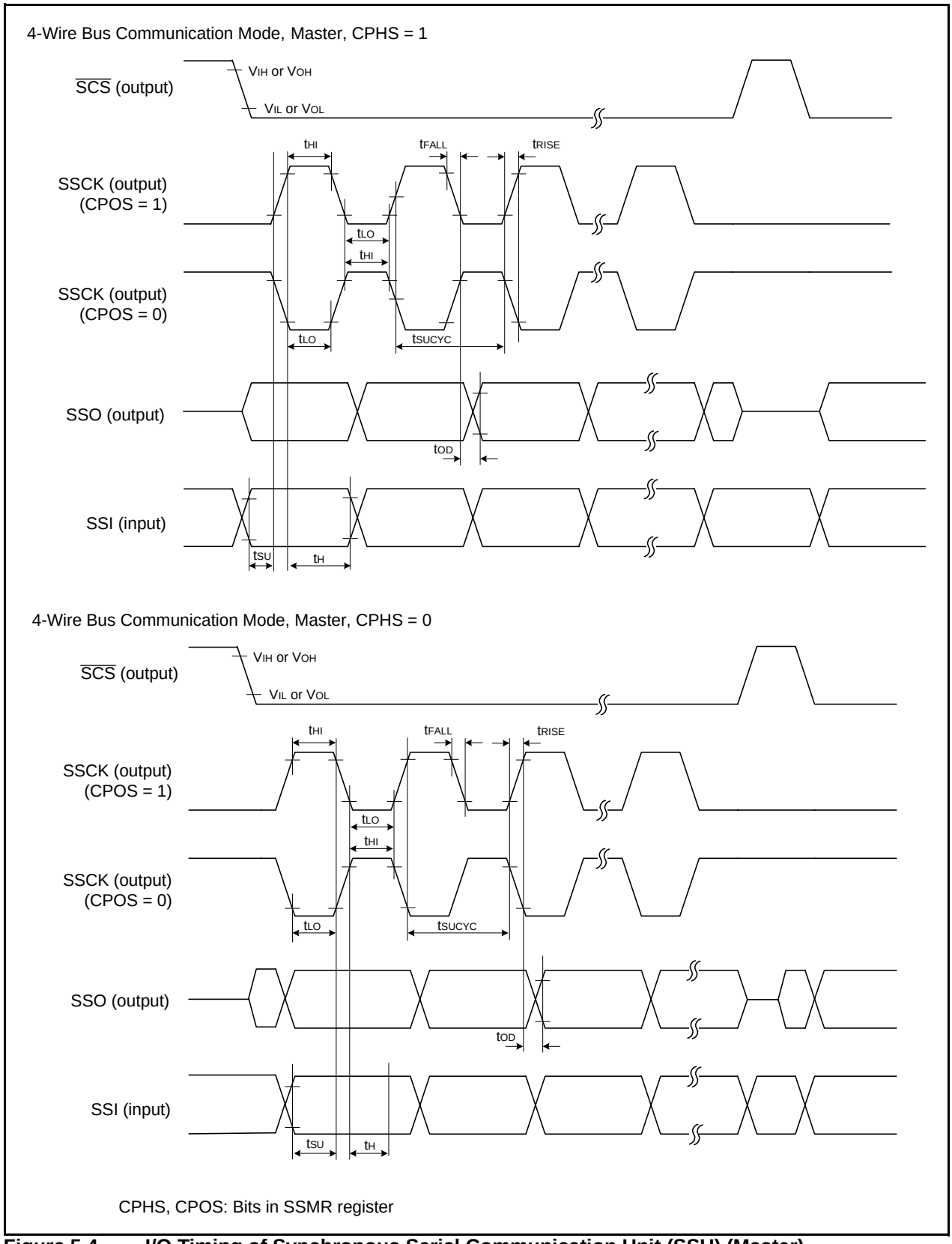


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.26 Timing Requirements of External Clock Input (XIN, XCIN)
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	50	–	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	24	–	24	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	24	–	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	20	–	20	–	20	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	10	–	10	–	10	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	10	–	10	–	10	–	µs

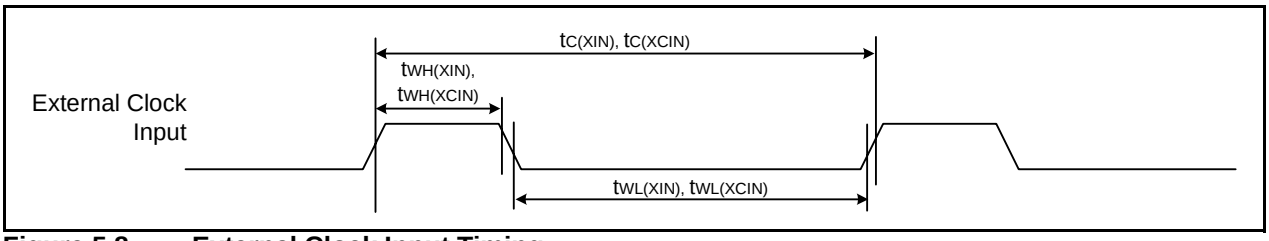


Figure 5.8 External Clock Input Timing

Table 5.27 Timing Requirements of TRJiIO (i = 0 or 1)
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJiIO input cycle time	500	–	300	–	100	–	ns
$t_{WH(TRJIO)}$	TRJiIO input “H” width	200	–	120	–	40	–	ns
$t_{WL(TRJIO)}$	TRJiIO input “L” width	200	–	120	–	40	–	ns

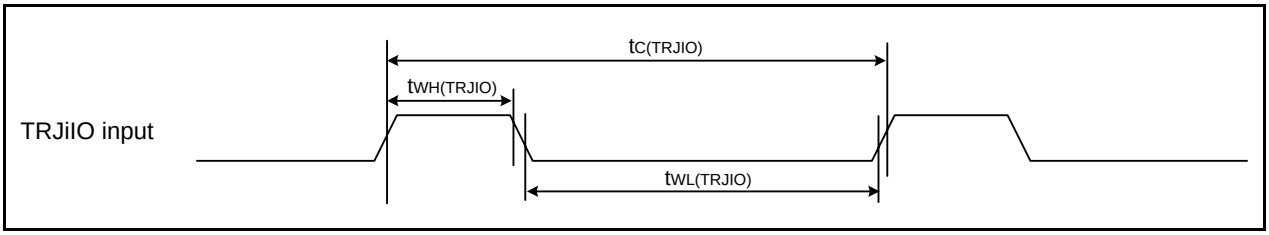


Figure 5.9 Input Timing of TRJiIO

5.2 Electrical Characteristics (R8C/LA6A Group and R8C/LA8A Group)

5.2.1 Absolute Maximum Ratings

Table 5.30 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		P5_4/VL1		–0.3 to VL2 (2)	V
		P5_5/VL2		VL1 to VL3	V
		P5_6/VL3		VL2 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		COM0 to COM3		–0.3 to VL3	V
		SEG0 to SEG39		–0.3 to VL3	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version)/ –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

Table 5.34 Gain Amplifier Characteristics
(VSS = 0 V and Topr = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
VGAIN	Gain amplifier operating range		0.4	–	AVCC – 1.0	V
ϕAD	A/D conversion clock		1	–	5	MHz

Table 5.35 Comparator B Characteristics
(VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	VCC – 1.4	V
VI	IVCMP1, IVCMP3 input voltage		-0.3	–	VCC + 0.3	V
–	Offset		–	5	100	mV
td	Comparator output delay time (1)	VI = Vref ± 100 mV	–	–	1	µs
ICMP	Comparator operating current	VCC = 5.0 V	–	12	–	µA

Note:
1. When the digital filter is disabled.

Table 5.36 Flash Memory (Program ROM) Characteristics
(VCC = 1.8 to 5.5 V and Topr = 0 to 60°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time		–	80	–	µs
–	Block erase time	Internal ROM Capacity: 16 KB, 32 KB, 48 KB, 64 KB	–	0.12	–	s
		Internal ROM Capacity: 96 KB, 128 KB	–	0.2	–	s
td(SR-SUS)	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
td(CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (6)	Ambient temperature = 85°C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.38 Voltage Detection 0 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)			1.8	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)			2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)			2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)			3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (3)	In operation	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	50	500	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	100	500	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V		–	1.5	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.39 Voltage Detection 1 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	At the falling of Vcc		2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	At the falling of Vcc		2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	At the falling of Vcc		2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	At the falling of Vcc		2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	At the falling of Vcc		2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	At the falling of Vcc		2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	At the falling of Vcc		2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	At the falling of Vcc		3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	At the falling of Vcc		3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	At the falling of Vcc		3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	At the falling of Vcc		3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	At the falling of Vcc		3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	At the falling of Vcc		3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	At the falling of Vcc		3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	At the falling of Vcc		4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	At the falling of Vcc		4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected		–	0.07	–	V
		Vdet1_6 to Vdet1_F selected		–	0.10	–	V
–	Voltage detection 1 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	60	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	250	500	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.42 High-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	VCC = 1.8 V to 5.5 V – 20°C ≤ Topr ≤ 85°C	19.2	20	20.8	MHz
		VCC = 1.8 V to 5.5 V – 40°C ≤ Topr ≤ 85°C	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (1)	VCC = 1.8 V to 5.5 V – 20°C ≤ Topr ≤ 85°C	17.694	18.432	19.169	MHz
		VCC = 1.8 V to 5.5 V – 40°C ≤ Topr ≤ 85°C	17.510	18.432	19.353	MHz
–	Oscillation stability time		–	5	30	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	530	–	µA

Note:
1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.43 Low-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time		–	–	35	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	2	–	µA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
–	Oscillation stability time		–	–	35	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	2	–	µA

Table 5.44 Power Supply Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on (1)		–	–	2000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

5.2.4 DC Characteristics

Table 5.47 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition			Standard			Unit
						Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P7_0, P7_1, P8 (1)	V_{CC} = 5V	I_{OH} = –20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Other pins	V_{CC} = 5V	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P7_0, P7_1, P8 (1)	V_{CC} = 5V	I_{OL} = 20 mA	–	–	2.0	V
			Other pins	V_{CC} = 5V	I_{OL} = 5 mA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{INT5}$, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO				0.05	0.5	–	V
		$\overline{RESET}$, $\overline{WKUP0}$				0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V			–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V			–	–	–5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5 V			20	40	80	kΩ
R_{fXIN}	Feedback resistance	XIN				–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN				–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode			1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.48 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	–		–	4.7	10	mA
			16 MHz	Off	Off	125 kHz	No division	–		–	3.9	8	mA
			10 MHz	Off	Off	125 kHz	No division	–		–	2.3	–	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	–	3.1	–	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.8	–	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.5	–	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	–		–	1.0	–	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	–		–	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	–		–	2.1	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	110	320	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	63	220	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	60	220	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	46	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.8	33	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	4.6	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	2.4	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.03	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.8	6.4	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2.7	–	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

5.2.5 AC Characteristics

Table 5.53 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	-	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (1)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1t_{CYC} + 20	ns
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

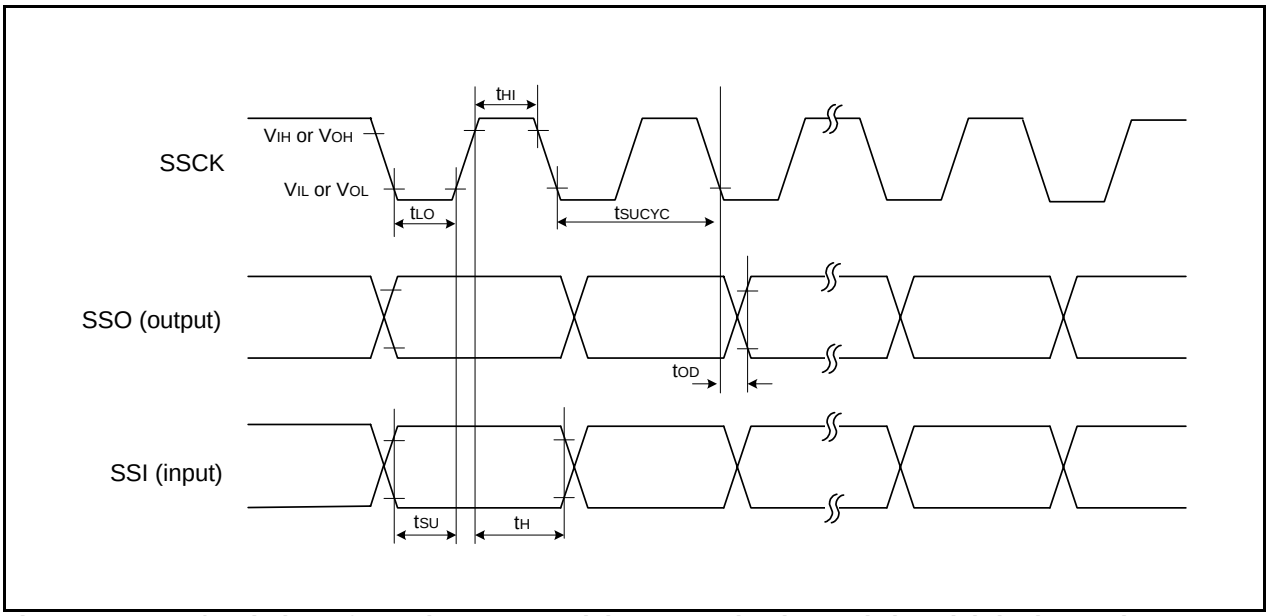
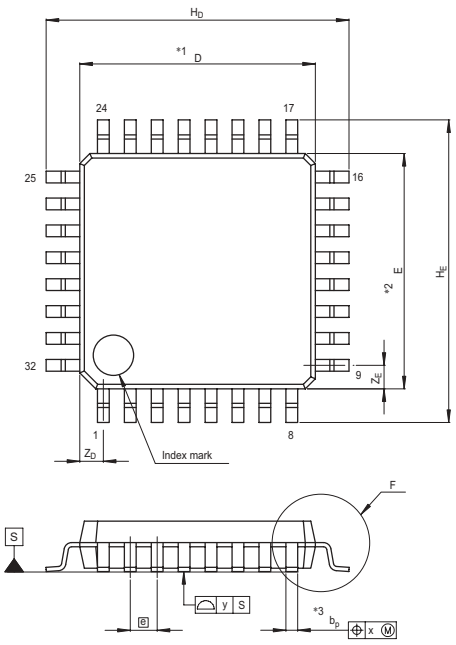


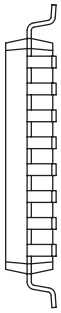
Figure 5.17 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

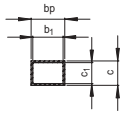
Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

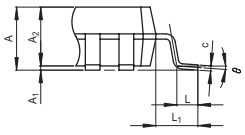
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—