



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

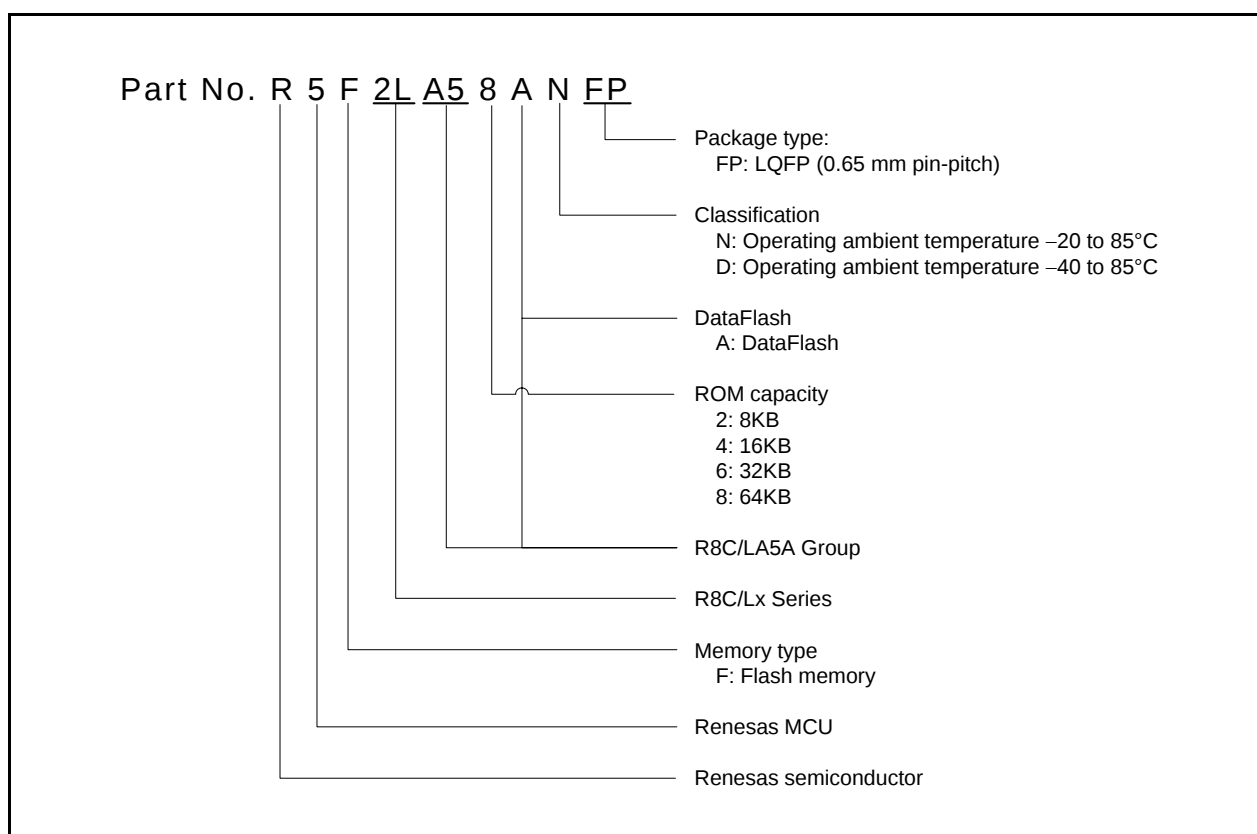
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	3.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la87anfa-u0

Table 1.10 Product List for R8C/LA5A Group**Current of Oct 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA52ANFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	N Version
R5F2LA54ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F2LA56ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F2LA58ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0052JA-A	
R5F2LA52ADFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	D Version
R5F2LA54ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F2LA56ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F2LA58ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0052JA-A	

**Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/LA5A Group**

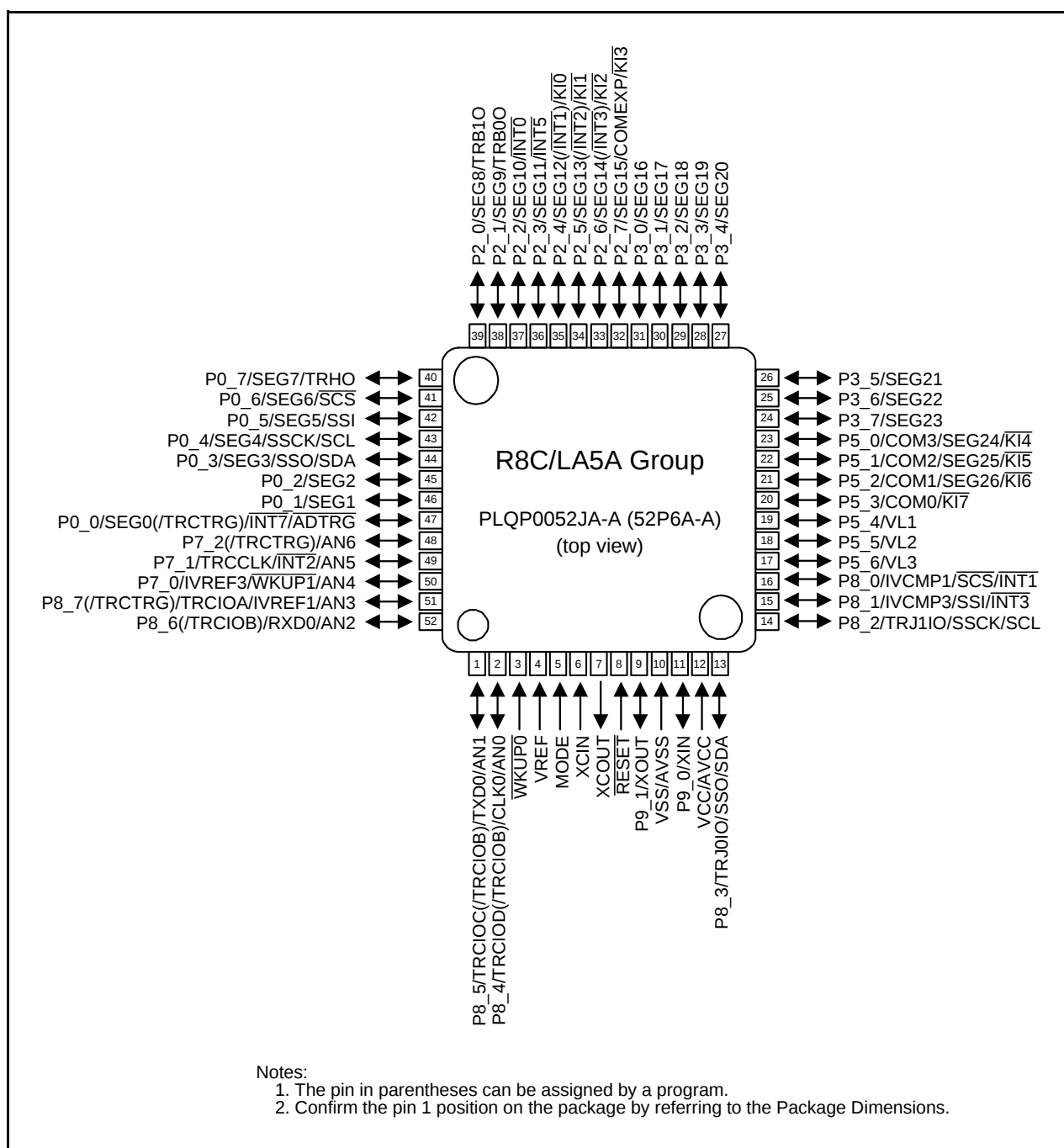


Figure 1.10 Pin Assignment (Top View) of PLQP0052JA-A Package

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.3 SFR Information for R8C/LA5A Group (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.5 SFR Information for R8C/LA5A Group (5) ⁽¹⁾

Address	Register	Symbol	After Reset
0100h			
0101h			
0102h			
0103h			
0104h			
0105h			
0106h			
0107h			
0108h	Timer RB0 Control Register	TRB0CR	00h
0109h	Timer RB0 One-Shot Control Register	TRB0OCR	00h
010Ah	Timer RB0 I/O Control Register	TRB0IOC	00h
010Bh	Timer RB0 Mode Register	TRB0MR	00h
010Ch	Timer RB0 Prescaler Register	TRB0PRE	FFh
010Dh	Timer RB0 Secondary Register	TRB0SC	FFh
010Eh	Timer RB0 Primary Register	TRB0PR	FFh
010Fh			
0110h	Timer RH Second Data Register / Counter Data Register	TRHSEC	XXh 00h ⁽²⁾
0111h	Timer RH Minute Data Register / Compare Data Register	TRHMIN	XXh 00h ⁽²⁾
0112h	Timer RH Hour Data Register	TRHHR	00XXXXXXb 00h ⁽²⁾
0113h	Timer RH Day-of-the-Week Data Register	TRHWK	00000XXXb 00h ⁽²⁾
0114h	Timer RH Date Data Register	TRHDY	00XXXXXXb 00000001b ⁽²⁾
0115h	Timer RH Month Data Register	TRHMON	000XXXXXb 00000001b ⁽²⁾
0116h	Timer RH Year Data Register	TRHYR	XXh 00h ⁽²⁾
0117h	Timer RH Control Register	TRHCR	XX0000Xb 000XX1X0b ⁽²⁾
0118h	Timer RH Count Source Select Register	TRHCSR	X0001000b 0XXXXXXXb ⁽²⁾
0119h	Timer RH Clock Error Correction Register	TRHADJ	XXh 00h ⁽²⁾
011Ah	Timer RH Interrupt Flag Register	TRHIFR	00000XXXb 000XX000b ⁽²⁾
011Bh	Timer RH Interrupt Enable Register	TRHIER	XXh 00h ⁽²⁾
011Ch	Timer RH Alarm Minute Register	TRHAMN	XXh 00h ⁽²⁾
011Dh	Timer RH Alarm Hour Register	TRHAHR	XXh 00h ⁽²⁾
011Eh	Timer RH Alarm Day-of-the-Week Register	TRHAWK	X0000XXXb 00h ⁽²⁾
011Fh	Timer RH Protect Register	TRHPRC	00h X0000000b ⁽²⁾
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.7 SFR Information for R8C/LA5A Group (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RJ Pin Select Register	TRJSR	00h
0181h			
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUICSR	00h
018Dh	Timer RH Second Interrupt Control Register	TRHICR	X0XXXXXXb 00000001b ⁽³⁾
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H ⁽²⁾	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H ⁽²⁾	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	000000X0b
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.
- This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.19 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
FFDFh	ID1		(Note 2)
FFE3h	ID2		(Note 2)
FFEBh	ID3		(Note 2)
FFEFh	ID4		(Note 2)
FFF3h	ID5		(Note 2)
FFF7h	ID6		(Note 2)
FFFBh	ID7		(Note 2)
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5.1.3 Peripheral Function Characteristics

Table 5.3 A/D Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85 °C (N version)/
 -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVcc		—	—	10	Bit
—	Absolute accuracy (2)	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	—	—	±3	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	—	—	±5	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	—	—	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	—	—	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	—	—	±2	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 ≤ Vref = AVcc ≤ 5.5 V (1)		1	—	20	MHz
			3.2 ≤ Vref = AVcc ≤ 5.5 V (1)		1	—	16	MHz
			2.7 ≤ Vref = AVcc ≤ 5.5 V (1)		1	—	10	MHz
			1.8 ≤ Vref = AVcc ≤ 5.5 V (1)		1	—	8	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	ms
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				1.8	—	AVcc	V
VIA	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Temperature Sensor Characteristics
($V_{SS} = 0$ V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless
otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{TMP}	Temperature sensor output voltage	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25 °C	550	600	650	mV
—	Temperature coefficient	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25 °C	—	-2.1	—	mV/°C
—	Start-up time	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	—	200	μ s
I_{TMP}	Operating current	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	100	—	μ A

Table 5.13 High-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8$ V to 5.5 V -20 °C $\leq T_{opr} \leq 85$ °C	19.2	20	20.8	MHz
		$V_{CC} = 1.8$ V to 5.5 V -40 °C $\leq T_{opr} \leq 85$ °C	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽¹⁾	$V_{CC} = 1.8$ V to 5.5 V -20 °C $\leq T_{opr} \leq 85$ °C	17.694	18.432	19.169	MHz
		$V_{CC} = 1.8$ V to 5.5 V -40 °C $\leq T_{opr} \leq 85$ °C	17.510	18.432	19.353	MHz
—	Oscillation stability time		—	5	30	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	530	—	μA

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.14 Low-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	—	35	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	2	—	μA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time		—	—	35	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	2	—	μA

Table 5.15 Power Supply Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = 25$ °C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽¹⁾		—	—	2000	μs

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.16 LCD Drive Control Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/
–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL3	2.2	–	5.5	V
VL2	VL2 voltage		VL1	–	VL3	V
VL1	VL1 voltage		1	–	VL2 (2)	V
f(FR)	Frame frequency		50	–	180	Hz
ILCD	LCD drive control circuit current		–	(1)	–	μA

Notes:

1. Refer to Table 5.19 DC Characteristics (2), Table 5.21 DC Characteristics (4), and Table 5.23 DC Characteristics (6).
2. The VL1 voltage should be VCC or below.

Table 5.17 Power-Off Mode Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/
–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Power-off mode operating supply voltage		1.8	–	5.5	V

Table 5.20 DC Characteristics (3) [2.7 V ≤ V_{CC} < 4.0 V]
(T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage		Port P8 (1)	I _{OH} = −5 mA	V _{CC} − 0.5	−	V _{CC}	V
			Other pins	I _{OH} = −1 mA	V _{CC} − 0.5	−	V _{CC}	V
V _{OL}	Output "L" voltage		Port P8 (1)	I _{OL} = 5 mA	−	−	0.5	V
			Other pins	I _{OL} = 1 mA	−	−	0.5	V
V _{T+} −V _{T−}	Hysteresis	INT0, INT1, INT2, INT3, INT5, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, ADTRG, RXD0, CLK0, SSI, SCL, SDA, SSO			0.05	0.4	−	V
		RESET, WKUP0			0.1	0.8	−	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3 V		−	−	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3 V		−	−	−5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3 V		25	80	140	kΩ
R _{FXIN}	Feedback resistance	XIN			−	2.0	−	MΩ
R _{FXCIN}	Feedback resistance	XCIN			−	14	−	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	−	−	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.23 DC Characteristics (6) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]**($T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)**

Symbol	Parameter		Condition							Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max .	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	8 MHz	Off	Off	125 kHz	No division	—		—	2.1	—	mA
			8 MHz	Off	Off	125 kHz	Divide-by-8	—		—	0.9	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	—		—	1.8	5	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	—		—	1.1	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		—	0.9	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		—	106	300	μA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		—	54	200	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		—	54	200	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	—	36	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	—	9.0	50	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	—	2.5	31	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	—	2.4	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	—	1.7	—	μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25 °C Peripheral clock off	—	0.5	2.2	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off	—	1.2	—	μA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25 °C	—	0.01	0.1	μA
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85 °C	—	0.02	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25 °C	—	1.2	4	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85 °C	—	2	—	μA

Notes:

1. $V_{CC} = 1.8\text{ V to }2.7\text{ V}$, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. $V_{CC} = 2.2\text{ V}$
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

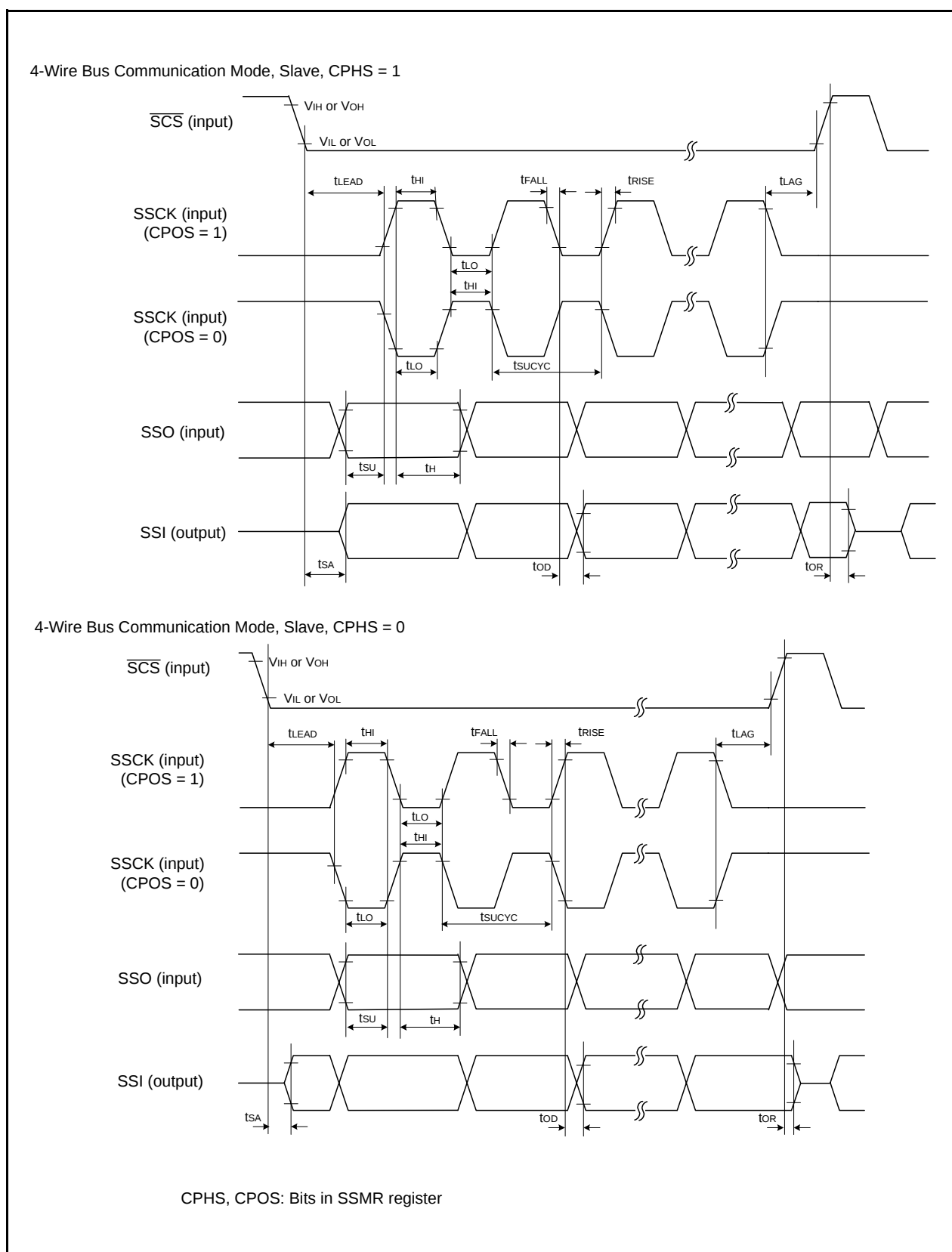


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

5.2 Electrical Characteristics (R8C/LA6A Group and R8C/LA8A Group)

5.2.1 Absolute Maximum Ratings

Table 5.30 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage			–0.3 to 6.5	V
V _I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) ⁽¹⁾	–0.3 to 1.9	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) ⁽¹⁾	–0.3 to V _{CC} + 0.3	V
		P5_4/VL1		–0.3 to VL2 ⁽²⁾	V
		P5_5/VL2		VL1 to VL3	V
		P5_6/VL3		VL2 to 6.5	V
		Other pins		–0.3 to V _{CC} + 0.3	V
V _O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) ⁽¹⁾	–0.3 to 1.9	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) ⁽¹⁾	–0.3 to V _{CC} + 0.3	V
		COM0 to COM3		–0.3 to VL3	V
		SEG0 to SEG39		–0.3 to VL3	V
		Other pins		–0.3 to V _{CC} + 0.3	V
P _d	Power dissipation		–40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature			–20 to 85 (N version)/ –40 to 85 (D version)	°C
T _{stg}	Storage temperature			–65 to 150	°C

Notes:

1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be V_{CC} or below.

5.2.3 Peripheral Function Characteristics

Table 5.32 A/D Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy (2)	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN11 input	—	—	±3	LSB
			Vref = AVCC = 2.2 V	AN0 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 1.8 V	AN0 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 1.8 V	AN0 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 ≤ Vref = AVCC ≤ 5.5 V (1)		1	—	20	MHz
			3.2 ≤ Vref = AVCC ≤ 5.5 V (1)		1	—	16	MHz
			2.7 ≤ Vref = AVCC ≤ 5.5 V (1)		1	—	10	MHz
			1.8 ≤ Vref = AVCC ≤ 5.5 V (1)		1	—	8	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	ms
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5 V, XIN = f1 = φAD = 20 MHz		-	45	—	μA
Vref	Reference voltage				1.8	—	AVCC	V
VIa	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.33 Temperature Sensor Characteristics
($V_{SS} = 0$ V and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{TMP}	Temperature sensor output voltage	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25°C	550	600	650	mV
—	Temperature coefficient	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25°C	—	-2.1	—	mV/ $^{\circ}\text{C}$
—	Start-up time	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	—	200	μs
I_{TMP}	Operating current	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	100	—	μA

Table 5.42 High-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8$ V to 5.5 V $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	19.2	20	20.8	MHz
		$V_{CC} = 1.8$ V to 5.5 V $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽¹⁾	$V_{CC} = 1.8$ V to 5.5 V $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	17.694	18.432	19.169	MHz
		$V_{CC} = 1.8$ V to 5.5 V $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	17.510	18.432	19.353	MHz
—	Oscillation stability time		—	5	30	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	530	—	μA

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.43 Low-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	—	35	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	2	—	μA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time		—	—	35	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	2	—	μA

Table 5.44 Power Supply Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = 25^{\circ}\text{C}$, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on ⁽¹⁾		—	—	2000	μs

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.52 DC Characteristics (6) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max .	
			XIN (2)	XCIN	High-Speed	Low-Speed								
I _{CC}	Power supply current ⁽¹⁾	High-speed clock mode	8 MHz	Off	Off	125 kHz	No division	—			—	2.1	—	mA
			8 MHz	Off	Off	125 kHz	Divide-by-8	—			—	0.9	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	—			—	1.8	5	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	—			—	1.1	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh			—	0.9	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0			—	106	300	μA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	54	200	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	54	200	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	36	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	9.0	50	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	2.5	31	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	LCD drive control circuit ⁽⁴⁾ When external division resistors are used	—	2.4	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode		—	1.7	—	μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{opr} = 25°C Peripheral clock off		—	0.5	2.2	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	T _{opr} = 85°C Peripheral clock off		—	1.2	—	μA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 T _{opr} = 25°C		—	0.01	0.1	μA
			Off	Off	Off	Off	—	—	Power-off 0 T _{opr} = 85°C		—	0.02	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 T _{opr} = 25°C		—	1.2	4	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 T _{opr} = 85°C		—	2	—	μA

Notes:

1. $V_{CC} = 1.8\text{ V to }2.7\text{ V}$, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. $V_{CC} = 2.2\text{ V}$
4. VLCD = V_{CC}, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

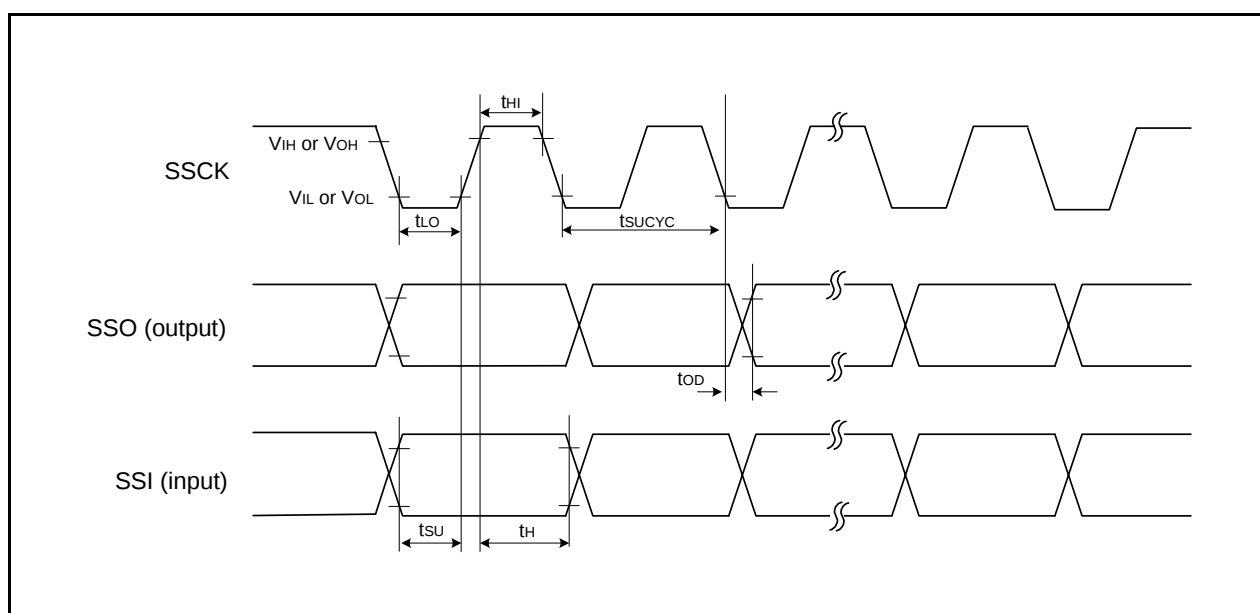


Figure 5.17 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.54 Timing Requirements of I²C bus Interface ⁽¹⁾
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cy} + 600 ⁽¹⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{cy} + 300 ⁽¹⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{cy} + 500 ⁽¹⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{cy} ⁽¹⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cy} ⁽¹⁾	–	–	ns
t _{STAH}	Start condition input hold time		3t _{cy} ⁽¹⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cy} ⁽¹⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{cy} ⁽¹⁾	–	–	ns
t _{SDAS}	Data input setup time		1t _{cy} + 40 ⁽¹⁾	–	–	ns
t _{SDAH}	Data input hold time		10	–	–	ns

Note:

1. 1t_{cy} = 1/f₁(s)

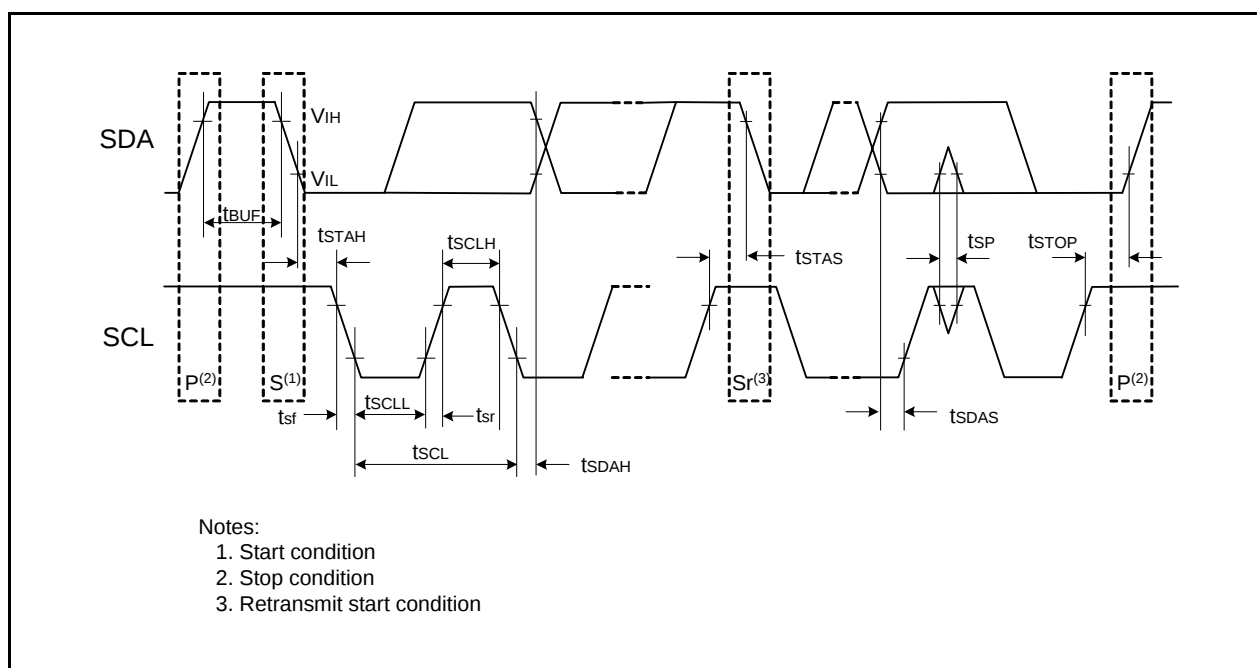


Figure 5.18 I/O Timing of I²C bus Interface

