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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	3.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la87anfp-u0

**Table 1.4 LCD Display Function Pins Provided for Each Group
(R8C/LA3A Group, R8C/LA5A Group)**

Shared I/O Port	R8C/LA3A Group Common output: Max. 4 Segment output: Max. 11								R8C/LA5A Group Common output: Max. 4 Segment output: Max. 27							
P0	—	—	—	—	—	—	—	—	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P2	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P3	—	—	—	—	—	—	—	—	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P5	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1 SEG 26	COM 2 SEG 25	COM 3 SEG 24	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1 SEG 26	COM 2 SEG 25	COM 3 SEG 24

Notes:

1. The symbol “—” indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE0, LSE2, and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

**Table 1.5 LCD Display Function Pins Provided for Each Group
(R8C/LA6A Group, R8C/LA8A Group)**

Shared I/O Port	R8C/LA6A Group Common output: Max. 4 Segment output: Max. 32								R8C/LA8A Group Common output: Max. 4 Segment output: Max. 40							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	—	—	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	—	—	—	—	—	—	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1	COM 2	COM 3	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1	COM 2	COM 3

Notes:

1. The symbol “—” indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE1, LSE4 and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

1.2 Product Lists

Tables 1.9 to 1.12 list product information for each group. Figures 1.1 to 1.4 show the Correspondence of Part No., with Memory Size and Package for each group.

Table 1.9 Product List for R8C/LA3A Group

Current of Oct 2011

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA32ANFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	N Version
R5F2LA34ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	
R5F2LA32ADFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	D Version
R5F2LA34ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	

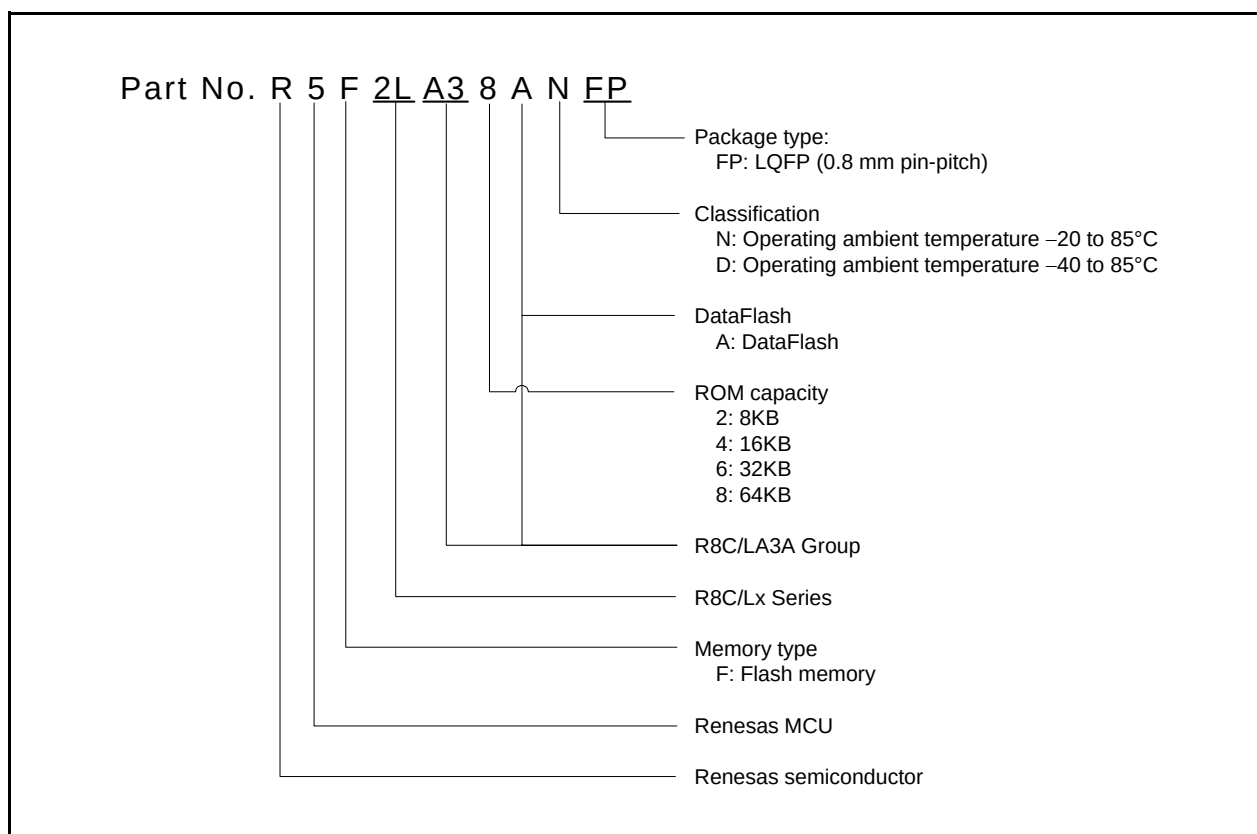


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/LA3A Group

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/LA3A Group. Figure 1.6 shows a Block Diagram of R8C/LA5A Group. Figure 1.7 shows a Block Diagram of R8C/LA6A Group. Figure 1.8 shows a Block Diagram of R8C/LA8A Group.

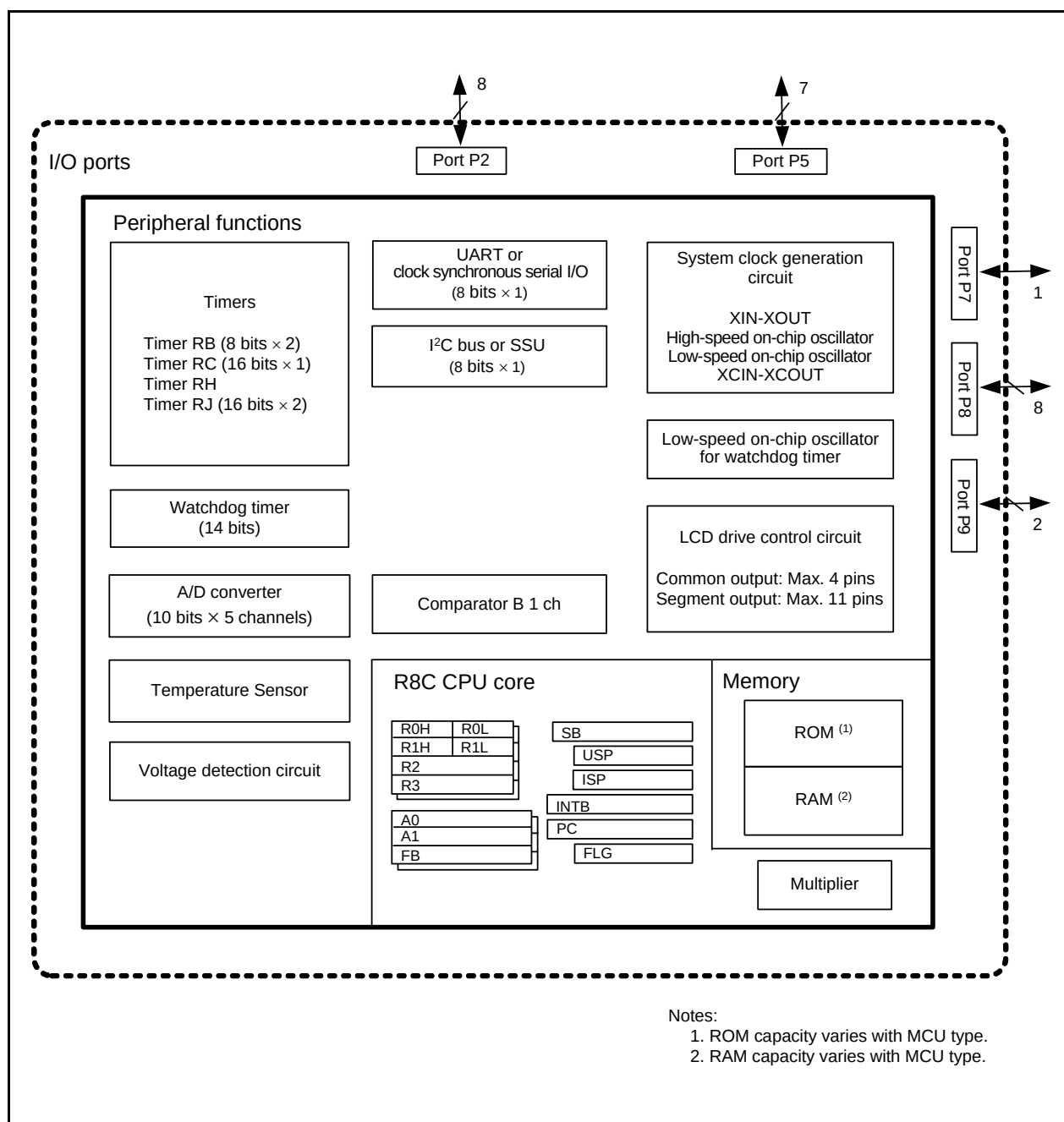


Figure 1.5 Block Diagram of R8C/LA3A Group

Table 1.13 Pin Name Information by Pin Number (R8C/LA3A Group, R8C/LA5A Group)(1)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA5A	LA3A			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, Comparator B	LCD drive Control Circuit
1	30		P8_5		TRCIOC/ (TRCIOB)	TXD0			AN1	
2	31		P8_4		TRCIOD/ (TRCIOB)	CLK0			AN0	
3	32	WKUP0								
4	1	VREF								
5	2	MODE								
6		XCIN								
7		XCOUT								
8	3	RESET								
9	4	XOUT (XCOUT) (2)	P9_1							
10	5	VSS/AVSS								
11	6	XIN (XCIN) (2)	P9_0							
12	7	VCC/AVCC								
13	8		P8_3		TRJ0IO		SSO	SDA		
14	9		P8_2		TRJ1IO		SSCK	SCL		
15	10		P8_1	INT3			SSI		IVCMP3 (3)	
16	11		P8_0	INT1			SCS		IVCMP1	
17	12		P5_6							VL3
18	13		P5_5							VL2
19	14		P5_4							VL1
20	15		P5_3	KI7						COM0
21	16		P5_2	KI6						SEG26/ COM1
22	17		P5_1	KI5						SEG25/ COM2
23	18		P5_0	KI4						SEG24/ COM3
24			P3_7							SEG23
25			P3_6							SEG22
26			P3_5							SEG21
27			P3_4							SEG20
28			P3_3							SEG19
29			P3_2							SEG18
30			P3_1							SEG17

Note:

1. The pin in parentheses can be assigned by a program.
2. Pins (XCOUT) and (XCIN) are not available in the R8C/LA5A Group.
3. The IVCMP3 pin is not available in the R8C/LA3A Group.

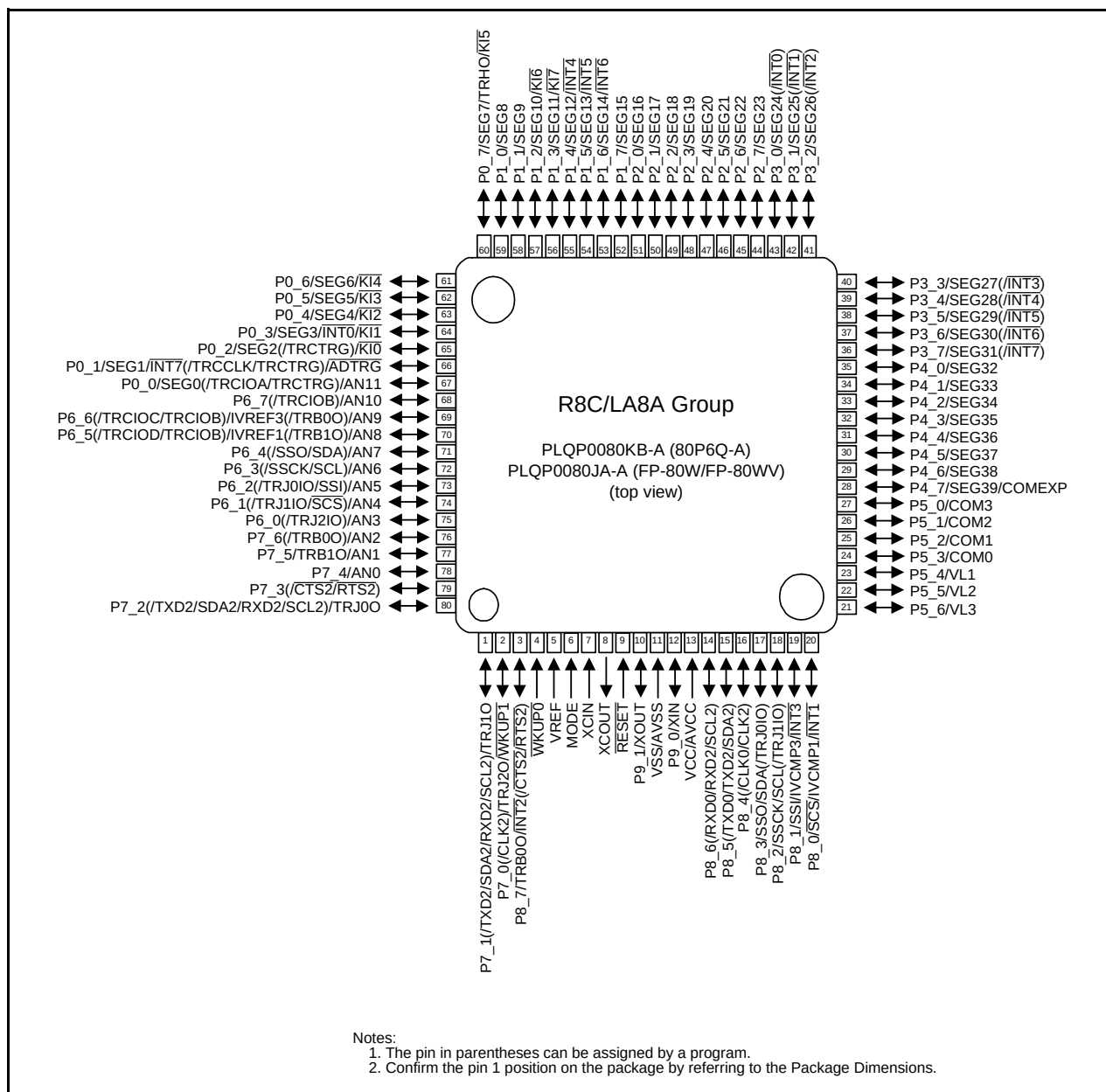


Figure 1.12 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

1.5 Pin Functions

Tables 1.18 and 1.19 list Pin Functions for R8C/LA5A Group, and Tables 1.20 and 1.21 list Pin Functions for R8C/LA8A Group.

Table 1.18 Pin Functions for R8C/LA5A Group (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Power-off 0 mode exit input	WKUP0	I	This pin is provided for input to exit the mode used in power-off 0 mode. Connect to VSS when not using power-off 0 mode.
	$\overline{\text{WKUP1}}$	I	This pin is provided for input to exit the mode used in power-off 0 mode.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. ⁽¹⁾ To use an external clock, input it to the XIN pin and set XOUT as the I/O port P9_1. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOU. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$, $\overline{\text{INT5}}$, $\overline{\text{INT7}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RB	TRB0O, TRB1O	O	Timer RB output pins.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RH	TRHO	O	Timer RH output pin.
Timer RJ	TRJ0IO, TRJ1IO	I/O	Timer RJ I/O pins.
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0	I	Serial data input pin.
	TXD0	O	Serial data output pin.

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.9 list SFR information for R8C/LA5A Group, Tables 4.10 to 4.18 list SFR information for R8C/LA8A Group, and Table 4.19 lists the ID Code Areas and Option Function Select Area. The description offered in this chapter is based on the R8C/LA8A Group.

Table 4.1 SFR Information for R8C/LA5A Group (1) ⁽¹⁾

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h 00000100b ⁽²⁾
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register 0	MSTCR0	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh ⁽³⁾
000Ch	Oscillation Stop Detection Register	OCD	00000100b ⁽⁴⁾ 00h ⁽⁴⁾
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTs	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h	Module Standby Control Register 1	MSTCR1	00h
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽⁵⁾
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	XXXXXX00b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Frequency Control Register 0	FRC0	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator 18 MHz Set Value Register 0	FR18S0	XXh
002Ah	High-Speed On-Chip Oscillator 18 MHz Set Value Register 1	FR18S1	XXh
002Bh			
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Frequency Control Register 1	FRC1	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁶⁾ 00100000b ⁽⁷⁾
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b ⁽⁶⁾ 1100X011b ⁽⁷⁾
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- The CSPRO bit in the CSPR register is set to 1.
- The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
- The reset value differs depending on the mode.
- The CSPROINI bit in the OFS register is set to 0.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.

Table 4.6 SFR Information for R8C/LA5A Group (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.7 SFR Information for R8C/LA5A Group (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RJ Pin Select Register	TRJSR	00h
0181h			
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUICSR	00h
018Dh	Timer RH Second Interrupt Control Register	TRHICR	X0XXXXXXb 00000001b ⁽³⁾
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H ⁽²⁾	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H ⁽²⁾	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	000000X0b
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.
- This is the reset value after reset by RTCRST bit in TRHCR register.

5.1.3 Peripheral Function Characteristics

Table 5.3 A/D Converter Characteristics
($V_{CC}/AV_{CC} = V_{REF} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85 °C (N version)/
 -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVcc		—	—	10	Bit
—	Absolute accuracy (2)	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	—	—	±3	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	—	—	±5	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	—	—	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN6 input	—	—	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN6 input	—	—	±2	LSB
			Vref = AVcc = 1.8 V	AN0 to AN6 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 ≤ Vref = AVcc ≤ 5.5 V (1)		1	—	20	MHz
			3.2 ≤ Vref = AVcc ≤ 5.5 V (1)		1	—	16	MHz
			2.7 ≤ Vref = AVcc ≤ 5.5 V (1)		1	—	10	MHz
			1.8 ≤ Vref = AVcc ≤ 5.5 V (1)		1	—	8	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVcc = 5.0 V, φAD = 20 MHz		2.2	—	—	ms
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				1.8	—	AVcc	V
VIA	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Temperature Sensor Characteristics
($V_{SS} = 0$ V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless
otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{TMP}	Temperature sensor output voltage	$1.8 \text{ V} \leq V_{REF} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25 °C	550	600	650	mV
—	Temperature coefficient	$1.8 \text{ V} \leq V_{REF} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25 °C	—	-2.1	—	mV/°C
—	Start-up time	$1.8 \text{ V} \leq V_{REF} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	—	200	μ s
I_{TMP}	Operating current	$1.8 \text{ V} \leq V_{REF} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	100	—	μ A

Table 5.5 Gain Amplifier Characteristics
(V_{SS} = 0 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V _{GAIN}	Gain amplifier operating range		0.4	—	AV _{CC} – 1.0	V
φ _{AD}	A/D conversion clock		1	—	5	MHz

Table 5.6 Comparator B Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{ref}	IVREF1, IVREF3 input reference voltage		0	—	V _{CC} – 1.4	V
V _I	IVCMP1, IVCMP3 input voltage		–0.3	—	V _{CC} + 0.3	V
—	Offset		—	5	100	mV
t _d	Comparator output delay time ⁽¹⁾	V _I = V _{ref} ± 100 mV	—	—	1	μs
I _{CMP}	Comparator operating current	V _{CC} = 5.0 V	—	12	—	μA

Note:

1. When the digital filter is disabled.

Table 5.23 DC Characteristics (6) [$1.8 \text{ V} \leq V_{CC} < 2.7 \text{ V}$]**($T_{opr} = -20 \text{ to } 85 \text{ }^{\circ}\text{C}$ (N version)/ $-40 \text{ to } 85 \text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)**

Symbol	Parameter		Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max .	
			XIN (2)	XCIN	High-Speed	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	8 MHz	Off	Off	125 kHz	No division	—			—	2.1	—	mA
			8 MHz	Off	Off	125 kHz	Divide-by-8	—			—	0.9	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	—			—	1.8	5	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	—			—	1.1	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh			—	0.9	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0			—	106	300	μA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	54	200	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	54	200	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	36	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	9.0	50	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	2.5	31	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	2.4	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode		—	1.7	—	μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25 °C Peripheral clock off		—	0.5	2.2	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85 °C Peripheral clock off		—	1.2	—	μA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25 °C		—	0.01	0.1	μA
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85 °C		—	0.02	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25 °C		—	1.2	4	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85 °C		—	2	—	μA

Notes:

1. $V_{CC} = 1.8 \text{ V}$ to 2.7 V , single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. $V_{CC} = 2.2 \text{ V}$
4. VLCD = V_{CC}, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG26 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

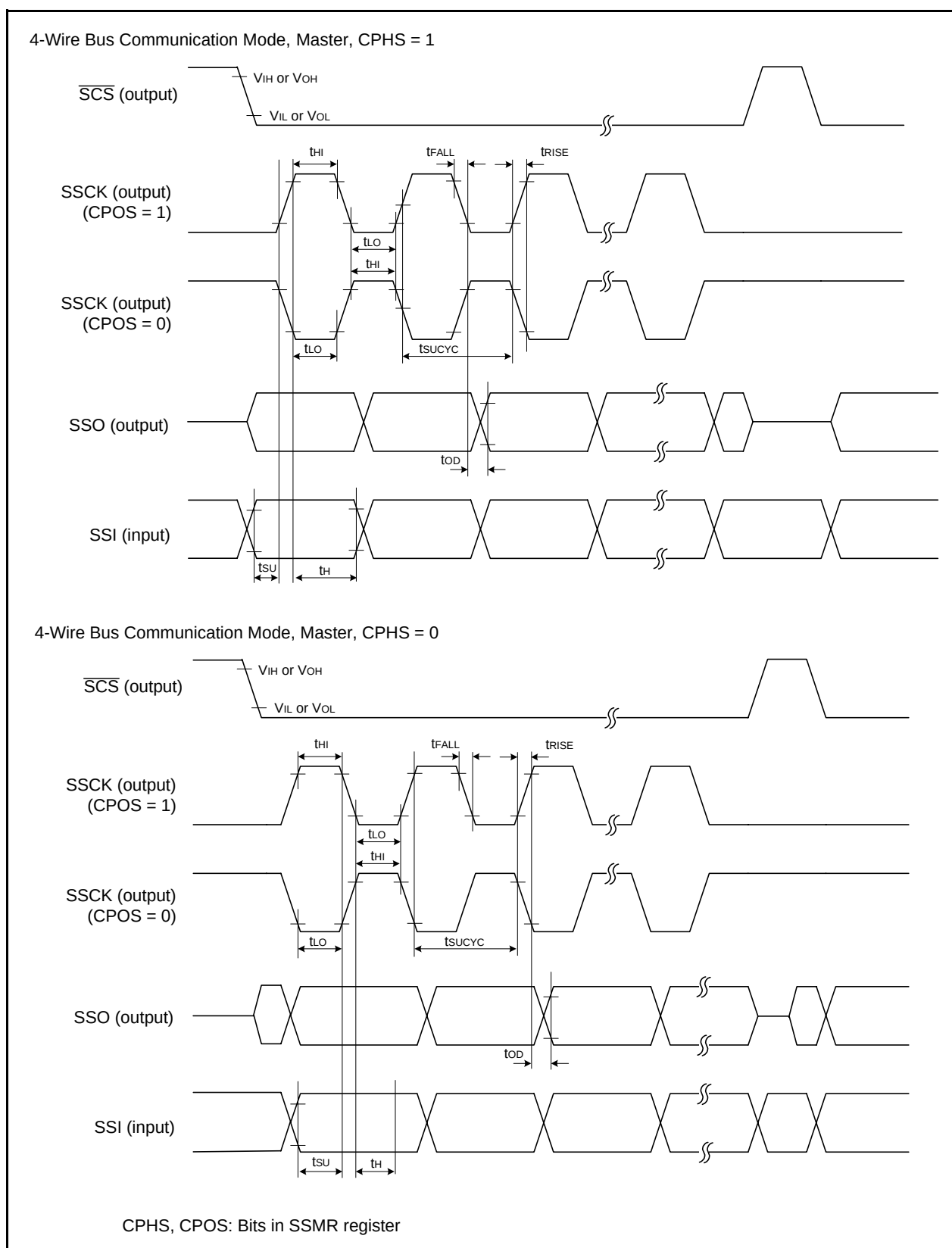


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

Table 5.25 Timing Requirements of I²C bus Interface ⁽¹⁾
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cyC} + 600 ⁽¹⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{cyC} + 300 ⁽¹⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{cyC} + 500 ⁽¹⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{cyC} ⁽¹⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cyC} ⁽¹⁾	–	–	ns
t _{STAH}	Start condition input hold time		3t _{cyC} ⁽¹⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cyC} ⁽¹⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{cyC} ⁽¹⁾	–	–	ns
t _{SDAS}	Data input setup time		1t _{cyC} + 40 ⁽¹⁾	–	–	ns
t _{SDAH}	Data input hold time		10	–	–	ns

Note:

1. 1t_{cyC} = 1/f₁(s)

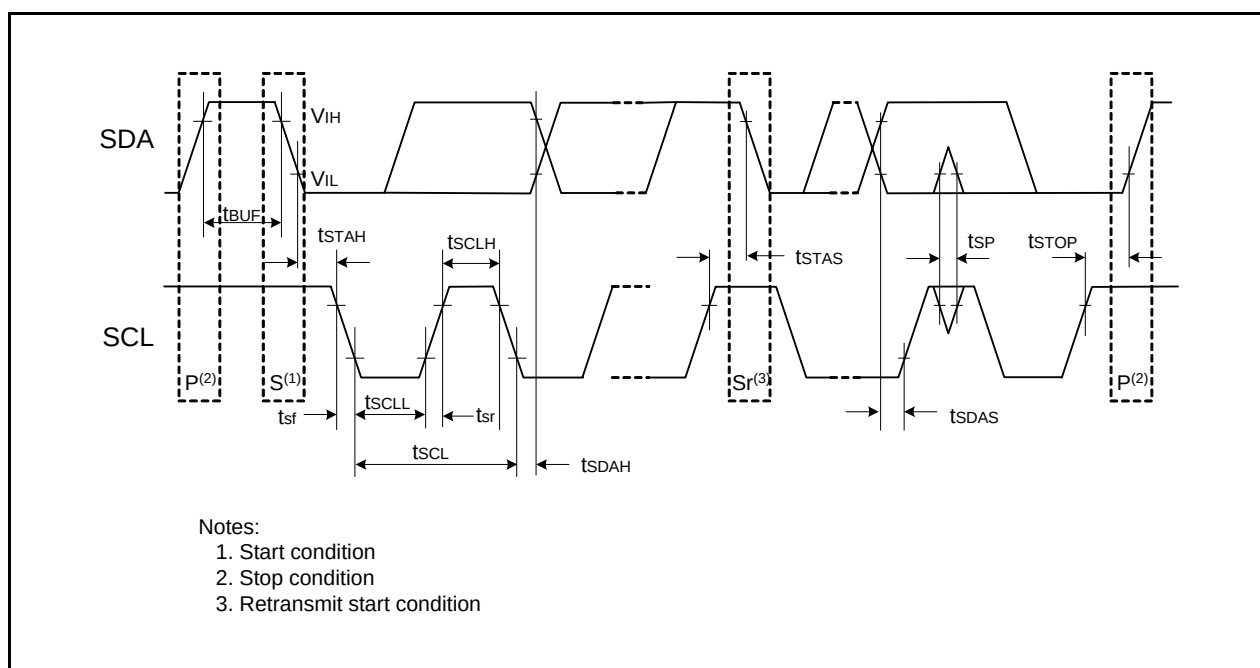


Figure 5.7 I/O Timing of I²C bus Interface

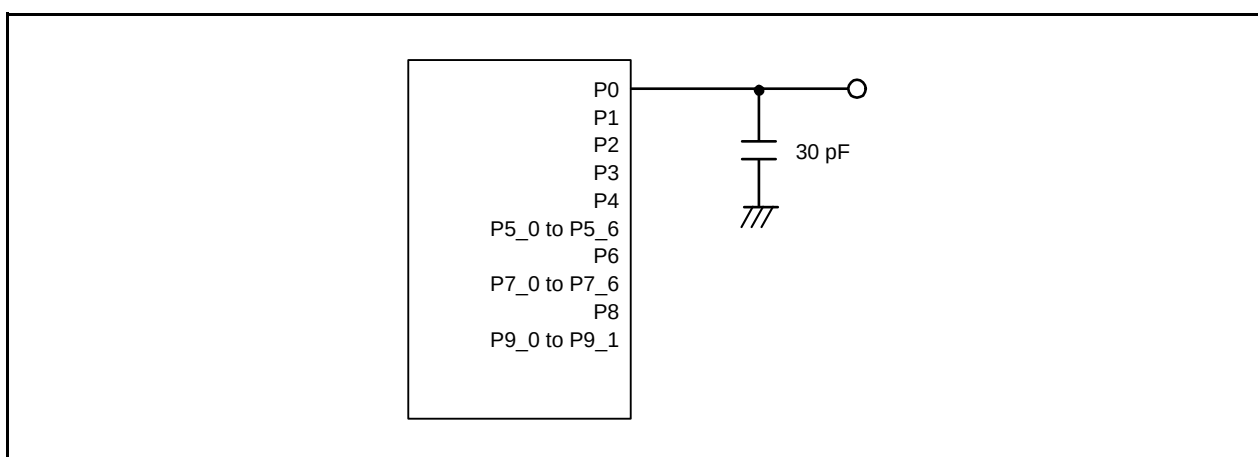


Figure 5.12 Ports P0 to P4, P5_0 to P5_6, P6, P7_0 to P7_6, P8, and P9_0 to P9_1 Timing Measurement Circuit

5.2.3 Peripheral Function Characteristics

Table 5.32 A/D Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy ⁽²⁾	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN11 input	—	—	±3	LSB
			Vref = AVCC = 2.2 V	AN0 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 1.8 V	AN0 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 1.8 V	AN0 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		1	—	20	MHz
			3.2 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		1	—	16	MHz
			2.7 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		1	—	10	MHz
			1.8 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		1	—	8	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	ms
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5 V, XIN = f1 = φAD = 20 MHz		-	45	—	μA
Vref	Reference voltage				1.8	—	AVCC	V
VIa	Analog input voltage ⁽³⁾				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.33 Temperature Sensor Characteristics
($V_{SS} = 0$ V and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{TMP}	Temperature sensor output voltage	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25°C	550	600	650	mV
—	Temperature coefficient	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25°C	—	-2.1	—	mV/ $^{\circ}\text{C}$
—	Start-up time	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	—	200	μs
I_{TMP}	Operating current	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	100	—	μA

Table 5.49 DC Characteristics (3) [$2.7\text{ V} \leq V_{CC} < 4.0\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	Output "H" voltage		Port P7_0, P7_1, P8 (1)	$I_{OH} = -5\text{ mA}$	$V_{CC} - 0.5$	–	V_{CC}
			Other pins	$I_{OH} = -1\text{ mA}$	$V_{CC} - 0.5$	–	V_{CC}
VOL	Output "L" voltage		Port P7_0, P7_1, P8 (1)	$I_{OL} = 5\text{ mA}$	–	–	0.5
			Other pins	$I_{OL} = 1\text{ mA}$	–	–	0.5
VT+–VT–	Hysteresis	INT0, INT1, INT2, INT3, INT4, INT5, INT6, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOA, TRCIOB, TRCIOA, TRCIOB, TRJ0IO, TRJ1IO, TRJ2IO, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	–
		RESET, WKUP0			0.1	0.8	–
I _{IH}	Input "H" current		$V_I = 3\text{ V}$, $V_{CC} = 3\text{ V}$		–	–	5.0
I _{IL}	Input "L" current		$V_I = 0\text{ V}$, $V_{CC} = 3\text{ V}$		–	–	–5.0
R _{PULLUP}	Pull-up resistance		$V_I = 0\text{ V}$, $V_{CC} = 3\text{ V}$		25	80	140
R _{fXIN}	Feedback resistance	XIN			–	2.0	–
R _{fXCIN}	Feedback resistance	XCIN			–	14	–
V _{RAM}	RAM hold voltage		During stop mode		1.8	–	–

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7DPR and P8DPR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.55 Timing Requirements of External Clock Input (XIN, XCIN)
(V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		VCC = 2.2V, Topr = 25°C		VCC = 3V, Topr = 25°C		VCC = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tC(XIN)	XIN input cycle time	200	—	50	—	50	—	ns
tWH(XIN)	XIN input “H” width	90	—	24	—	24	—	ns
tWL(XIN)	XIN input “L” width	90	—	24	—	24	—	ns
tC(XCIN)	XCIN input cycle time	20	—	20	—	20	—	μs
tWH(XCIN)	XCIN input “H” width	10	—	10	—	10	—	μs
tWL(XCIN)	XCIN input “L” width	10	—	10	—	10	—	μs

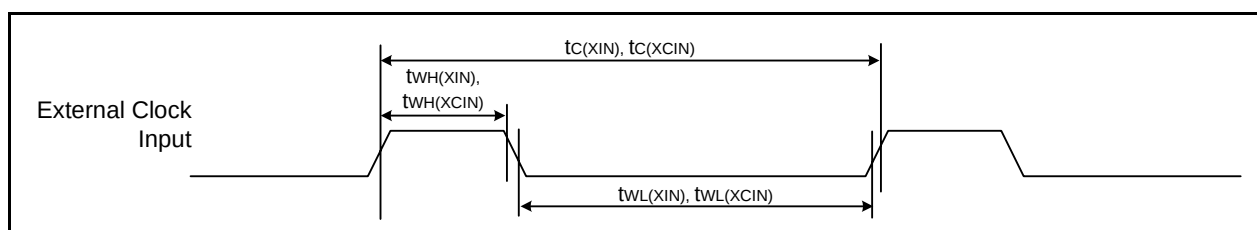


Figure 5.19 External Clock Input Timing

Table 5.56 Timing Requirements of TRJiIO (i = 0 to 2)
(V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (TRJiO)	TRJiO input cycle time	500	—	300	—	100	—	ns
t _{WH} (TRJiO)	TRJiO input “H” width	200	—	120	—	40	—	ns
t _{WL} (TRJiO)	TRJiO input “L” width	200	—	120	—	40	—	ns

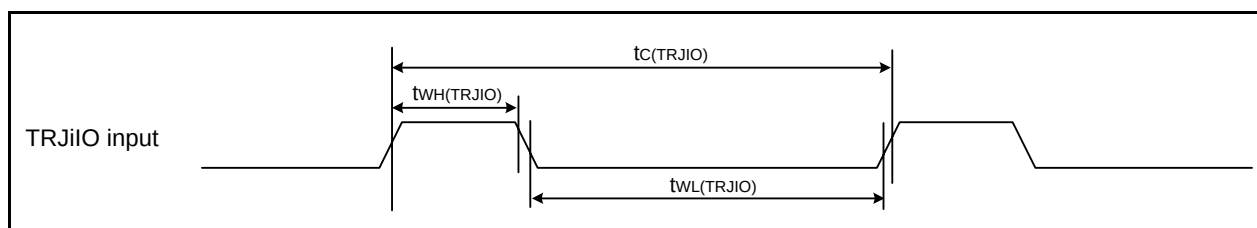


Figure 5.20 Input Timing of TRJiIO

Table 5.57 Timing Requirements of Serial Interface
($V_{SS} = 0\text{ V}$ and $T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (CK)	CLKi input cycle time	800	—	300	—	200	—	ns
t _w (CKH)	CLKi input “H” width	400	—	150	—	100	—	ns
t _w (CKL)	CLKi input “L” width	400	—	150	—	100	—	ns
t _d (C-Q)	TXDi output delay time	—	200	—	80	—	50	ns
t _h (C-Q)	TXDi hold time	0	—	0	—	0	—	ns
t _{su} (D-C)	RXDi input setup time	150	—	70	—	50	—	ns
t _h (C-D)	RXDi input hold time	90	—	90	—	90	—	ns

$i = 0, 2$

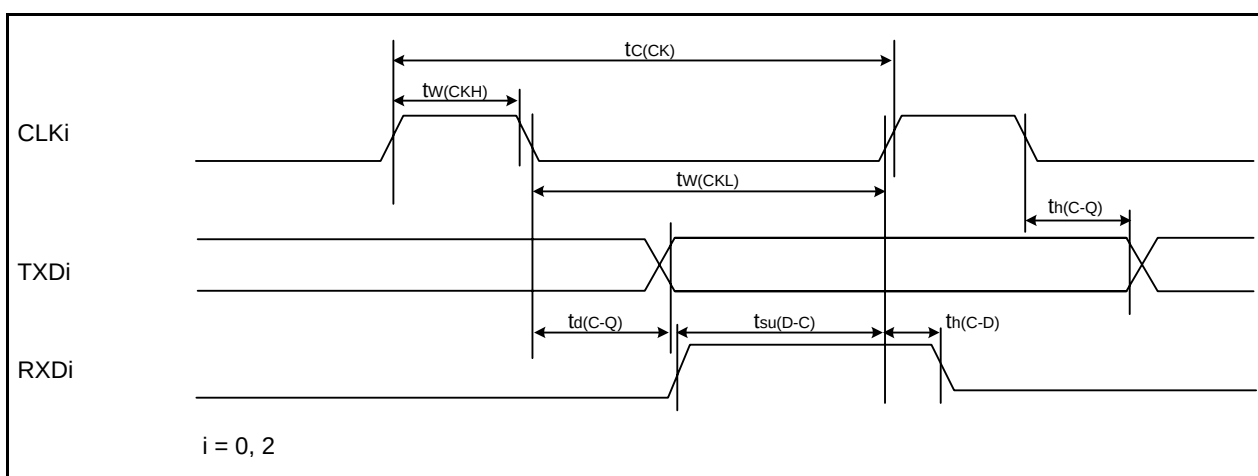


Figure 5.21 Input and Output Timing of Serial Interface

Table 5.58 Timing Requirements of External Interrupt $\overline{\text{INT}}i$ ($i = 0$ to 7) and Key Input Interrupt $\overline{\text{K}}i$ ($i = 0$ to 7)
($V_{SS} = 0\text{ V}$ and $T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tw(INH)	$\overline{\text{INTi}}$ input "H" width, $\overline{\text{Kli}}$ input "H" width	1000 ⁽¹⁾	—	380 ⁽¹⁾	—	250 ⁽¹⁾	—	ns
tw(INL)	$\overline{\text{INTi}}$ input "L" width, $\overline{\text{Kli}}$ input "L" width	1000 ⁽²⁾	—	380 ⁽²⁾	—	250 ⁽²⁾	—	ns

Notes:

- When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

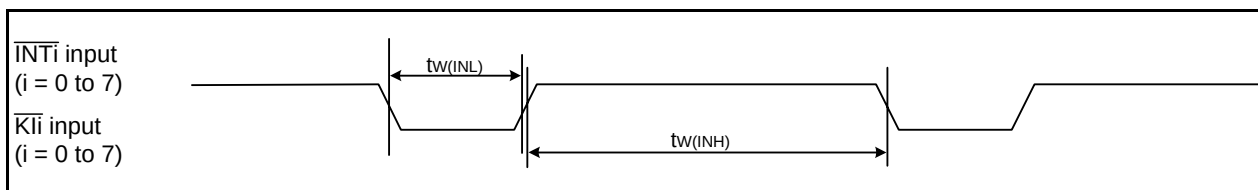


Figure 5.22 Input Timing of External Interrupt $\overline{\text{INT}}i$ and Key Input Interrupt $\overline{\text{K}}i$