Renesas Electronics America Inc - R5F2LA88ADFA#V0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	3.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la88adfa-v0

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Tables 1.2 and 1.3 list the Programmable I/O Ports Provided for Each Group, and Tables 1.4 and 1.5 list the LCD Display Function Pins Provided for Each Group.
Figures 1.9 to 1.12 show the pin assignment for each group, and Tables 1.9 to 1.12 list product information.
The explanations in the chapters which follow apply to the R8C/LA8A Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/LA3A Group	R8C/LA5A Group	R8C/LA6A Group	R8C/LA8A Group
I/O Ports	Programmable I/O ports	26 pins	44 pins	56 pins	72 pins
	High current drive ports	8 pins	8 pins	8 pins	10 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	6 pins	8 pins	8 pins
Timer RJ	Timer RJ0 output pin	None	None	None	1 pin
	Timer RJ1 output pin	None	None	None	1 pin
	Timer RJ2 I/O pin	None	None	None	1 pin
	Timer RJ2 output pin	None	None	None	1 pin
Timer RH	Timer RH output pin	None	1 pin	1 pin	1 pin
Serial interface	UART2	None	None	1 pin	1 pin
A/D Converter	Analog input pins	5 pins	7 pins	8 pins	12 pins
LCD Drive Control Circuit	Segment output pins	Max. 11 pins	Max. 27 pins	Max. 32 pins	Max. 40 pins
Comparator B	Analog input voltage	1 pin	2 pins	2 pins	2 pins
	Reference input voltage	1 pin	2 pins	2 pins	2 pins
Clock	XCIN pin	Shared with XIN pin	Dedicated pin	Dedicated pin	Dedicated pin
	XCOUT pin	Shared with XOUT pin	Dedicated pin	Dedicated pin	Dedicated pin
Packages		32-pin LQFP	52-pin LQFP	64-pin LQFP	80-pin LQFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
   Refer to Tables 1.13 to 1.17, Pin Name Information by Pin Number, for details.

Table 1.4 LCD Display Function Pins Provided for Each Group (R8C/LA3A Group, R8C/LA5A Group)

Shared I/O Port	R8C/LA3A Group Common output: Max. 4 Segment output: Max. 11								R8C/LA5A Group Common output: Max. 4 Segment output: Max. 27							
P0	—	—	—	—	—	—	—	—	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P2	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P3	—	—	—	—	—	—	—	—	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P5	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1 SEG 26	COM 2 SEG 25	COM 3 SEG 24	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1 SEG 26	COM 2 SEG 25	COM 3 SEG 24

Notes:
1. The symbol "—" indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE0, LSE2, and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

Table 1.5 LCD Display Function Pins Provided for Each Group (R8C/LA6A Group, R8C/LA8A Group)

Shared I/O Port	R8C/LA6A Group Common output: Max. 4 Segment output: Max. 32								R8C/LA8A Group Common output: Max. 4 Segment output: Max. 40							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	—	—	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	—	—	—	—	—	—	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1	COM 2	COM 3	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1	COM 2	COM 3

Notes:
1. The symbol "—" indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE1, LSE4 and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

1.1.3 Specifications

Tables 1.6 to 1.8 list the specifications.

Table 1.6 Specifications (1)

Item	Function		Specification
CPU	Central processing unit		R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V) 125 ns (f(XIN) = 8 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM/RAM Data flash		Refer to Tables 1.9 to 1.12 Product Lists.
Power Supply Voltage Detection	Voltage detection circuit		• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	R8C/LA3A Group	• CMOS I/O ports: 26, selectable pull-up resistor (1) • High current drive ports: 8
		R8C/LA5A Group	• CMOS I/O ports: 44, selectable pull-up resistor (1) • High current drive ports: 8
		R8C/LA6A Group	• CMOS I/O ports: 56, selectable pull-up resistor (1) • High current drive ports: 8
		R8C/LA8A Group	• CMOS I/O ports: 72, selectable pull-up resistor (1) • High current drive ports: 10
Clock	Clock generation circuits		4 circuits: XIN clock oscillation circuit XCIN clock oscillation circuit (32 kHz) High-speed on-chip oscillator (with frequency adjustment function) Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Division ratio selectable from 1, 2, 4, 8, and 16 • Low-power-consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode
			Real-time clock (timer RH)
Interrupts		R8C/LA3A Group	• Number of interrupt vectors: 69 • External Interrupt: 13 ($\overline{\text{INT}}$ × 5, key input × 8) • Priority levels: 7 levels
		R8C/LA5A Group	• Number of interrupt vectors: 69 • External Interrupt: 14 ($\overline{\text{INT}}$ × 6, key input × 8) • Priority levels: 7 levels
		R8C/LA6A Group	• Number of interrupt vectors: 69 • External Interrupt: 16 ($\overline{\text{INT}}$ × 8, key input × 8) • Priority levels: 7 levels
		R8C/LA8A Group	
Watchdog Timer			• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for watchdog timer

Note:
1. No pull-up resistor is provided in the pins P5_4 to P5_6.

Table 1.15 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(1)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, Comparator B	LCD drive Control Circuit
1			P7_1		TRJ1O	(TXD2/SDA2/RXD2/SCL2)				
2		$\overline{\text{WKUP1}}$	P7_0		TRJ2O	(CLK2)				
3	64		P8_7	$\overline{\text{INT2}}$	TRB0O	($\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$)				
4	1	$\overline{\text{WKUP0}}$								
5	2	VREF								
6	3	MODE								
7	4	XCIN								
8	5	XCOUT								
9	6	$\overline{\text{RESET}}$								
10	7	XOUT	P9_1							
11	8	VSS/ AVSS								
12	9	XIN	P9_0							
13	10	VCC/ AVCC								
14	11		P8_6			(RXD0/RXD2/SCL2)				
15	12		P8_5			(TXD0/TXD2/SDA2)				
16	13		P8_4			(CLK0/CLK2)				
17	14		P8_3		(TRJ0IO)		SSO	SDA		
18	15		P8_2		(TRJ1IO)		SSCK	SCL		
19	16		P8_1	$\overline{\text{INT3}}$			SSI		IVCMP3	
20	17		P8_0	$\overline{\text{INT1}}$			$\overline{\text{SCS}}$		IVCMP1	
21	18		P5_6							VL3
22	19		P5_5							VL2
23	20		P5_4							VL1
24	21		P5_3							COM0
25	22		P5_2							COM1
26	23		P5_1							COM2
27	24		P5_0							COM3
28	25		P4_7							SEG39/ COMEXP
29	26		P4_6							SEG38
30			P4_5							SEG37

Note:
1. The pin in parentheses can be assigned by a program.

Table 1.16 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(2)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, Comparator B	LCD drive Control Circuit
31			P4_4							SEG36
32			P4_3							SEG35
33			P4_2							SEG34
34			P4_1							SEG33
35			P4_0							SEG32
36	27		P3_7	($\overline{\text{INT7}}$)						SEG31
37	28		P3_6	($\overline{\text{INT6}}$)						SEG30
38	29		P3_5	($\overline{\text{INT5}}$)						SEG29
39	30		P3_4	($\overline{\text{INT4}}$)						SEG28
40	31		P3_3	($\overline{\text{INT3}}$)						SEG27
41	32		P3_2	($\overline{\text{INT2}}$)						SEG26
42	33		P3_1	($\overline{\text{INT1}}$)						SEG25
43	34		P3_0	($\overline{\text{INT0}}$)						SEG24
44	35		P2_7							SEG23
45	36		P2_6							SEG22
46	37		P2_5							SEG21
47	38		P2_4							SEG20
48	39		P2_3							SEG19
49	40		P2_2							SEG18
50	41		P2_1							SEG17
51	42		P2_0							SEG16
52	43		P1_7							SEG15
53	44		P1_6	$\overline{\text{INT6}}$						SEG14
54	45		P1_5	$\overline{\text{INT5}}$						SEG13
55	46		P1_4	$\overline{\text{INT4}}$						SEG12
56	47		P1_3	$\overline{\text{KI7}}$						SEG11
57	48		P1_2	$\overline{\text{KI6}}$						SEG10
58			P1_1							SEG9
59			P1_0							SEG8
60	49		P0_7	$\overline{\text{KI5}}$	TRHO					SEG7
61	50		P0_6	$\overline{\text{KI4}}$						SEG6
62	51		P0_5	$\overline{\text{KI3}}$						SEG5
63	52		P0_4	$\overline{\text{KI2}}$						SEG4
64	53		P0_3	$\overline{\text{KI1}}$/ $\overline{\text{INT0}}$						SEG3
65	54		P0_2	$\overline{\text{KI0}}$	(TRCTRG)					SEG2
66	55		P0_1	$\overline{\text{INT7}}$	(TRCTRG/ TRCCLK)				$\overline{\text{ADTRG}}$	SEG1
67	56		P0_0		(TRCIOA/ TRCTRG)				AN11	SEG0
68	57		P6_7		(TRCIOB)				AN10	

Note:
1. The pin in parentheses can be assigned by a program.

Table 1.17 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(3)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, Comparator B	LCD drive Control Circuit
69	58		P6_6		(TRB0O/ TRCIOB/ TRCIOC)				AN9/IVREF3	
70	59		P6_5		(TRB1O/ TRCIOB/ TRCIOD)				AN8/IVREF1	
71	60		P6_4				(SSO)	(SDA)	AN7	
72	61		P6_3				(SSCK)	(SCL)	AN6	
73	62		P6_2		(TRJ0IO)		(SSI)		AN5	
74	63		P6_1		(TRJ1IO)		($\overline{SCS}$)		AN4	
75			P6_0		(TRJ2IO)				AN3	
76			P7_6		(TRB0O)				AN2	
77			P7_5		TRB1O				AN1	
78			P7_4						AN0	
79			P7_3			($\overline{CTS2}$/$\overline{RTS2}$)				
80			P7_2		TRJ0O	(RXD2/SCL2/ TXD2/SDA2)				

Note:
1. The pin in parentheses can be assigned by a program.

Table 4.2 SFR Information for R8C/LA5A Group (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h	INT7 Interrupt Control Register	INT7IC	XX00X000b
0044h			
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RH Interrupt Control Register	TRHIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RJ0 Interrupt Control Register	TRJ0IC	XXXXX000b
0057h	Timer RB1 Interrupt Control Register	TRB1IC	XXXXX000b
0058h	Timer RB0 Interrupt Control Register	TRB0IC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RJ1 Interrupt Control Register	TRJ1IC	XXXXX000b
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	LCD Interrupt Control Register	LCDIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.7 SFR Information for R8C/LA5A Group (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RJ Pin Select Register	TRJSR	00h
0181h			
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh	Timer RH Second Interrupt Control Register	TRHICR	X0XXXXXXb 00000001b (3)
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	000000X0b
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.12 SFR Information for R8C/LA8A Group (3) (1)

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h	Timer RJ2 Control Register	TRJ2CR	00h
0091h	Timer RJ2 I/O Control Register	TRJ2IOC	00h
0092h	Timer RJ2 Mode Register	TRJ2MR	00h
0093h	Timer RJ2 Event Pin Select Register	TRJ2ISR	00h
0094h	Timer RJ2 Register	TRJ2	FFh
0095h			FFh
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.14 SFR Information for R8C/LA8A Group (5) (1)

Address	Register	Symbol	After Reset
0100h			
0101h			
0102h			
0103h			
0104h			
0105h			
0106h			
0107h			
0108h	Timer RB0 Control Register	TRB0CR	00h
0109h	Timer RB0 One-Shot Control Register	TRB0OCR	00h
010Ah	Timer RB0 I/O Control Register	TRB0IOC	00h
010Bh	Timer RB0 Mode Register	TRB0MR	00h
010Ch	Timer RB0 Prescaler Register	TRB0PRE	FFh
010Dh	Timer RB0 Secondary Register	TRB0SC	FFh
010Eh	Timer RB0 Primary Register	TRB0PR	FFh
010Fh			
0110h	Timer RH Second Data Register / Counter Data Register	TRHSEC	XXh 00h (2)
0111h	Timer RH Minute Data Register / Compare Data Register	TRHMIN	XXh 00h (2)
0112h	Timer RH Hour Data Register	TRHHR	00XXXXXXb 00h (2)
0113h	Timer RH Day-of-the-Week Data Register	TRHWK	00000XXXb 00h (2)
0114h	Timer RH Date Data Register	TRHDY	00XXXXXXb 00000001b (2)
0115h	Timer RH Month Data Register	TRHMON	000XXXXXb 00000001b (2)
0116h	Timer RH Year Data Register	TRHYR	XXh 00h (2)
0117h	Timer RH Control Register	TRHCR	XXX00X0Xb 000XX1X0b (2)
0118h	Timer RH Count Source Select Register	TRHCSR	X0001000b 0XXXXXXXb (2)
0119h	Timer RH Clock Error Correction Register	TRHADJ	XXh 00h (2)
011Ah	Timer RH Interrupt Flag Register	TRHIFR	00000XXXb 000XX000b (2)
011Bh	Timer RH Interrupt Enable Register	TRHIER	XXh 00h (2)
011Ch	Timer RH Alarm Minute Register	TRHAMN	XXh 00h (2)
011Dh	Timer RH Alarm Hour Register	TRHAHR	XXh 00h (2)
011Eh	Timer RH Alarm Day-of-the-Week Register	TRHAWK	X0000XXXb 00h (2)
011Fh	Timer RH Protect Register	TRHPRC	00h X0000000b (2)
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. This is the reset value after reset by RTCRST bit in TRHCR register.

Table 5.7 Flash Memory (Program ROM) Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time		–	80	–	µs
–	Block erase time		–	0.12	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time (6)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.8 Flash Memory (Data flash Block A and Block B) Characteristics (V_{CC} = 1.8 to 5.5 V and T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time (program/erase endurance ≤ 10,000 times)		–	150	–	µs
–	Block erase time (program/erase endurance ≤ 10,000 times)		–	0.05	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		−20 (6)	–	85	°C
–	Data hold time (7)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. −40 °C for D version.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

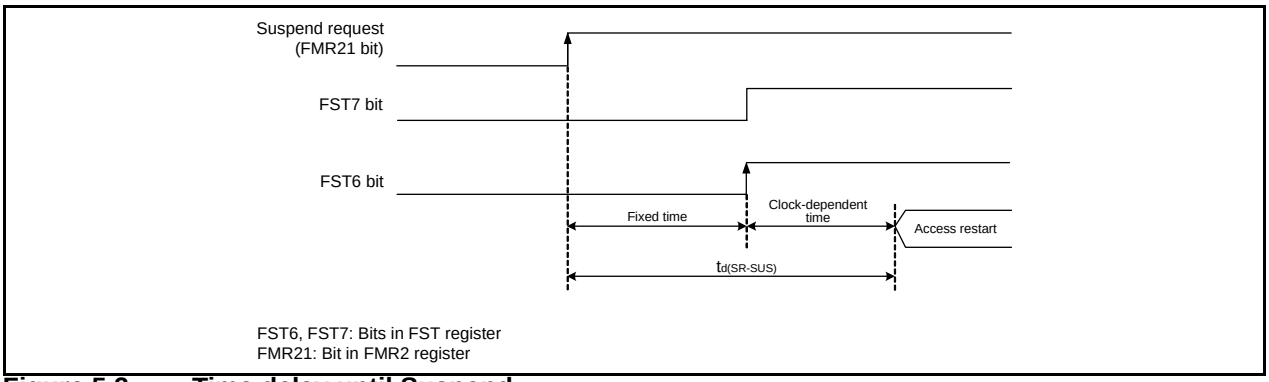

Figure 5.2 Time delay until Suspend

Table 5.20 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P8 (1)	I_{OH} = –5 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P8 (1)	I_{OL} = 5 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT5}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, $\overline{ADTRG}$, RXD0, CLK0, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V		–	–	–5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V		25	80	140	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.28 Timing Requirements of Serial Interface
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	800	–	300	–	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	400	–	150	–	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	400	–	150	–	100	–	ns
$t_{d(C-Q)}$	TXD0 output delay time	–	200	–	80	–	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	–	0	–	0	–	ns
$t_{su(D-C)}$	RXD0 input setup time	150	–	70	–	50	–	ns
$t_{h(C-D)}$	RXD0 input hold time	90	–	90	–	90	–	ns

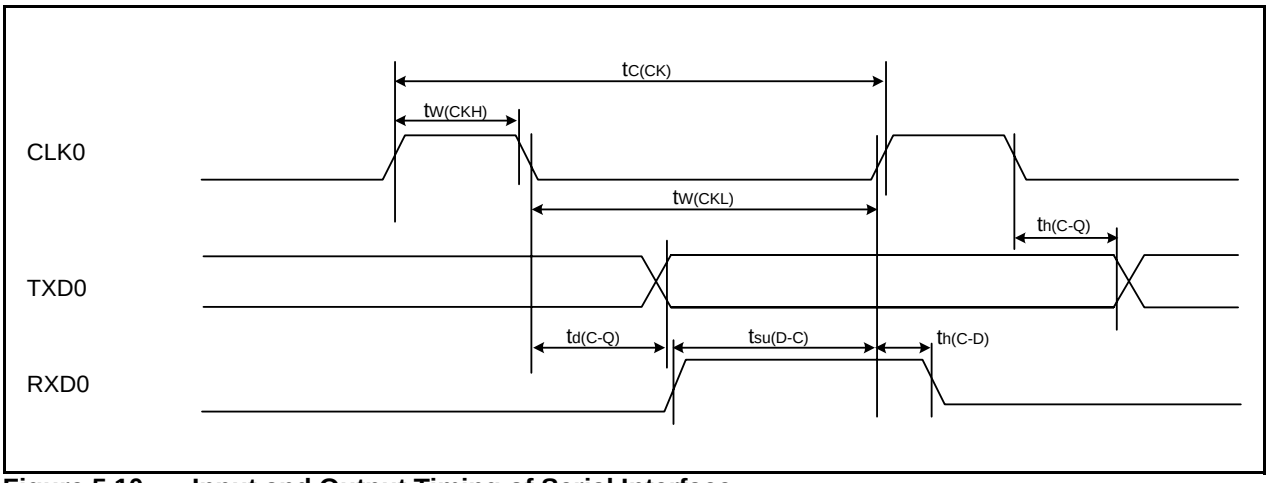

Figure 5.10 Input and Output Timing of Serial Interface

Table 5.29 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 3, 5, 7) and Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)
(Vss = 0 V and Topr = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	–	380 (1)	–	250 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	–	380 (2)	–	250 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

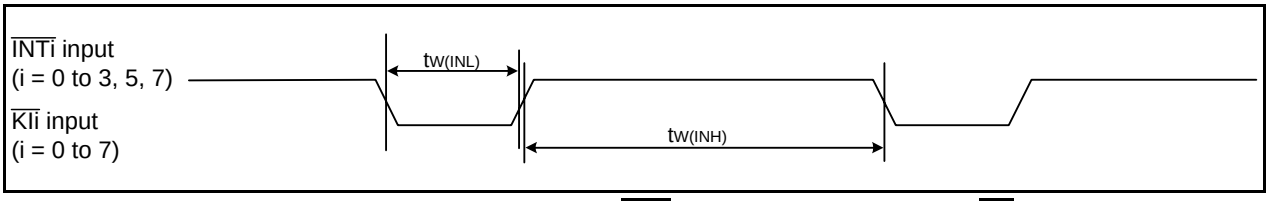

Figure 5.11 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$

Table 5.37 Flash Memory (Data flash Block A and Block B) Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (1)		10,000 (2)	–	–	times
–	Byte program time (program/erase endurance ≤ 10,000 times)		–	150	–	µs
–	Block erase time (program/erase endurance ≤ 10,000 times)	Internal ROM Capacity: 1 KB × 2	–	0.05	1	s
		Internal ROM Capacity: 2 KB × 2	–	0.055	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		–20 (6)	–	85	°C
–	Data hold time (7)	Ambient temperature = 85 °C	10	–	–	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. –40°C for D version.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

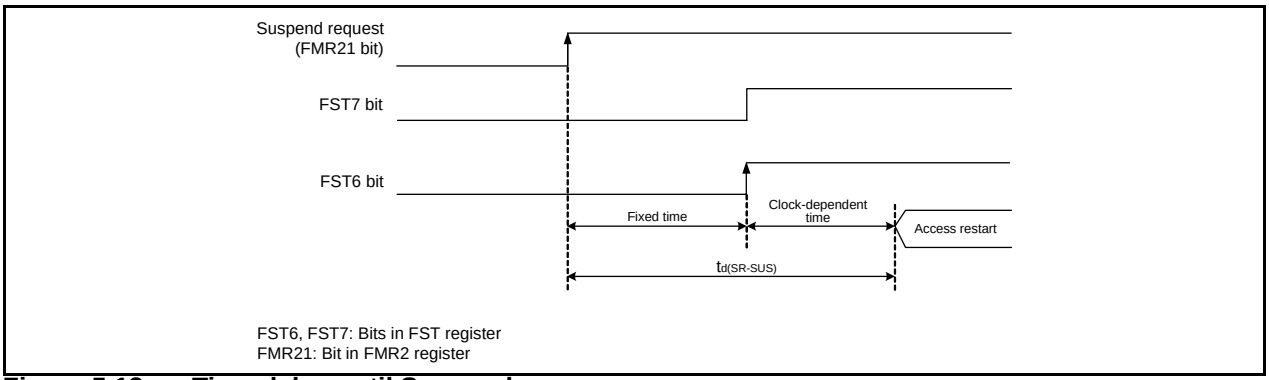

Figure 5.13 Time delay until Suspend

Table 5.38 Voltage Detection 0 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)			1.8	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)			2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)			2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)			3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (3)	In operation	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	50	500	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	–	100	500	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V		–	1.5	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.39 Voltage Detection 1 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	At the falling of Vcc		2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	At the falling of Vcc		2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	At the falling of Vcc		2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	At the falling of Vcc		2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	At the falling of Vcc		2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	At the falling of Vcc		2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	At the falling of Vcc		2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	At the falling of Vcc		3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	At the falling of Vcc		3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	At the falling of Vcc		3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	At the falling of Vcc		3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	At the falling of Vcc		3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	At the falling of Vcc		3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	At the falling of Vcc		3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	At the falling of Vcc		4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	At the falling of Vcc		4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected		–	0.07	–	V
		Vdet1_6 to Vdet1_F selected		–	0.10	–	V
–	Voltage detection 1 circuit response time (2)	In operation	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	60	150	µs
		In stop mode	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	–	250	500	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V		–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)			–	–	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.49 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P7_0, P7_1, P8 (1)	I_{OH} = –5 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P7_0, P7_1, P8 (1)	I_{OL} = 5 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V		–	–	–5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V		25	80	140	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.51 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		Port P7_0, P7_1, P8 (1)	I_{OH} = –2 mA	V_{CC} – 0.5	–	V_{CC}	V
			Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		Port P7_0, P7_1, P8 (1)	I_{OL} = 2 mA	–	–	0.5	V
			Other pins	I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	–	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	0.8	–	V
I_{IH}	Input “H” current		VI = 1.8 V, V_{CC} = 1.8 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 1.8 V		–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 1.8 V		85	220	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	2.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	14	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.52 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	8 MHz	Off	Off	125 kHz	No division	–		–	2.1	–	mA
			8 MHz	Off	Off	125 kHz	Divide-by-8	–		–	0.9	–	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz	125 kHz	No division	–		–	1.8	5	mA
			Off	Off	5 MHz	125 kHz	Divide-by-8	–		–	1.1	–	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		–	0.9	–	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		–	106	300	µA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		–	54	200	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		–	54	200	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	–	36	–	µA
		Wait mode	Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	–	9.0	50	µA
			Off	Off	Off	125 kHz	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	–	2.5	31	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode LCD drive control circuit (4) When external division resistors are used	–	2.4	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	–	1.7	–	µA
		Stop mode	Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	–	0.5	2.2	µA
			Off	Off	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	–	1.2	–	µA
		Power-off mode	Off	Off	Off	Off	–	–	Power-off 0 Topr = 25°C	–	0.01	0.1	µA
			Off	Off	Off	Off	–	–	Power-off 0 Topr = 85°C	–	0.02	–	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	–	1.2	4	µA
			Off	32 kHz	Off	Off	–	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	–	2	–	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 2.2 V
4. VLCD = Vcc, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open.The standard value does not include the current that flows through external division resistors.

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