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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la8aadfp-30

Table 1.2 Programmable I/O Ports Provided for Each Group (R8C/LA3A Group, R8C/LA5A Group)

Programmable I/O Port	R8C/LA3A Group Total: 26 I/O pins								R8C/LA5A Group Total: 44 I/O pins							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	✓	—	—	—	—	—	—	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:

1. The symbol “✓” indicates a programmable I/O port.
2. The symbol “—” indicates the settings should be made as follows:
 - Set 0 to the corresponding bits in the PDi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the Pi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.

Table 1.3 Programmable I/O Ports Provided for Each Group (R8C/LA6A Group, R8C/LA8A Group)

Programmable I/O Port	R8C/LA6A Group Total: 56 I/O pins								R8C/LA8A Group Total: 72 I/O pins							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P1	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P4	✓	✓	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P6	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:

1. The symbol “✓” indicates a programmable I/O port.
2. The symbol “—” indicates the settings should be made as follows:
 - Set 0 to the corresponding bits in the PDi (i = 1, 4 to 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the Pi (i = 1, 4 to 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the P7DRR register. When read, the content is 0.

**Table 1.4 LCD Display Function Pins Provided for Each Group
(R8C/LA3A Group, R8C/LA5A Group)**

Shared I/O Port	R8C/LA3A Group Common output: Max. 4 Segment output: Max. 11								R8C/LA5A Group Common output: Max. 4 Segment output: Max. 27							
P0	—	—	—	—	—	—	—	—	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P2	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P3	—	—	—	—	—	—	—	—	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P5	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1 SEG 26	COM 2 SEG 25	COM 3 SEG 24	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1 SEG 26	COM 2 SEG 25	COM 3 SEG 24

Notes:

1. The symbol “—” indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE0, LSE2, and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

**Table 1.5 LCD Display Function Pins Provided for Each Group
(R8C/LA6A Group, R8C/LA8A Group)**

Shared I/O Port	R8C/LA6A Group Common output: Max. 4 Segment output: Max. 32								R8C/LA8A Group Common output: Max. 4 Segment output: Max. 40							
P0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0
P1	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	—	—	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8
P2	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
P3	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
P4	SEG 39	SEG 38	—	—	—	—	—	—	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
P5	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1	COM 2	COM 3	—	VL3 (2)	VL2 (2)	VL1 (2)	COM 0	COM 1	COM 2	COM 3

Notes:

1. The symbol “—” indicates there is no LCD display function. Set the corresponding bits to 0 by setting registers LSE1, LSE4 and LSE5 for these pins.
2. When using the LCD drive control circuit, set the corresponding bit in the LSE5 register to 1.

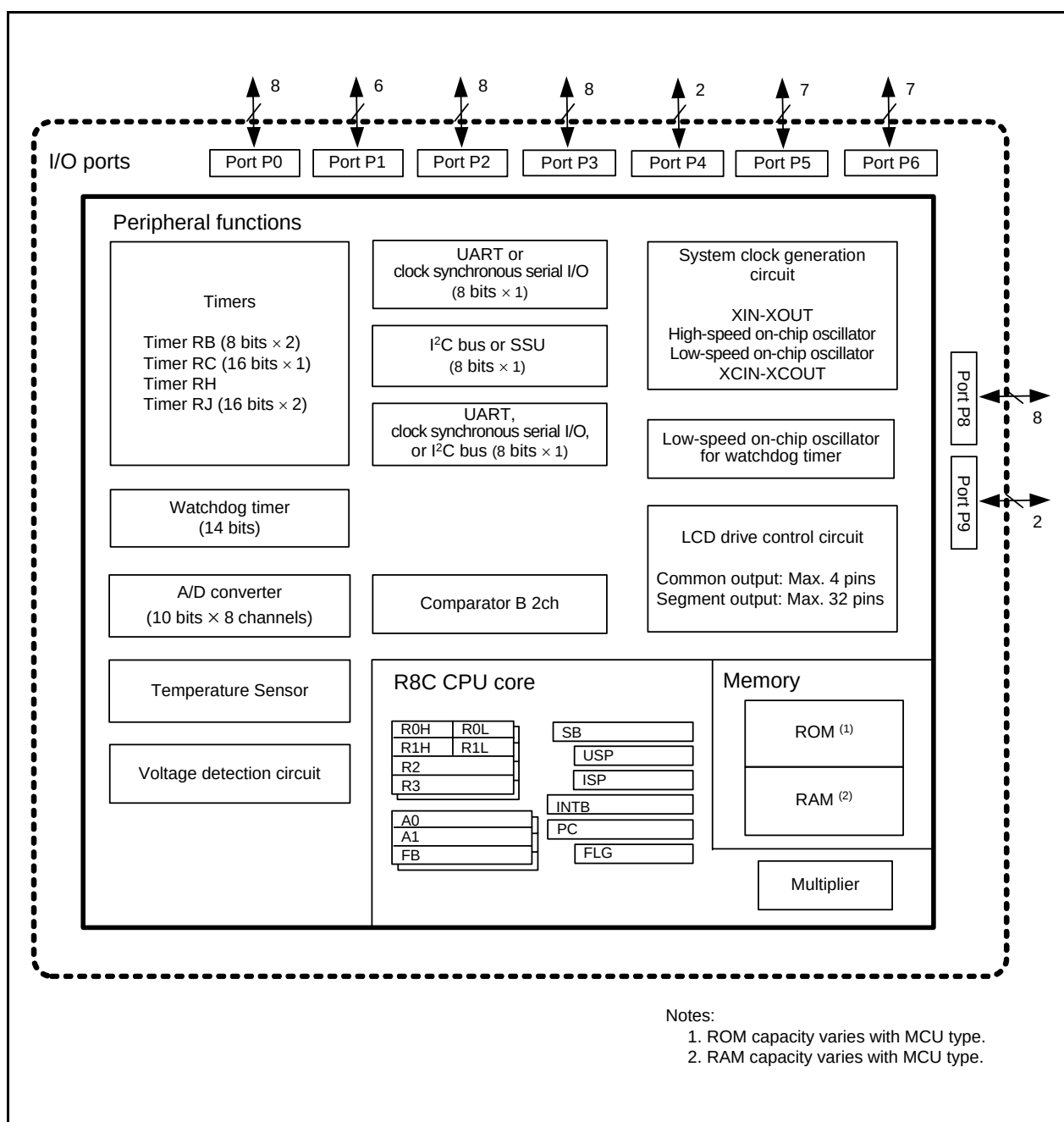


Figure 1.7 Block Diagram of R8C/LA6A Group

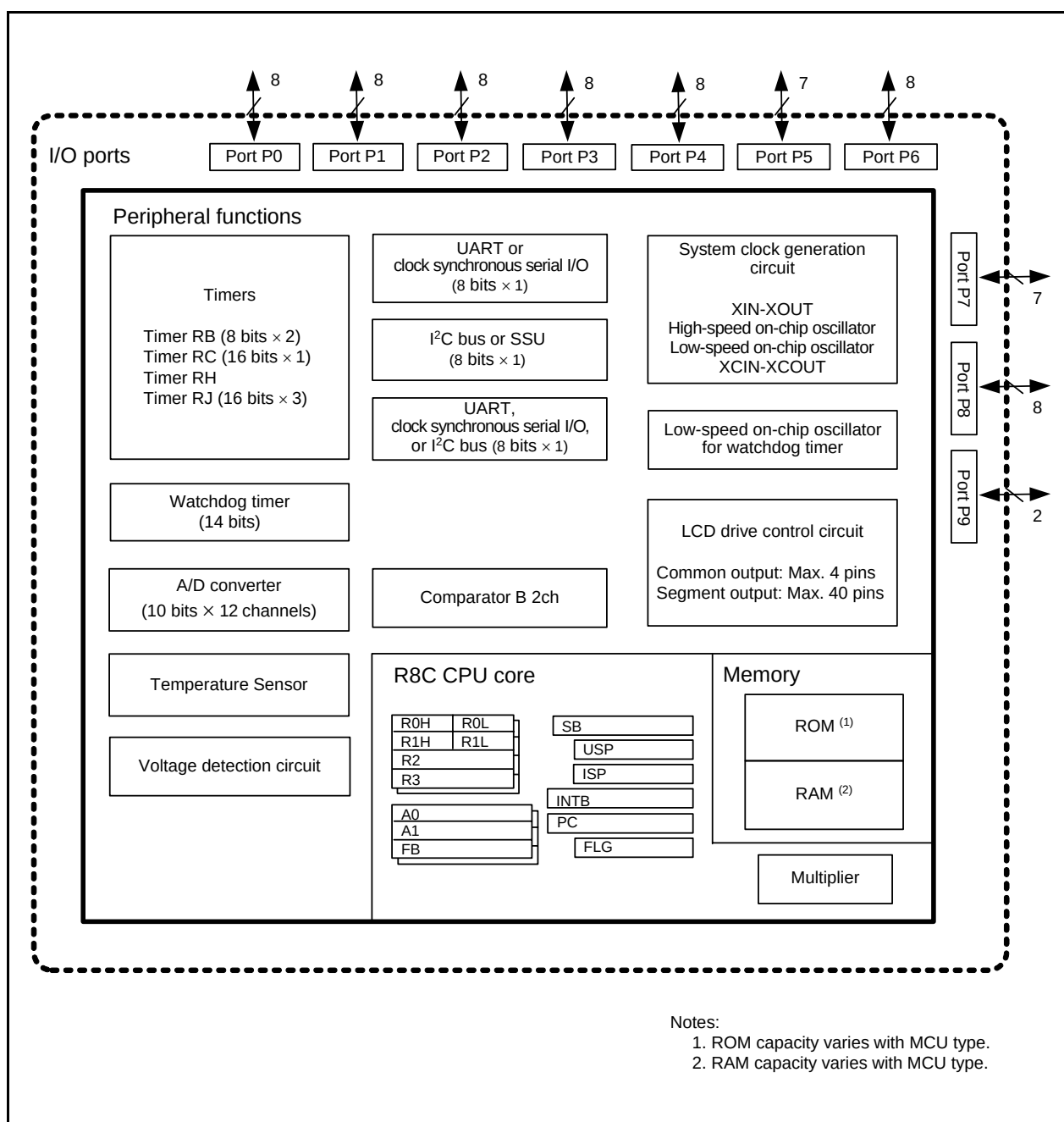


Figure 1.8 Block Diagram of R8C/LA8A Group

1.4 Pin Assignments

Figures 1.9 to 1.12 show pin assignments (top view). Tables 1.13 to 1.17 list the pin name information by pin number.

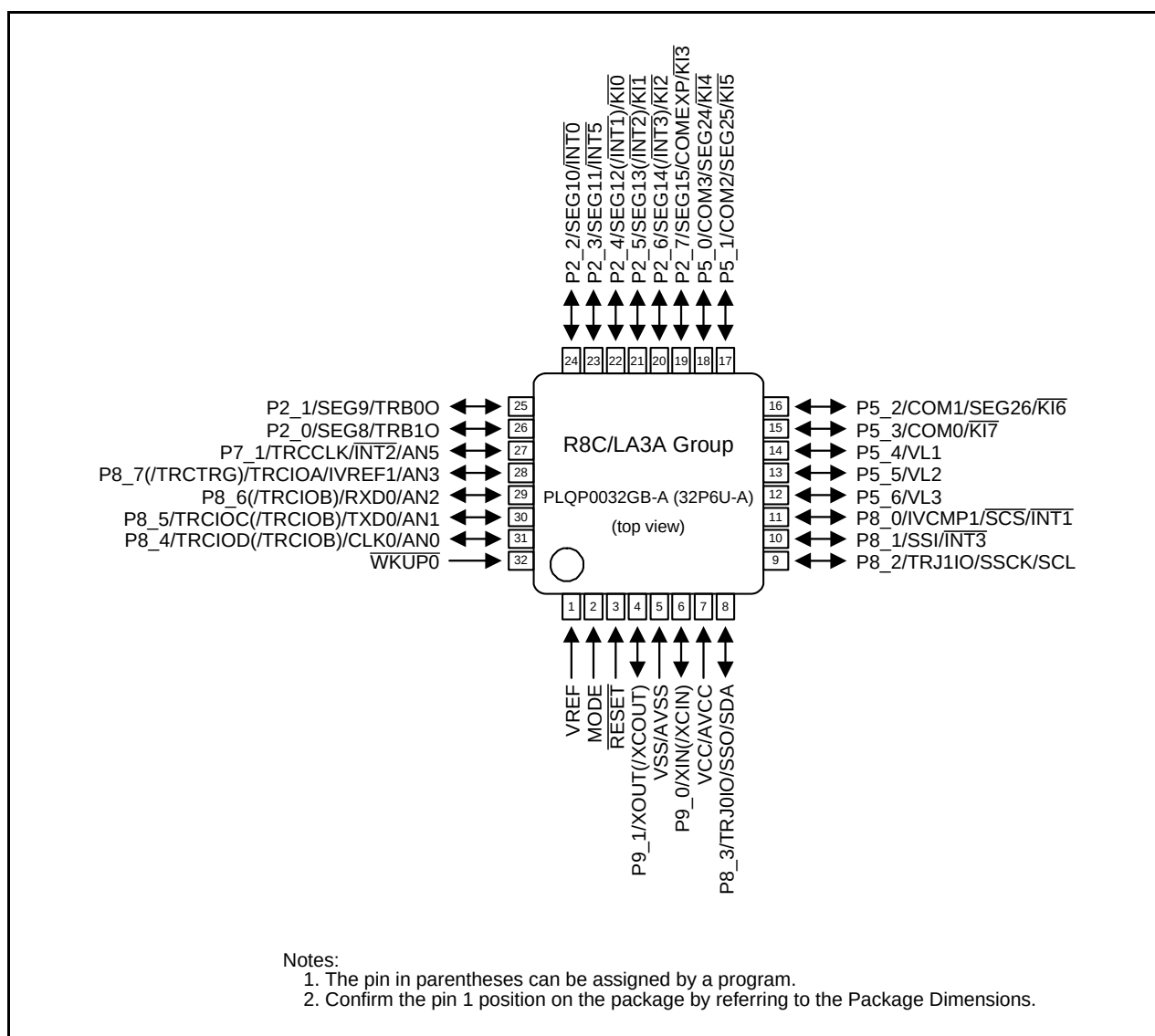


Figure 1.9 Pin Assignment (Top View) of PLQP0032GB-A Package

Table 1.16 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(2)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, Comparator B	LCD drive Control Circuit
31			P4_4							SEG36
32			P4_3							SEG35
33			P4_2							SEG34
34			P4_1							SEG33
35			P4_0							SEG32
36	27		P3_7	($\overline{\text{INT7}}$)						SEG31
37	28		P3_6	($\overline{\text{INT6}}$)						SEG30
38	29		P3_5	($\overline{\text{INT5}}$)						SEG29
39	30		P3_4	($\overline{\text{INT4}}$)						SEG28
40	31		P3_3	($\overline{\text{INT3}}$)						SEG27
41	32		P3_2	($\overline{\text{INT2}}$)						SEG26
42	33		P3_1	($\overline{\text{INT1}}$)						SEG25
43	34		P3_0	($\overline{\text{INT0}}$)						SEG24
44	35		P2_7							SEG23
45	36		P2_6							SEG22
46	37		P2_5							SEG21
47	38		P2_4							SEG20
48	39		P2_3							SEG19
49	40		P2_2							SEG18
50	41		P2_1							SEG17
51	42		P2_0							SEG16
52	43		P1_7							SEG15
53	44		P1_6	$\overline{\text{INT6}}$						SEG14
54	45		P1_5	$\overline{\text{INT5}}$						SEG13
55	46		P1_4	$\overline{\text{INT4}}$						SEG12
56	47		P1_3	$\overline{\text{KI7}}$						SEG11
57	48		P1_2	$\overline{\text{KI6}}$						SEG10
58			P1_1							SEG9
59			P1_0							SEG8
60	49		P0_7	$\overline{\text{KI5}}$	TRHO					SEG7
61	50		P0_6	$\overline{\text{KI4}}$						SEG6
62	51		P0_5	$\overline{\text{KI3}}$						SEG5
63	52		P0_4	$\overline{\text{KI2}}$						SEG4
64	53		P0_3	$\overline{\text{KI1}}/\overline{\text{INT0}}$						SEG3
65	54		P0_2	$\overline{\text{KI0}}$	(TRCTR $\overline{\text{G}}$)					SEG2
66	55		P0_1	$\overline{\text{INT7}}$	(TRCTR $\overline{\text{G}}$ /TRCCLK)				$\overline{\text{ADTRG}}$	SEG1
67	56		P0_0		(TRCIOA/TRCTR $\overline{\text{G}}$)				AN11	SEG0
68	57		P6_7		(TRCIOB)				AN10	

Note:

1. The pin in parentheses can be assigned by a program.

Table 4.10 SFR Information for R8C/LA8A Group (1) ⁽¹⁾

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h 00000100b ⁽²⁾
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register 0	MSTCR0	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh ⁽³⁾
000Ch	Oscillation Stop Detection Register	OCD	00000100b ⁽⁴⁾ 00h ⁽⁴⁾
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h	Module Standby Control Register 1	MSTCR1	00h
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽⁵⁾
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	XXXXXX00b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Frequency Control Register 0	FRC0	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator 18 MHz Set Value Register 0	FR18S0	XXh
002Ah	High-Speed On-Chip Oscillator 18 MHz Set Value Register 1	FR18S1	XXh
002Bh			
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Frequency Control Register 1	FRC1	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁶⁾ 00100000b ⁽⁷⁾
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b ⁽⁶⁾ 1100X011b ⁽⁷⁾
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- The CSPRO bit in the CSPR register is set to 1.
- The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off 0 mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
- The reset value differs depending on the mode.
- The CSPROINI bit in the OFS register is set to 0.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.

Table 4.12 SFR Information for R8C/LA8A Group (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h	Timer RJ2 Control Register	TRJ2CR	00h
0091h	Timer RJ2 I/O Control Register	TRJ2IOC	00h
0092h	Timer RJ2 Mode Register	TRJ2MR	00h
0093h	Timer RJ2 Event Pin Select Register	TRJ2ISR	00h
0094h	Timer RJ2 Register	TRJ2	FFh
0095h			FFh
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.18 SFR Information for R8C/LA8A Group (9) ⁽¹⁾

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h			
0202h	LCD Option Clock Control Register	LCR2	00h
0203h	LCD Clock Control Register	LCR3	00h
0204h	LCD Display Control Register	LCR4	00h
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h	LCD Port Select Register 3	LSE3	00h
020Ah	LCD Port Select Register 4	LSE4	00h
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch			
020Dh			
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh		LRA27L	XXh
022Ch		LRA28L	XXh
022Dh		LRA29L	XXh
022Eh		LRA30L	XXh
022Fh		LRA31L	XXh
0230h		LRA32L	XXh
0231h		LRA33L	XXh
0232h		LRA34L	XXh
0233h		LRA35L	XXh
0234h		LRA36L	XXh
0235h		LRA37L	XXh
0236h		LRA38L	XXh
0237h		LRA39L	XXh
:			
2FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

5.1.4 DC Characteristics

Table 5.18 DC Characteristics (1) [4.0 V ≤ V_{CC} ≤ 5.5 V]
(T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition			Standard			Unit
						Min.	Typ.	Max.	
V _{OH}	Output "H" voltage		Port P8 ⁽¹⁾	V _{CC} = 5V	I _{OH} = −20 mA	V _{CC} − 2.0	−	V _{CC}	V
			Other pins	V _{CC} = 5V	I _{OH} = −5 mA	V _{CC} − 2.0	−	V _{CC}	V
V _{OL}	Output "L" voltage		Port P8 ⁽¹⁾	V _{CC} = 5V	I _{OL} = 20 mA	−	−	2.0	V
			Other pins	V _{CC} = 5V	I _{OL} = 5 mA	−	−	2.0	V
V _{T+} −V _{T−}	Hysteresis	INT0, INT1, INT2, INT3, INT5, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOA, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, ADTRG, RXD0, CLK0, SSI, SCL, SDA, SSO				0.05	0.5	−	V
		RESET, WKUP0				0.1	0.8	−	V
I _{IH}	Input "H" current		V _I = 5 V, V _{CC} = 5 V			−	−	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 5 V			−	−	−5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 5 V			20	40	80	kΩ
R _{FXIN}	Feedback resistance	XIN				−	2.0	−	MΩ
R _{FXCIN}	Feedback resistance	XCIN				−	14	−	MΩ
V _{RAM}	RAM hold voltage		During stop mode			1.8	−	−	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.20 DC Characteristics (3) [2.7 V ≤ V_{CC} < 4.0 V]**(T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)**

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage		Port P8 (1)	I _{OH} = −5 mA	V _{CC} − 0.5	−	V _{CC}	V
			Other pins	I _{OH} = −1 mA	V _{CC} − 0.5	−	V _{CC}	V
V _{OL}	Output "L" voltage		Port P8 (1)	I _{OL} = 5 mA	−	−	0.5	V
			Other pins	I _{OL} = 1 mA	−	−	0.5	V
V _{T+} −V _{T−}	Hysteresis	INT0, INT1, INT2, INT3, INT5, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, ADTRG, RXD0, CLK0, SSI, SCL, SDA, SSO			0.05	0.4	−	V
		RESET, WKUP0			0.1	0.8	−	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3 V		−	−	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3 V		−	−	−5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3 V		25	80	140	kΩ
R _{FXIN}	Feedback resistance	XIN			−	2.0	−	MΩ
R _{FXCIN}	Feedback resistance	XCIN			−	14	−	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	−	−	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.22 DC Characteristics (5) [1.8 V ≤ V_{CC} < 2.7 V]
(T_{opr} = −20 to 85 °C (N version)/ −40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage		Port P8 ⁽¹⁾	I _{OH} = −2 mA	V _{CC} − 0.5	−	V _{CC}	V
			Other pins	I _{OH} = −1 mA	V _{CC} − 0.5	−	V _{CC}	V
V _{OL}	Output "L" voltage		Port P8 ⁽¹⁾	I _{OL} = 2 mA	−	−	0.5	V
			Other pins	I _{OL} = 1 mA	−	−	0.5	V
V _{T+} −V _{T−}	Hysteresis	INT0, INT1, INT2, INT3, INT5, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRCTRG, TRCCLK, ADTRG, RXD0, CLK0, SSI, SCL, SDA, SSO			0.05	0.4	−	V
		RESET, WKUP0			0.1	0.8	−	V
I _{IH}	Input "H" current		V _I = 1.8 V, V _{CC} = 1.8 V		−	−	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 1.8 V		−	−	−4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 1.8 V		85	220	500	kΩ
R _{FXIN}	Feedback resistance	XIN			−	2.0	−	MΩ
R _{FXCIN}	Feedback resistance	XCIN			−	14	−	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	−	−	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by P8DRR register. When the drive capacity is set to Low, the value of any other pin applies.

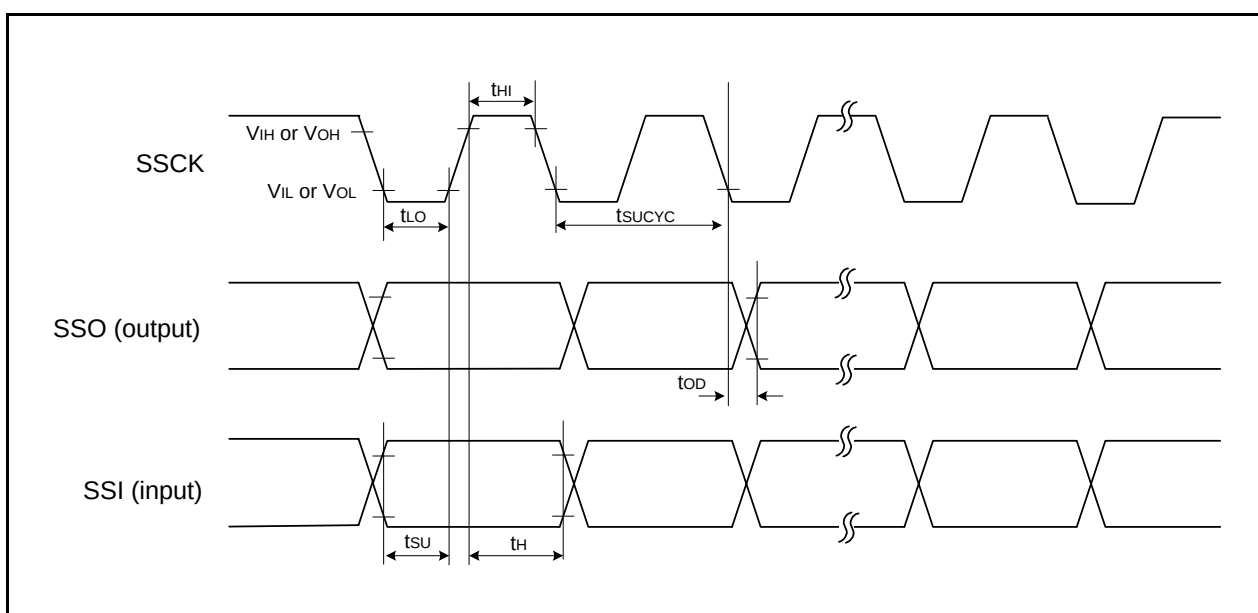


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.28 Timing Requirements of Serial Interface
($V_{SS} = 0\text{ V}$ and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (CK)	CLK0 input cycle time	800	—	300	—	200	—	ns
t _w (CKH)	CLK0 input “H” width	400	—	150	—	100	—	ns
t _w (CKL)	CLK0 input “L” width	400	—	150	—	100	—	ns
t _d (C-Q)	TXD0 output delay time	—	200	—	80	—	50	ns
t _h (C-Q)	TXD0 hold time	0	—	0	—	0	—	ns
t _{su} (D-C)	RXD0 input setup time	150	—	70	—	50	—	ns
t _h (C-D)	RXD0 input hold time	90	—	90	—	90	—	ns

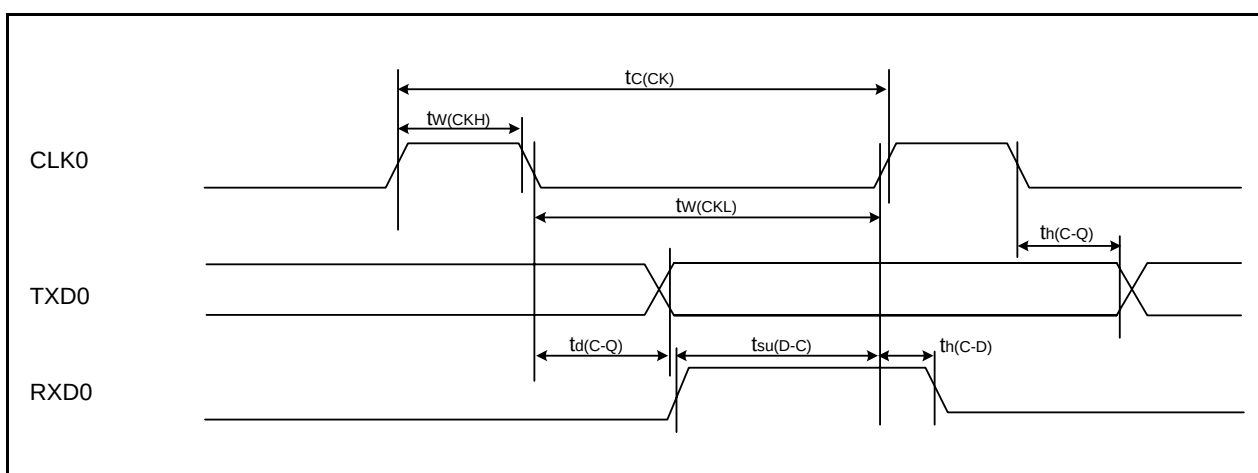


Figure 5.10 Input and Output Timing of Serial Interface

Table 5.29 Timing Requirements of External Interrupt $\overline{\text{INT}}i$ ($i = 0\text{ to }3, 5, 7$) and Key Input Interrupt $\overline{\text{K}}i$ ($i = 0\text{ to }7$)
($V_{SS} = 0\text{ V}$ and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tw(INH)	$\overline{\text{INT}}i$ input "H" width, $\overline{\text{K}}i$ input "H" width	1000 ⁽¹⁾	—	380 ⁽¹⁾	—	250 ⁽¹⁾	—	ns
tw(INL)	$\overline{\text{INT}}i$ input "L" width, $\overline{\text{K}}i$ input "L" width	1000 ⁽²⁾	—	380 ⁽²⁾	—	250 ⁽²⁾	—	ns

Notes:

- When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

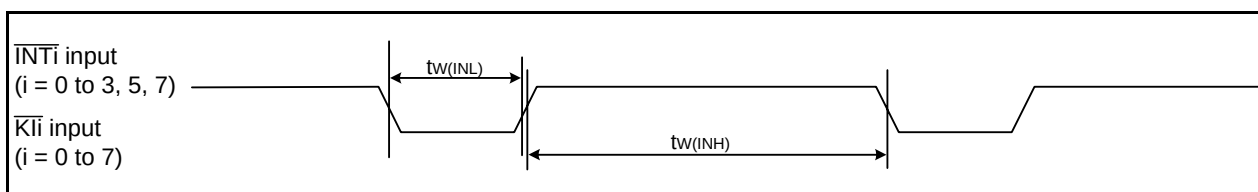


Figure 5.11 Input Timing of External Interrupt $\overline{\text{INT}}i$ and Key Input Interrupt $\overline{\text{K}}i$

Table 5.34 Gain Amplifier Characteristics
(VSS = 0 V and Topr = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
VGAIN	Gain amplifier operating range		0.4	–	AVCC – 1.0	V
φAD	A/D conversion clock		1	–	5	MHz

Table 5.35 Comparator B Characteristics
(Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version)/–40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	Vcc – 1.4	V
Vi	IVCMP1, IVCMP3 input voltage		-0.3	–	Vcc + 0.3	V
–	Offset		–	5	100	mV
td	Comparator output delay time ⁽¹⁾	Vi = Vref ± 100 mV	–	–	1	μs
ICMP	Comparator operating current	Vcc = 5.0 V	–	12	–	μA

Note:

1. When the digital filter is disabled.

Table 5.36 Flash Memory (Program ROM) Characteristics
(Vcc = 1.8 to 5.5 V and Topr = 0 to 60°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽¹⁾		10,000 ⁽²⁾	–	–	times
–	Byte program time		–	80	–	μs
–	Block erase time	Internal ROM Capacity: 16 KB, 32 KB, 48 KB, 64 KB	–	0.12	–	s
		Internal ROM Capacity: 96 KB, 128 KB	–	0.2	–	s
td(SR-SUS)	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	μs
td(CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	μs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time ⁽⁶⁾	Ambient temperature = 85°C	10	–	–	year

Notes:

1. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.40 Voltage Detection 2 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage detection level V _{det2_0} ⁽¹⁾	At the falling of V _{CC}	3.70	4.0	4.30	V
–	Hysteresis width at the rising of V _{CC} in voltage detection 2 circuit		–	0.10	–	V
–	Voltage detection 2 circuit response time ⁽²⁾	In operation		20	150	μs
		In stop mode		200	500	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, V _{CC} = 5.0 V	–	1.7	–	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		–	–	100	μs

Notes:

1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.41 Power-on Reset Circuit Characteristics ⁽¹⁾
(T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{rth}	External power V _{CC} rise gradient		0	–	50000	mV/ms

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

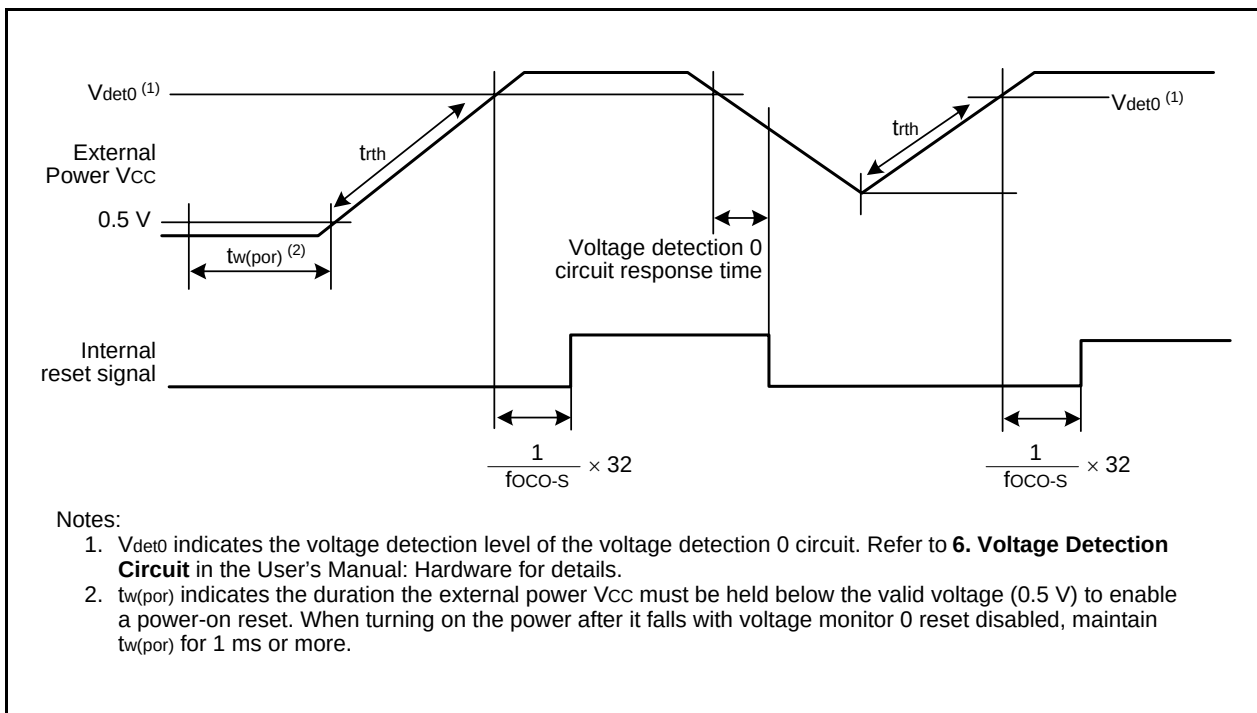


Figure 5.14 Power-on Reset Circuit Characteristics

Table 5.51 DC Characteristics (5) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output “H” voltage		Port P7_0, P7_1, P8 ⁽¹⁾	I _{OH} = −2 mA	V _{CC} − 0.5	−	V _{CC}	V
			Other pins	I _{OH} = −1 mA	V _{CC} − 0.5	−	V _{CC}	V
V _{OL}	Output “L” voltage		Port P7_0, P7_1, P8 ⁽¹⁾	I _{OL} = 2 mA	−	−	0.5	V
			Other pins	I _{OL} = 1 mA	−	−	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, INT4, INT5, INT6, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	−	V
		RESET, WKUP0						
I _{IH}	Input “H” current		V _I = 1.8 V, V _{CC} = 1.8 V		−	−	4.0	μA
I _{IL}	Input “L” current		V _I = 0 V, V _{CC} = 1.8 V		−	−	−4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 1.8 V		85	220	500	kΩ
R _{IXIN}	Feedback resistance	XIN			−	2.0	−	MΩ
R _{IXCIN}	Feedback resistance	XCIN			−	14	−	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	−	−	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7D_{RR} and P8D_{RR}. When the drive capacity is set to Low, the value of any other pin applies.

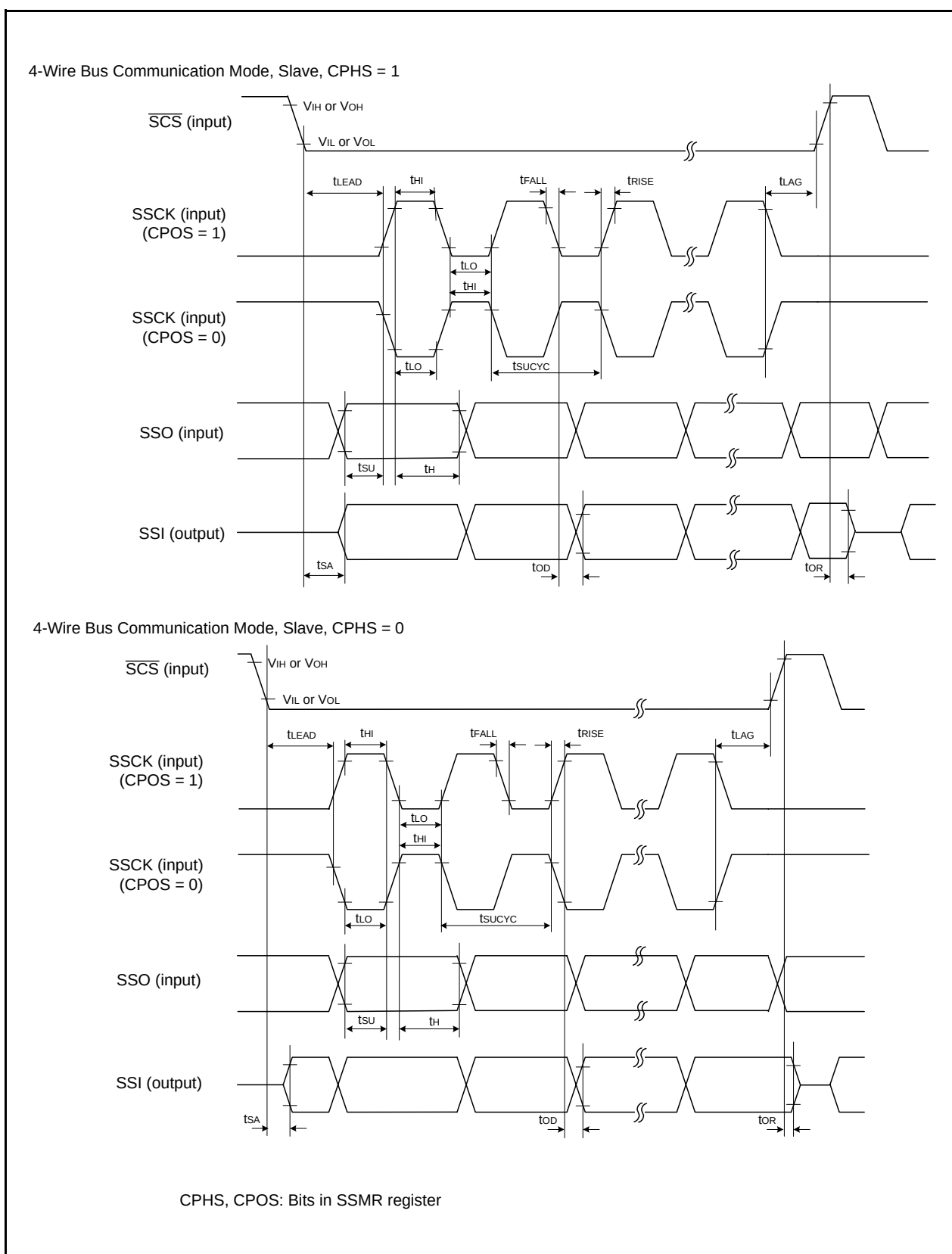


Figure 5.16 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

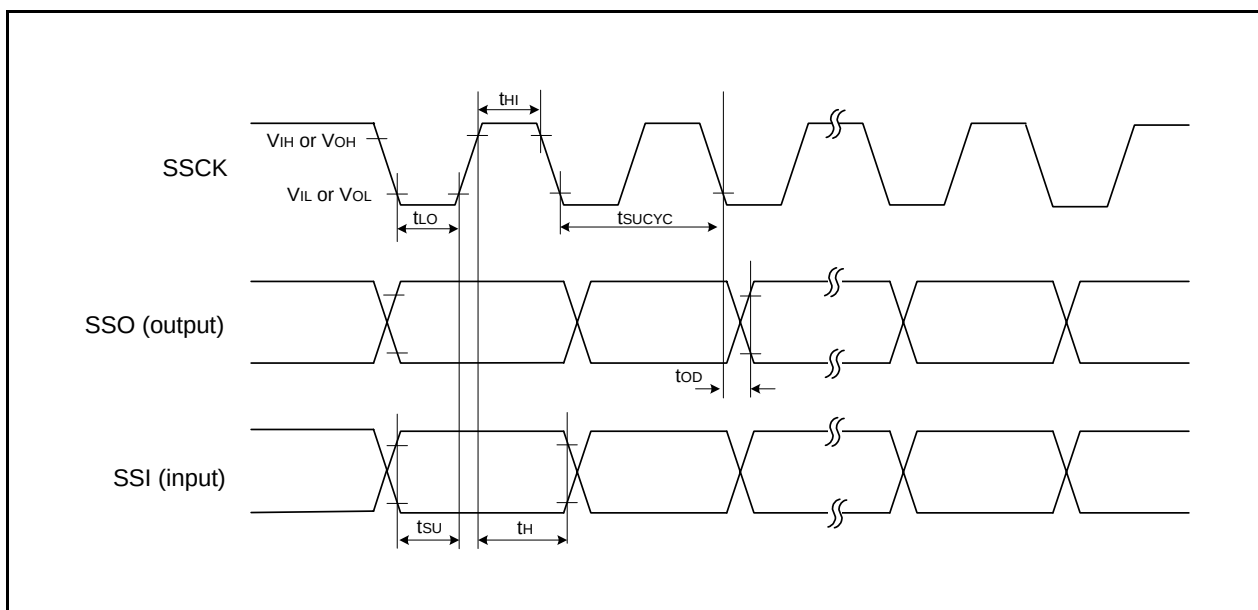


Figure 5.17 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

