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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la8aadfp-v0

1.2 Product Lists

Tables 1.9 to 1.12 list product information for each group. Figures 1.1 to 1.4 show the Correspondence of Part No., with Memory Size and Package for each group.

Table 1.9 Product List for R8C/LA3A Group

Current of Oct 2011

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA32ANFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	N Version
R5F2LA34ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	
R5F2LA32ADFP	8 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	D Version
R5F2LA34ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA36ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0032GB-A	
R5F2LA38ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0032GB-A	

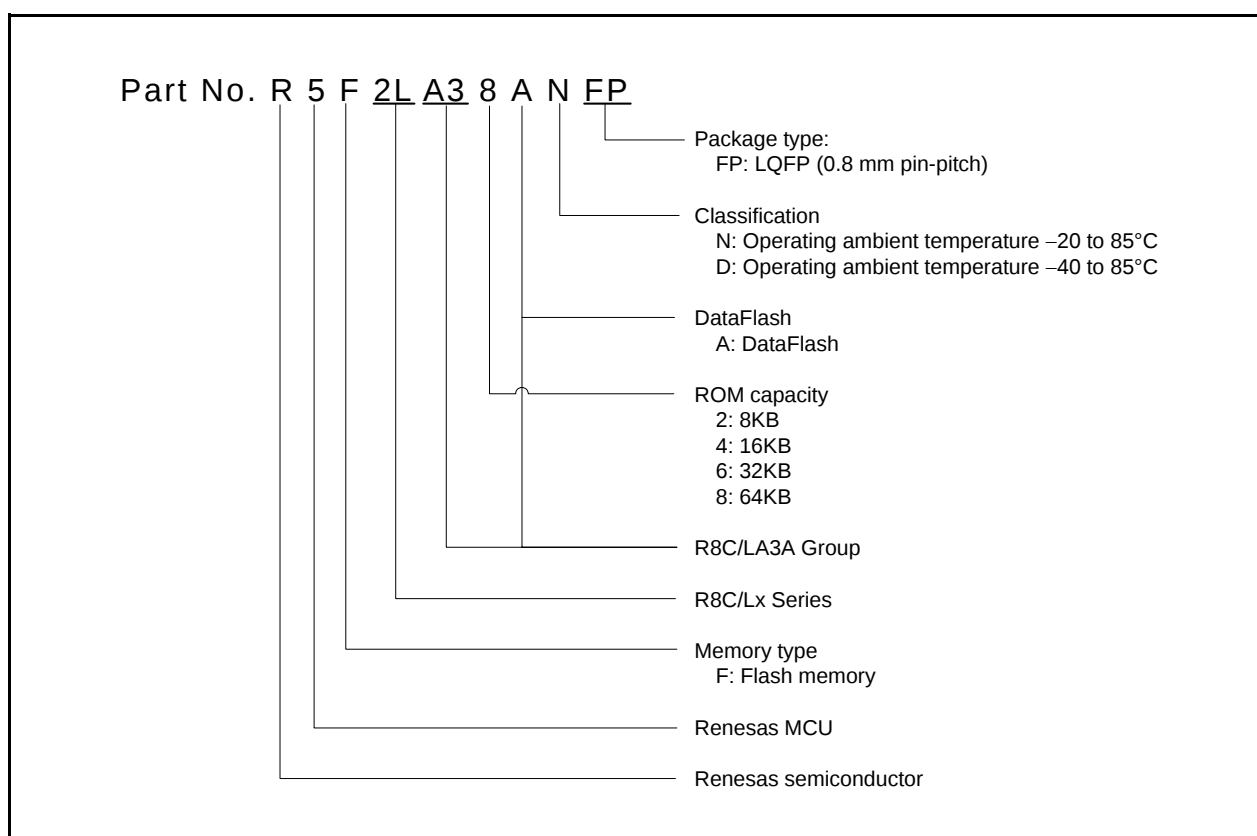


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/LA3A Group

Table 1.12 Product List for R8C/LA8A Group**Current of Oct 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2LA84ANFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	N Version
R5F2LA84ANFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA86ANFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	
R5F2LA86ANFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA87ANFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA87ANFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA88ANFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA88ANFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA8AANFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080KB-A	
R5F2LA8AANFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080JA-A	
R5F2LA8CANFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080KB-A	
R5F2LA8CANFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080JA-A	
R5F2LA84ADFP	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	D Version
R5F2LA84ADFA	16 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA86ADFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080KB-A	
R5F2LA86ADFA	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0080JA-A	
R5F2LA87ADFP	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA87ADFA	48 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA88ADFP	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080KB-A	
R5F2LA88ADFA	64 Kbytes	1 Kbyte × 2	3.5 Kbytes	PLQP0080JA-A	
R5F2LA8AADFP	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080KB-A	
R5F2LA8AADFA	96 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080JA-A	
R5F2LA8CADFP	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080KB-A	
R5F2LA8CADFA	128 Kbytes	2 Kbytes × 2	5.5 Kbytes	PLQP0080JA-A	

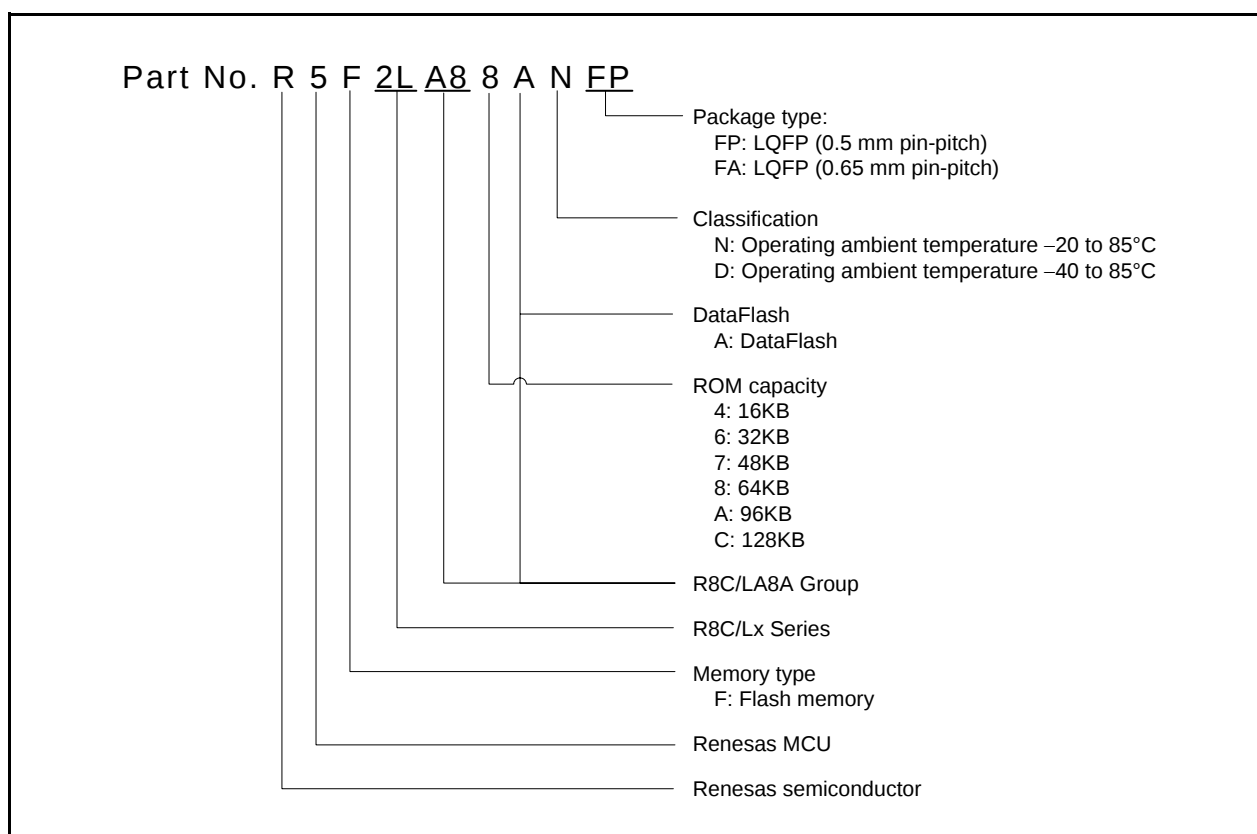
**Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/LA8A Group**

Table 1.17 Pin Name Information by Pin Number (R8C/LA6A Group, R8C/LA8A Group)(3)

Pin Number		Control Pin	Port	I/O Pin Functions for Peripheral Modules						
LA8A	LA6A			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, Comparator B	LCD drive Control Circuit
69	58		P6_6		(TRB00/ TRCIOB/ TRCIOC)				AN9/IVREF3	
70	59		P6_5		(TRB10/ TRCIOB/ TRCIOD)				AN8/IVREF1	
71	60		P6_4				(SSO)	(SDA)	AN7	
72	61		P6_3				(SSCK)	(SCL)	AN6	
73	62		P6_2		(TRJ0IO)		(SSI)		AN5	
74	63		P6_1		(TRJ1IO)		(SCS)		AN4	
75			P6_0		(TRJ2IO)				AN3	
76			P7_6		(TRB00)				AN2	
77			P7_5		TRB10				AN1	
78			P7_4						AN0	
79			P7_3			(CTS2/RTS2)				
80			P7_2		TRJ0O	(RXD2/SCL2/ TXD2/SDA2)				

Note:

1. The pin in parentheses can be assigned by a program.

Table 4.2 SFR Information for R8C/LA5A Group (2) ⁽¹⁾

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h	INT7 Interrupt Control Register	INT7IC	XX00X000b
0044h			
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RH Interrupt Control Register	TRHIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register ⁽²⁾	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RJ0 Interrupt Control Register	TRJ0IC	XXXXX000b
0057h	Timer RB1 Interrupt Control Register	TRB1IC	XXXXX000b
0058h	Timer RB0 Interrupt Control Register	TRB0IC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RJ1 Interrupt Control Register	TRJ1IC	XXXXX000b
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	LCD Interrupt Control Register	LCDIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.11 SFR Information for R8C/LA8A Group (2) ⁽¹⁾

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h	INT7 Interrupt Control Register	INT7IC	XX00X000b
0044h	INT6 Interrupt Control Register	INT6IC	XX00X000b
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RH Interrupt Control Register	TRHIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register ⁽²⁾	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RJ0 Interrupt Control Register	TRJ0IC	XXXXX000b
0057h	Timer RB1 Interrupt Control Register	TRB1IC	XXXXX000b
0058h	Timer RB0 Interrupt Control Register	TRB0IC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RJ1 Interrupt Control Register	TRJ1IC	XXXXX000b
005Ch	Timer RJ2 Interrupt Control Register	TRJ2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah	LCD Interrupt Control Register	LCDIC	XXXXX000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.12 SFR Information for R8C/LA8A Group (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h	Timer RJ2 Control Register	TRJ2CR	00h
0091h	Timer RJ2 I/O Control Register	TRJ2IOC	00h
0092h	Timer RJ2 Mode Register	TRJ2MR	00h
0093h	Timer RJ2 Event Pin Select Register	TRJ2ISR	00h
0094h	Timer RJ2 Register	TRJ2	FFh
0095h			FFh
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.15 SFR Information for R8C/LA8A Group (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.17 SFR Information for R8C/LA8A Group (8) ⁽¹⁾

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h	Port P1 Pull-Up Control Register	P1PUR	00h
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h	Port P4 Pull-Up Control Register	P4PUR	00h
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h	Port P6 Pull-Up Control Register	P6PUR	00h
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h	Port P8 Pull-Up Control Register	P8PUR	00h
01E9h	Port P9 Pull-Up Control Register	P9PUR	00h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P7 Drive Capacity Control Register	P7DRR	00h
01F1h	Port P8 Drive Capacity Control Register	P8DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 5.11 Voltage Detection 2 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage detection level V _{det2_0} ⁽¹⁾	At the falling of V _{CC}	3.70	4.0	4.30	V
–	Hysteresis width at the rising of V _{CC} in voltage detection 2 circuit		–	0.10	–	V
–	Voltage detection 2 circuit response time ⁽²⁾	In operation		20	150	μs
		In stop mode		200	500	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, V _{CC} = 5.0 V	–	1.7	–	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		–	–	100	μs

Notes:

1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.12 Power-on Reset Circuit Characteristics ⁽¹⁾
(T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{rth}	External power V _{CC} rise gradient		0	–	50000	mV/ms

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

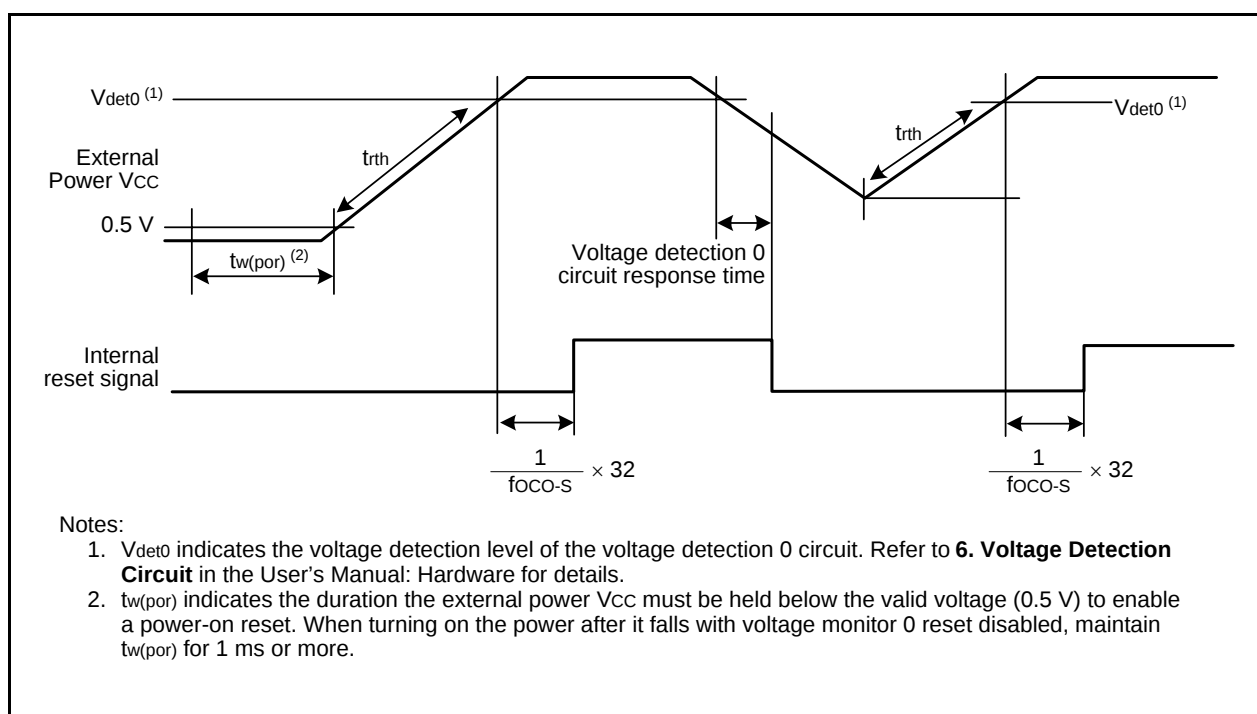


Figure 5.3 Power-on Reset Circuit Characteristics

Table 5.13 High-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8$ V to 5.5 V -20 °C $\leq T_{opr} \leq 85$ °C	19.2	20	20.8	MHz
		$V_{CC} = 1.8$ V to 5.5 V -40 °C $\leq T_{opr} \leq 85$ °C	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽¹⁾	$V_{CC} = 1.8$ V to 5.5 V -20 °C $\leq T_{opr} \leq 85$ °C	17.694	18.432	19.169	MHz
		$V_{CC} = 1.8$ V to 5.5 V -40 °C $\leq T_{opr} \leq 85$ °C	17.510	18.432	19.353	MHz
—	Oscillation stability time		—	5	30	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	530	—	μA

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.14 Low-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	—	35	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	2	—	μA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time		—	—	35	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	2	—	μA

Table 5.15 Power Supply Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = 25$ °C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽¹⁾		—	—	2000	μs

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

5.1.5 AC Characteristics

Table 5.24 Timing Requirements of Synchronous Serial Communication Unit (SSU)
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85 °C (N version)/
 -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	—	—	tcyc (1)
t _{HI}	SSCK clock "H" width			0.4	—	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	—	0.6	tsucyc
trise	SSCK clock rising time	Master		—	—	1	tcyc (1)
		Slave		—	—	1	μs
tfall	SSCK clock falling time	Master		—	—	1	tcyc (1)
		Slave		—	—	1	μs
tsu	SSO, SSI data input setup time			100	—	—	ns
t _H	SSO, SSI data input hold time			1	—	—	tcyc (1)
t _{LEAD}	$\overline{SCS}$ setup time	Slave		1tcyc + 50	—	—	ns
t _{LAG}	$\overline{SCS}$ hold time	Slave		1tcyc + 50	—	—	ns
t _{OD}	SSO, SSI data output delay time			—	—	1tcyc + 20	ns
t _{SA}	SSI slave access time		$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	1.5tcyc + 100	ns
			$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.5tcyc + 200	ns
t _{OR}	SSI slave out open time		$2.7\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	—	—	1.5tcyc + 100	ns
			$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.5tcyc + 200	ns

Note:

1. $1tcyc = 1/f_1(s)$

Table 5.25 Timing Requirements of I²C bus Interface ⁽¹⁾
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/ –40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cy} + 600 ⁽¹⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{cy} + 300 ⁽¹⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{cy} + 500 ⁽¹⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{cy} ⁽¹⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cy} ⁽¹⁾	–	–	ns
t _{STAH}	Start condition input hold time		3t _{cy} ⁽¹⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cy} ⁽¹⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{cy} ⁽¹⁾	–	–	ns
t _{SDAS}	Data input setup time		1t _{cy} + 40 ⁽¹⁾	–	–	ns
t _{SDAH}	Data input hold time		10	–	–	ns

Note:

1. 1t_{cy} = 1/f₁(s)

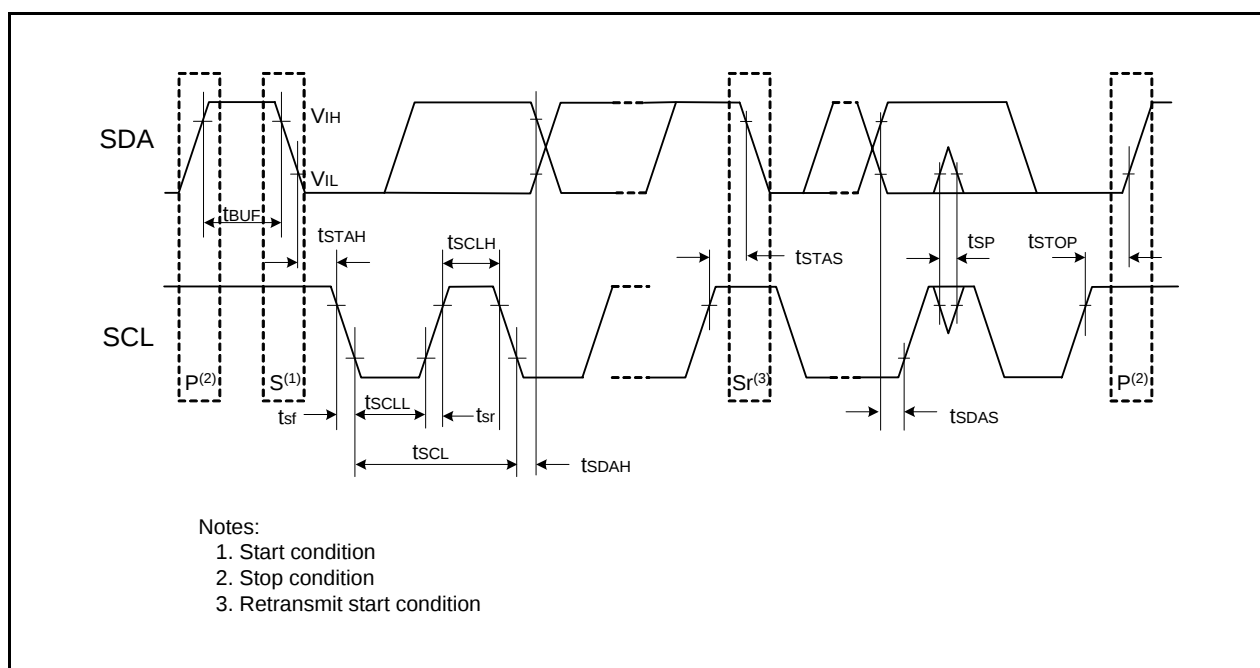


Figure 5.7 I/O Timing of I²C bus Interface

Table 5.28 Timing Requirements of Serial Interface
($V_{SS} = 0\text{ V}$ and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tc(CK)	CLK0 input cycle time	800	—	300	—	200	—	ns
tw(CKH)	CLK0 input “H” width	400	—	150	—	100	—	ns
tw(CKL)	CLK0 input “L” width	400	—	150	—	100	—	ns
td(C-Q)	TXD0 output delay time	—	200	—	80	—	50	ns
th(C-Q)	TXD0 hold time	0	—	0	—	0	—	ns
tsu(D-C)	RXD0 input setup time	150	—	70	—	50	—	ns
th(C-D)	RXD0 input hold time	90	—	90	—	90	—	ns

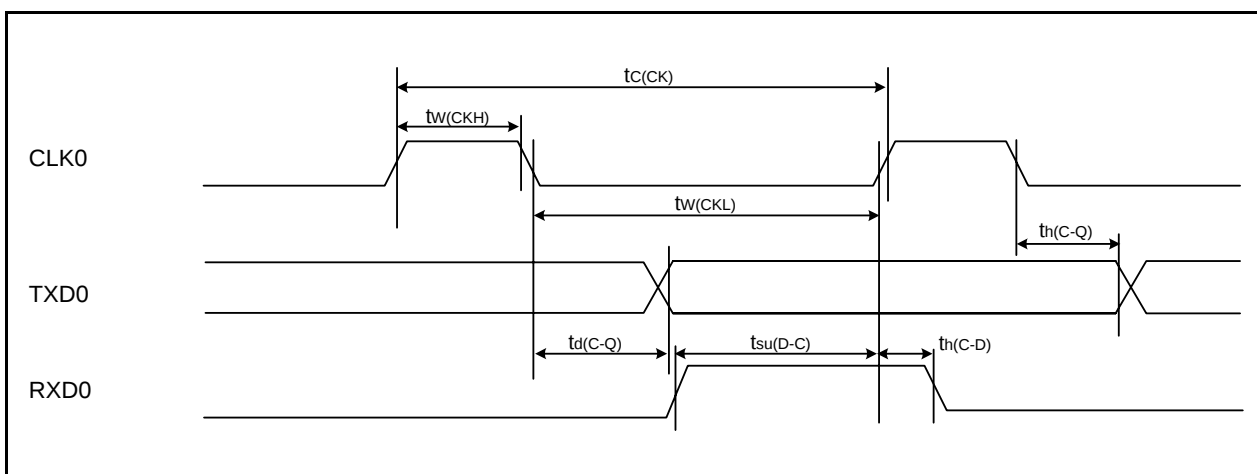


Figure 5.10 Input and Output Timing of Serial Interface

Table 5.29 Timing Requirements of External Interrupt $\overline{\text{INT}}i$ ($i = 0\text{ to }3, 5, 7$) and Key Input Interrupt $\overline{\text{KLI}}i$ ($i = 0\text{ to }7$)
($V_{SS} = 0\text{ V}$ and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tw(INH)	$\overline{\text{INTi}}$ input "H" width, $\overline{\text{KLi}}$ input "H" width	1000 ⁽¹⁾	—	380 ⁽¹⁾	—	250 ⁽¹⁾	—	ns
tw(INL)	$\overline{\text{INTi}}$ input "L" width, $\overline{\text{KLi}}$ input "L" width	1000 ⁽²⁾	—	380 ⁽²⁾	—	250 ⁽²⁾	—	ns

Notes:

1. When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

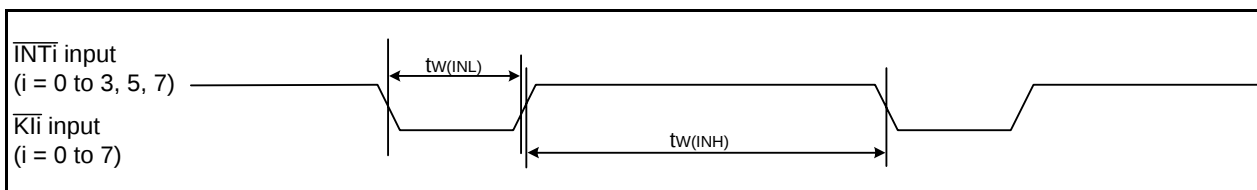


Figure 5.11 Input Timing of External Interrupt $\overline{\text{INT}}i$ and Key Input Interrupt $\overline{\text{KLI}}i$

5.2.2 Recommended Operating Conditions

Table 5.31 Recommended Operating Conditions
(VCC = 1.8 to 5.5 V and Topr = -20 to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc/AVcc	Supply voltage					1.8	–	5.5	V
Vss/AVss	Supply voltage					–	0	–	V
VIH	Input “H” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0.8 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.8 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.9 Vcc	–	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	–	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	–	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	–	Vcc	V
VIL	Input “L” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.05 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.35 Vcc	V
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)				–	–	–160	mA
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)				–	–	–80	mA
IOH(peak)	Peak output “H” current	Port P7_0, P7_1, P8 (2)				–	–	–40	mA
		Other pins				–	–	–10	mA
IOH(avg)	Average output “H” current (1)	Port P7_0, P7_1, P8 (2)				–	–	–20	mA
		Other pins				–	–	–5	mA
IoL(sum)	Peak sum output “L” current	Sum of all pins IoL(peak)				–	–	160	mA
IoL(sum)	Average sum output “L” current	Sum of all pins IoL(avg)				–	–	80	mA
IoL(peak)	Peak output “L” current	Port P7_0, P7_1, P8 (2)				–	–	40	mA
		Other pins				–	–	10	mA
IoL(avg)	Average output “L” current (1)	Port P7_0, P7_1, P8 (2)				–	–	20	mA
		Other pins				–	–	5	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	2	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	2	–	8	MHz
f(XCIN)	XCIN oscillation frequency				1.8 V ≤ Vcc ≤ 5.5 V	–	32.768	–	kHz
					XCIN external clock input frequency				1.8 V ≤ Vcc ≤ 5.5 V
fOCO20M	When used as the count source for timer RC (3)				2.7 V ≤ Vcc ≤ 5.5 V	18.432	–	20	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	-	-	20	MHz
					1.8 V ≤ Vcc < 2.7 V	-	-	8	MHz
–	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	-	-	20	MHz
					1.8 V ≤ Vcc < 2.7 V	-	-	8	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	0	-	20	MHz
					1.8 V ≤ Vcc < 2.7 V	0	-	8	MHz

Notes:

1. The average output current indicates the average value of current measured during 100 ms.
2. This applies when the drive capacity of the output transistor is set to High by registers P7DRR and P8DRR. When the drive capacity is set to Low, the value of any other pin applies.
3. fOCO20M can be used as the count source for timer RC in the range of VCC = 2.7 V to 5.5V.

Table 5.37 Flash Memory (Data flash Block A and Block B) Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽¹⁾		10,000 (2)	–	–	times
–	Byte program time (program/erase endurance ≤ 10,000 times)		–	150	–	μs
–	Block erase time (program/erase endurance ≤ 10,000 times)	Internal ROM Capacity: 1 KB × 2	–	0.05	1	s
		Internal ROM Capacity: 2 KB × 2	–	0.055	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		–	–	0.25 + CPU clock × 3 cycles	ms
–	Time from suspend until erase restart		–	–	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		–	–	30 + CPU clock × 1 cycle	μs
–	Program, erase voltage		1.8	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		–20 ⁽⁶⁾	–	85	°C
–	Data hold time ⁽⁷⁾	Ambient temperature = 85 °C	10	–	–	year

Notes:

- Definition of programming/erasure endurance
 The programming and erasure endurance is defined on a per-block basis.
 If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40°C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.

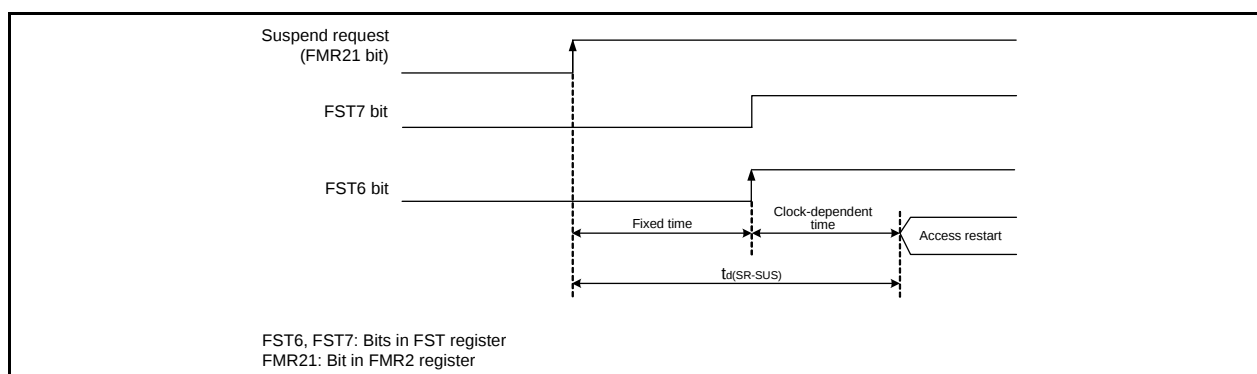


Figure 5.13 Time delay until Suspend

Table 5.49 DC Characteristics (3) [$2.7\text{ V} \leq V_{CC} < 4.0\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version)/ $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output “H” voltage		Port P7_0, P7_1, P8 (1)	IOH = −5 mA	Vcc − 0.5	−	Vcc	V
			Other pins	IOH = −1 mA	Vcc − 0.5	−	Vcc	V
VOL	Output “L” voltage		Port P7_0, P7_1, P8 (1)	IOL = 5 mA	−	−	0.5	V
			Other pins	IOL = 1 mA	−	−	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, INT4, INT5, INT6, INT7, KI0, KI1, KI2, KI3, KI4, KI5, KI6, KI7, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRJ0IO, TRJ1IO, TRJ2IO, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SSI, SCL, SDA, SSO			0.05	0.4	−	V
		RESET, WKUP0			0.1	0.8	−	V
IIH	Input “H” current		VI = 3 V, Vcc = 3 V		−	−	5.0	μA
IIL	Input “L” current		VI = 0 V, Vcc = 3 V		−	−	−5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3 V		25	80	140	kΩ
RFXIN	Feedback resistance	XIN			−	2.0	−	MΩ
RFXCIN	Feedback resistance	XCIN			−	14	−	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	−	−	V

Note:

1. This applies when the drive capacity of the output transistor is set to High by registers P7DDR and P8DDR. When the drive capacity is set to Low, the value of any other pin applies.

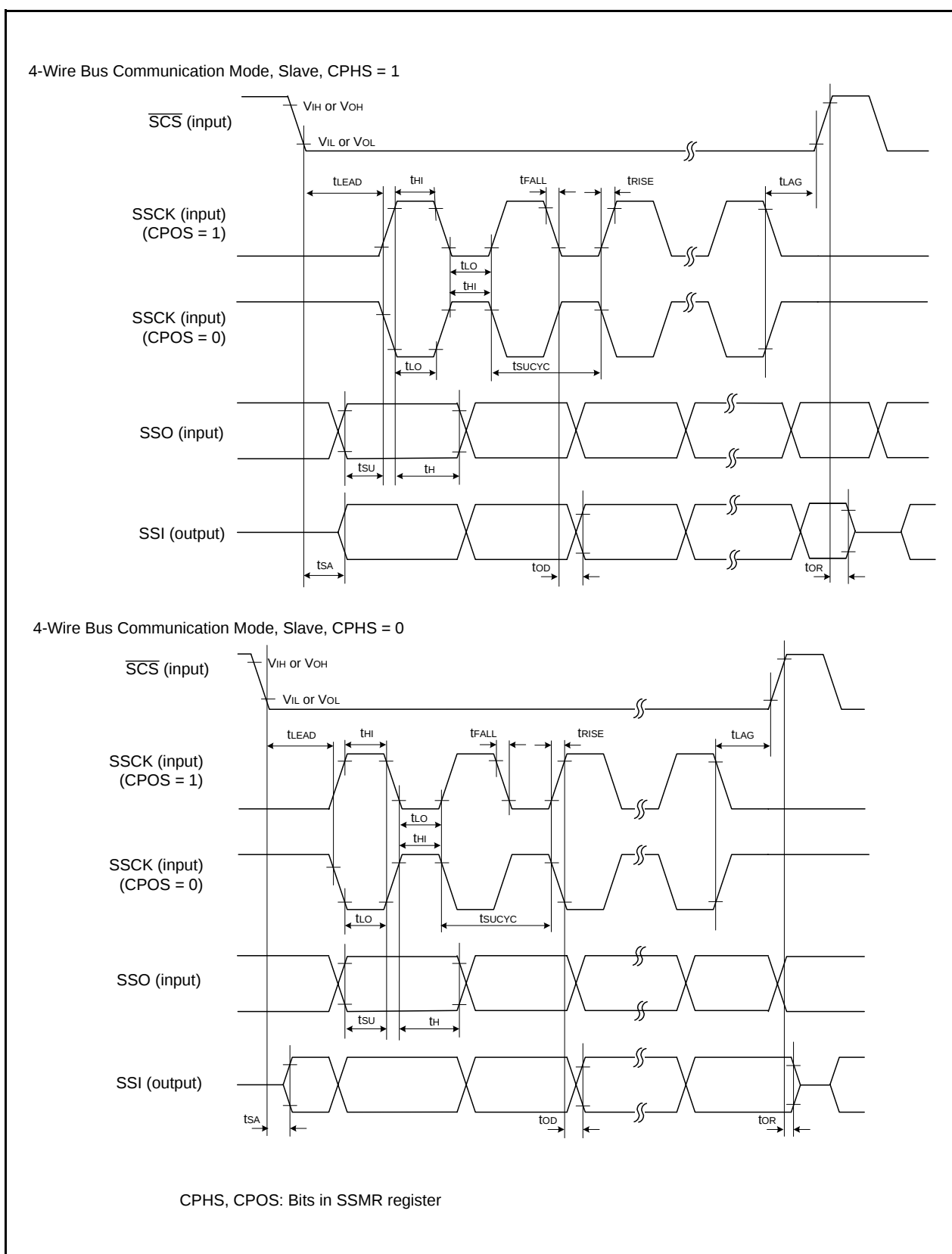


Figure 5.16 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

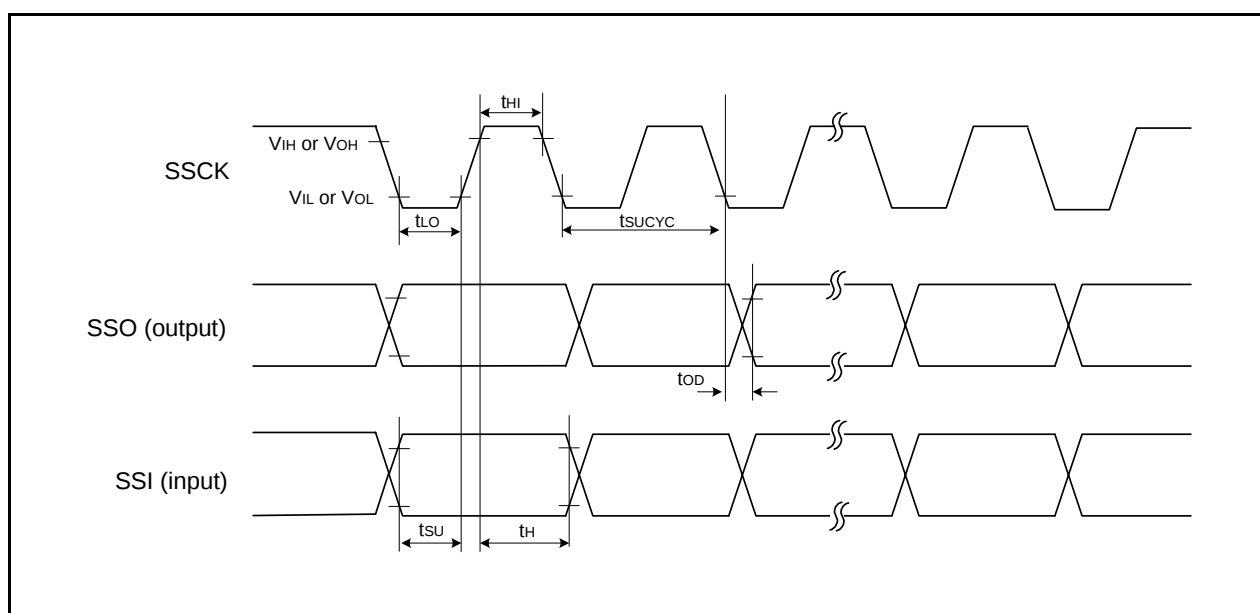


Figure 5.17 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.55 Timing Requirements of External Clock Input (XIN, XCIN)
(V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		VCC = 2.2V, Topr = 25°C		VCC = 3V, Topr = 25°C		VCC = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tC(XIN)	XIN input cycle time	200	—	50	—	50	—	ns
tWH(XIN)	XIN input “H” width	90	—	24	—	24	—	ns
tWL(XIN)	XIN input “L” width	90	—	24	—	24	—	ns
tC(XCIN)	XCIN input cycle time	20	—	20	—	20	—	μs
tWH(XCIN)	XCIN input “H” width	10	—	10	—	10	—	μs
tWL(XCIN)	XCIN input “L” width	10	—	10	—	10	—	μs

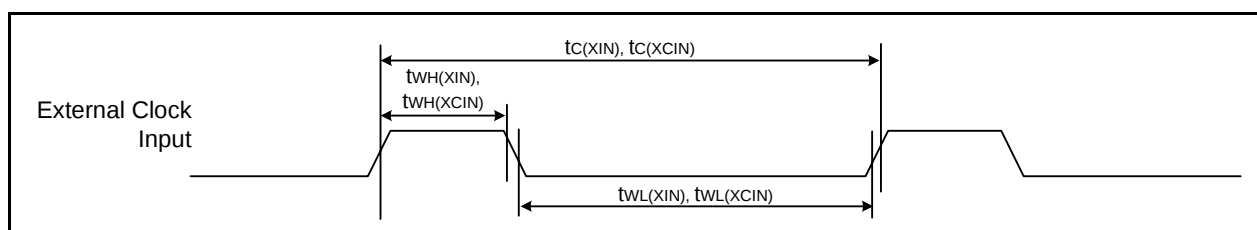


Figure 5.19 External Clock Input Timing

Table 5.56 Timing Requirements of TRJiIO (i = 0 to 2)
(V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version)/ –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (TRJiO)	TRJiO input cycle time	500	—	300	—	100	—	ns
t _{WH} (TRJiO)	TRJiO input “H” width	200	—	120	—	40	—	ns
t _{WL} (TRJiO)	TRJiO input “L” width	200	—	120	—	40	—	ns

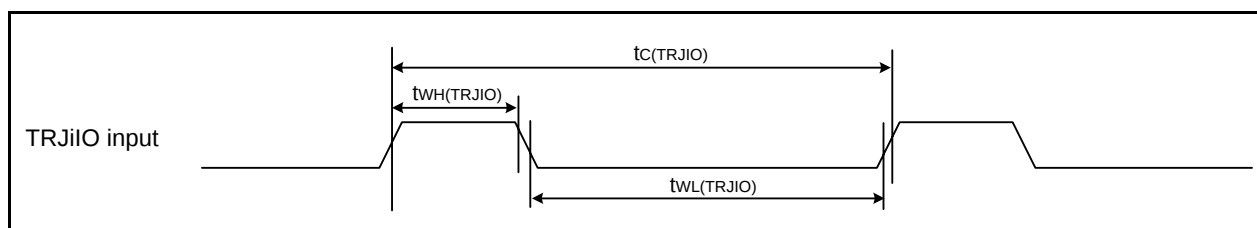


Figure 5.20 Input Timing of TRJiIO

