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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	72
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2la8aanfp-30

Table 1.2 Programmable I/O Ports Provided for Each Group (R8C/LA3A Group, R8C/LA5A Group)

Programmable I/O Port	R8C/LA3A Group Total: 26 I/O pins								R8C/LA5A Group Total: 44 I/O pins							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	✓	—	—	—	—	—	—	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:

1. The symbol “✓” indicates a programmable I/O port.
2. The symbol “—” indicates the settings should be made as follows:
 - Set 0 to the corresponding bits in the PDi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the Pi (i = 0, 3, 5, 7, 9) register. When read, the content is 0.

Table 1.3 Programmable I/O Ports Provided for Each Group (R8C/LA6A Group, R8C/LA8A Group)

Programmable I/O Port	R8C/LA6A Group Total: 56 I/O pins								R8C/LA8A Group Total: 72 I/O pins							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P1	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P4	✓	✓	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓
P5	—	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
P6	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓	✓
P7	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
P8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
P9	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	✓	✓

Notes:

1. The symbol “✓” indicates a programmable I/O port.
2. The symbol “—” indicates the settings should be made as follows:
 - Set 0 to the corresponding bits in the PDi (i = 1, 4 to 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the Pi (i = 1, 4 to 7, 9) register. When read, the content is 0.
 - Set 0 to the corresponding bits in the P7DRR register. When read, the content is 0.

Table 1.7 Specifications (2)

Item	Function		Specification		
Timer	Timer RB0, Timer RB1		8 bits × 2 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode		
	Timer RC		16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)		
	Timer RH		Real-time clock mode (counting of seconds, minutes, hours, day of the week, date, month, year), output compare mode		
	Timer RJ0 Timer RJ1 Timer RJ2	R8C/LA3A Group R8C/LA5A Group R8C/LA6A Group	Timer RJ0, Timer RJ1	16 bits × 2	Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
		R8C/LA8A Group	Timer RJ0, Timer RJ1, Timer RJ2	16 bits × 3	
Serial Interface	UART0		1 channel Clock synchronous serial I/O/UART		
	UART2		1 channel Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), multiprocessor communication function		
Synchronous Serial Communication Unit (SSU)			1 (shared with I ² C-bus)		
I ² C bus			1 (shared with SSU)		
A/D Converter	R8C/LA3A Group		10-bit resolution × 5 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))		
	R8C/LA5A Group		10-bit resolution × 7 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))		
	R8C/LA6A Group		10-bit resolution × 8 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))		
	R8C/LA8A Group		10-bit resolution × 12 channels, including sample and hold function, with sweep mode, temperature sensor included (measurement temperature range: –20 to 85 °C (N version)/ –40 to 85 °C (D version))		
Comparator B	R8C/LA3A Group		1 circuit (comparator B1)		
	R8C/LA5A Group R8C/LA6A Group R8C/LA8A Group		2 circuits (comparator B1, comparator B3)		

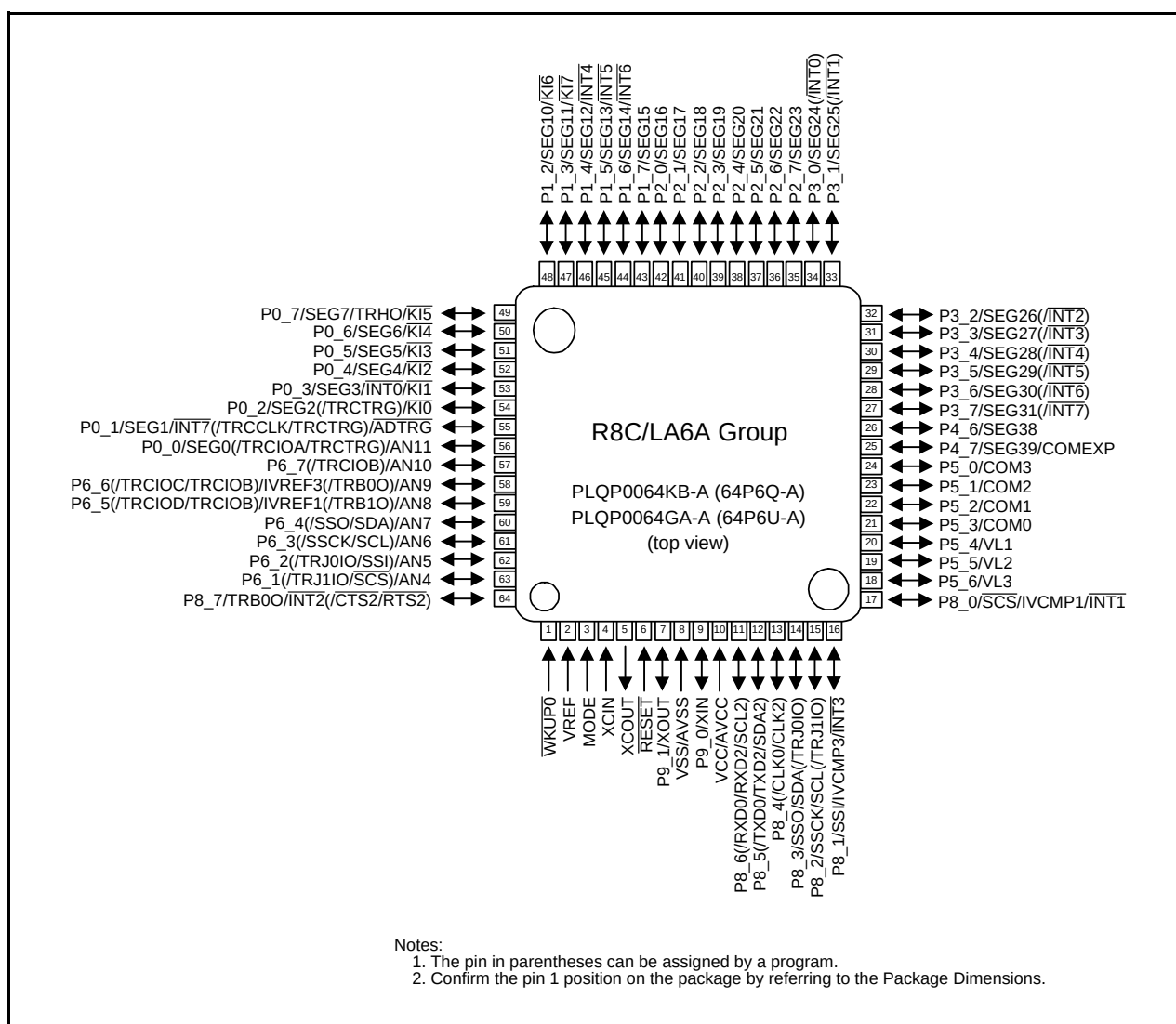


Figure 1.11 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages

Table 1.21 Pin Functions for R8C/LA8A Group (2)

Item	Pin Name	I/O Type	Description
I ² C bus	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter.
A/D converter	AN0 to AN11	I	A/D converter analog input pins.
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_6, P6_0 to P6_7, P7_0 to P7_6, P8_0 to P8_7, P9_0, P9_1	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Ports P7_0, P7_1 and P8 can be used as LED drive ports.
Segment output	SEG0 to SEG39	O	LCD segment output pins.
Common output	COM0 to COM3, COMEXP	O	LCD common output pins.
LCD power supply	VL1	I	Apply the following voltage: $1\text{ V} \leq \text{VL1} \leq \text{VCC}$ and $\text{VL1} \leq \text{VL2}$.
	VL2	I	Apply the following voltage: $\text{VL2} \leq 5.5\text{ V}$ and $\text{VL1} \leq \text{VL2} \leq \text{VL3}$.
	VL3	I	Apply the following voltage: $\text{VL3} \leq 5.5\text{ V}$ and $\text{VL2} \leq \text{VL3}$.

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 4.3 SFR Information for R8C/LA5A Group (3) ⁽¹⁾

Address	Register	Symbol	After Reset
0080h	Timer RJ0 Control Register	TRJ0CR	00h
0081h	Timer RJ0 I/O Control Register	TRJ0IOC	00h
0082h	Timer RJ0 Mode Register	TRJ0MR	00h
0083h	Timer RJ0 Event Pin Select Register	TRJ0ISR	00h
0084h	Timer RJ0 Register	TRJ0	FFh
0085h			FFh
0086h			
0087h			
0088h	Timer RJ1 Control Register	TRJ1CR	00h
0089h	Timer RJ1 I/O Control Register	TRJ1IOC	00h
008Ah	Timer RJ1 Mode Register	TRJ1MR	00h
008Bh	Timer RJ1 Event Pin Select Register	TRJ1ISR	00h
008Ch	Timer RJ1 Register	TRJ1	FFh
008Dh			FFh
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h	Timer RB1 Control Register	TRB1CR	00h
0099h	Timer RB1 One-Shot Control Register	TRB1OCR	00h
009Ah	Timer RB1 I/O Control Register	TRB1IOC	00h
009Bh	Timer RB1 Mode Register	TRB1MR	00h
009Ch	Timer RB1 Prescaler Register	TRB1PRE	FFh
009Dh	Timer RB1 Secondary Register	TRB1SC	FFh
009Eh	Timer RB1 Primary Register	TRB1PR	FFh
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.6 SFR Information for R8C/LA5A Group (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. Blank spaces are reserved. No access is allowed.

Table 4.7 SFR Information for R8C/LA5A Group (7) ⁽¹⁾

Address	Register	Symbol	After Reset
0180h	Timer RJ Pin Select Register	TRJSR	00h
0181h			
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUICSR	00h
018Dh	Timer RH Second Interrupt Control Register	TRHICR	X0XXXXXXb 00000001b ⁽³⁾
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H ⁽²⁾	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register ⁽²⁾	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H ⁽²⁾	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 ⁽²⁾	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register ⁽²⁾	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register ⁽²⁾	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register ⁽²⁾	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	000000X0b
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.
- This is the reset value after reset by RTCRST bit in TRHCR register.

Table 4.8 SFR Information for R8C/LA5A Group (8) ⁽¹⁾

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h			
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h			
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h			
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h	Port P8 Pull-Up Control Register	P8PUR	00h
01E9h	Port P9 Pull-Up Control Register	P9PUR	00h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h	Port P8 Drive Capacity Control Register	P8DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.9 SFR Information for R8C/LA5A Group (9) ⁽¹⁾

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h			
0202h	LCD Option Clock Control Register	LCR2	00h
0203h	LCD Clock Control Register	LCR3	00h
0204h	LCD Display Control Register	LCR4	00h
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h			
020Ah			
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch			
020Dh			
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
:			
2FFFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.18 SFR Information for R8C/LA8A Group (9) ⁽¹⁾

Address	Register	Symbol	After Reset
0200h	LCD Control Register	LCR0	00h
0201h			
0202h	LCD Option Clock Control Register	LCR2	00h
0203h	LCD Clock Control Register	LCR3	00h
0204h	LCD Display Control Register	LCR4	00h
0205h			
0206h	LCD Port Select Register 0	LSE0	00h
0207h	LCD Port Select Register 1	LSE1	00h
0208h	LCD Port Select Register 2	LSE2	00h
0209h	LCD Port Select Register 3	LSE3	00h
020Ah	LCD Port Select Register 4	LSE4	00h
020Bh	LCD Port Select Register 5	LSE5	00h
020Ch			
020Dh			
020Eh			
020Fh			
0210h	LCD Display Data Register	LRA0L	XXh
0211h		LRA1L	XXh
0212h		LRA2L	XXh
0213h		LRA3L	XXh
0214h		LRA4L	XXh
0215h		LRA5L	XXh
0216h		LRA6L	XXh
0217h		LRA7L	XXh
0218h		LRA8L	XXh
0219h		LRA9L	XXh
021Ah		LRA10L	XXh
021Bh		LRA11L	XXh
021Ch		LRA12L	XXh
021Dh		LRA13L	XXh
021Eh		LRA14L	XXh
021Fh		LRA15L	XXh
0220h		LRA16L	XXh
0221h		LRA17L	XXh
0222h		LRA18L	XXh
0223h		LRA19L	XXh
0224h		LRA20L	XXh
0225h		LRA21L	XXh
0226h		LRA22L	XXh
0227h		LRA23L	XXh
0228h		LRA24L	XXh
0229h		LRA25L	XXh
022Ah		LRA26L	XXh
022Bh		LRA27L	XXh
022Ch		LRA28L	XXh
022Dh		LRA29L	XXh
022Eh		LRA30L	XXh
022Fh		LRA31L	XXh
0230h		LRA32L	XXh
0231h		LRA33L	XXh
0232h		LRA34L	XXh
0233h		LRA35L	XXh
0234h		LRA36L	XXh
0235h		LRA37L	XXh
0236h		LRA38L	XXh
0237h		LRA39L	XXh
:			
2FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.19 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
FFDFh	ID1		(Note 2)
FFE3h	ID2		(Note 2)
FFEBh	ID3		(Note 2)
FFEFh	ID4		(Note 2)
FFF3h	ID5		(Note 2)
FFF7h	ID6		(Note 2)
FFFBh	ID7		(Note 2)
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

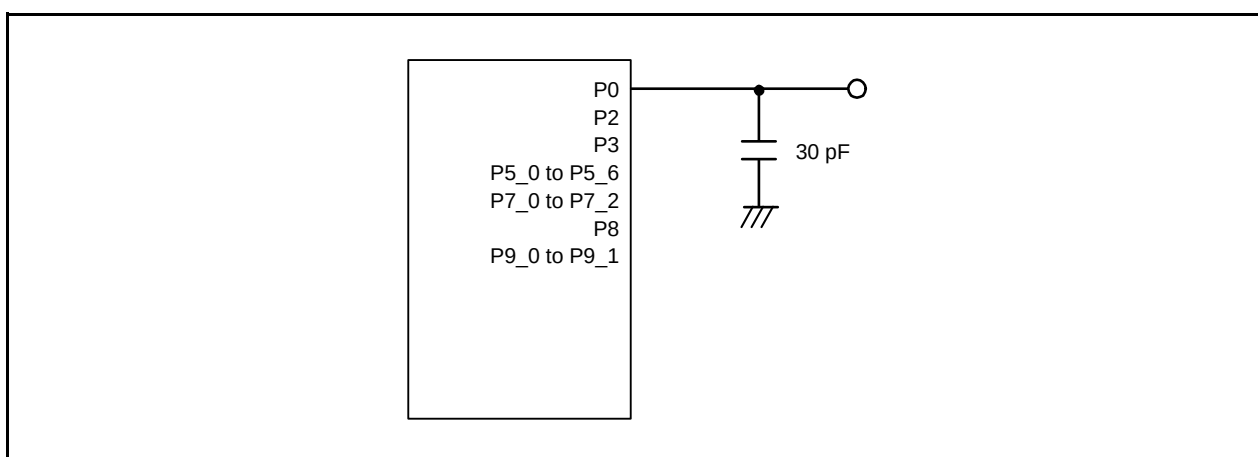


Figure 5.1 Ports P0, P2, P3, P5_0 to P5_6, P7_0 to P7_2, P8, and P9_0 to P9_1 Timing Measurement Circuit

5.1.3 Peripheral Function Characteristics

Table 5.3 A/D Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85 °C (N version)/
 -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy ⁽²⁾	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN6 input	—	—	±3	LSB
			Vref = AVCC = 2.2 V	AN0 to AN6 input	—	—	±5	LSB
			Vref = AVCC = 1.8 V	AN0 to AN6 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN6 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN6 input	—	—	±2	LSB
			Vref = AVCC = 1.8 V	AN0 to AN6 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		1	—	20	MHz
			3.2 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		1	—	16	MHz
			2.7 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		1	—	10	MHz
			1.8 ≤ Vref = AVCC ≤ 5.5 V ⁽¹⁾		1	—	8	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	ms
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				1.8	—	AVCC	V
VIa	Analog input voltage ⁽³⁾				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Temperature Sensor Characteristics
($V_{SS} = 0$ V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless
otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{TMP}	Temperature sensor output voltage	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25 °C	550	600	650	mV
—	Temperature coefficient	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25 °C	—	-2.1	—	mV/°C
—	Start-up time	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	—	200	μ s
I_{TMP}	Operating current	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	100	—	μ A

Table 5.13 High-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8$ V to 5.5 V -20 °C $\leq T_{opr} \leq 85$ °C	19.2	20	20.8	MHz
		$V_{CC} = 1.8$ V to 5.5 V -40 °C $\leq T_{opr} \leq 85$ °C	19.0	20	21.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽¹⁾	$V_{CC} = 1.8$ V to 5.5 V -20 °C $\leq T_{opr} \leq 85$ °C	17.694	18.432	19.169	MHz
		$V_{CC} = 1.8$ V to 5.5 V -40 °C $\leq T_{opr} \leq 85$ °C	17.510	18.432	19.353	MHz
—	Oscillation stability time		—	5	30	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	530	—	μA

Note:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.14 Low-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	—	35	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	2	—	μA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time		—	—	35	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25$ °C	—	2	—	μA

Table 5.15 Power Supply Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = 25$ °C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{d(P-R)}	Time for internal power supply stabilization during power-on ⁽¹⁾		—	—	2000	μs

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.16 LCD Drive Control Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/
–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL3	2.2	–	5.5	V
VL2	VL2 voltage		VL1	–	VL3	V
VL1	VL1 voltage		1	–	VL2 (2)	V
f(FR)	Frame frequency		50	–	180	Hz
ILCD	LCD drive control circuit current		–	(1)	–	μA

Notes:

1. Refer to Table 5.19 DC Characteristics (2), Table 5.21 DC Characteristics (4), and Table 5.23 DC Characteristics (6).
2. The VL1 voltage should be VCC or below.

Table 5.17 Power-Off Mode Characteristics
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/
–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Power-off mode operating supply voltage		1.8	–	5.5	V

Table 5.28 Timing Requirements of Serial Interface
($V_{SS} = 0\text{ V}$ and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (CK)	CLK0 input cycle time	800	—	300	—	200	—	ns
t _w (CKH)	CLK0 input “H” width	400	—	150	—	100	—	ns
t _w (CKL)	CLK0 input “L” width	400	—	150	—	100	—	ns
t _d (C-Q)	TXD0 output delay time	—	200	—	80	—	50	ns
t _h (C-Q)	TXD0 hold time	0	—	0	—	0	—	ns
t _{su} (D-C)	RXD0 input setup time	150	—	70	—	50	—	ns
t _h (C-D)	RXD0 input hold time	90	—	90	—	90	—	ns

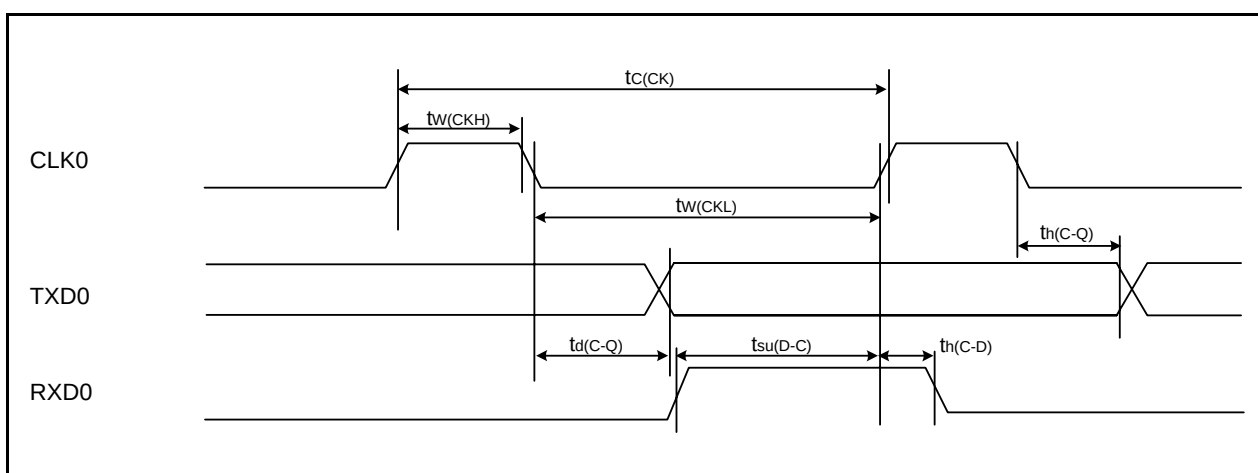


Figure 5.10 Input and Output Timing of Serial Interface

Table 5.29 Timing Requirements of External Interrupt $\overline{\text{INT}}i$ ($i = 0\text{ to }3, 5, 7$) and Key Input Interrupt $\overline{\text{KLI}}i$ ($i = 0\text{ to }7$)
($V_{SS} = 0\text{ V}$ and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2V, Topr = 25°C		Vcc = 3V, Topr = 25°C		Vcc = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
tw(INH)	$\overline{\text{INT}}i$ input "H" width, $\overline{\text{KLI}}i$ input "H" width	1000 ⁽¹⁾	—	380 ⁽¹⁾	—	250 ⁽¹⁾	—	ns
tw(INL)	$\overline{\text{INT}}i$ input "L" width, $\overline{\text{KLI}}i$ input "L" width	1000 ⁽²⁾	—	380 ⁽²⁾	—	250 ⁽²⁾	—	ns

Notes:

- When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input HIGH width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the $\overline{\text{INT}}i$ input filter select bit, use an $\overline{\text{INT}}i$ input LOW width of either (1/digital filter clock frequency $\times 3$) or the minimum value of standard, whichever is greater.

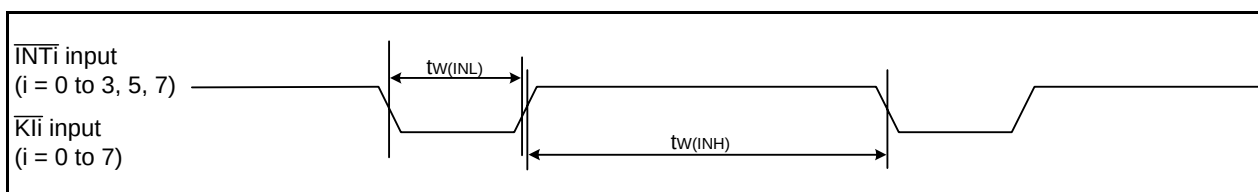


Figure 5.11 Input Timing of External Interrupt $\overline{\text{INT}}i$ and Key Input Interrupt $\overline{\text{KLI}}i$

5.2.3 Peripheral Function Characteristics

Table 5.32 A/D Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V _{ref} = AV _{CC}		—	—	10	Bit
—	Absolute accuracy ⁽²⁾	10-bit mode	V _{ref} = AV _{CC} = 5.0 V	AN0 to AN11 input	—	—	±3	LSB
			V _{ref} = AV _{CC} = 2.2 V	AN0 to AN11 input	—	—	±5	LSB
			V _{ref} = AV _{CC} = 1.8 V	AN0 to AN11 input	—	—	±5	LSB
		8-bit mode	V _{ref} = AV _{CC} = 5.0 V	AN0 to AN11 input	—	—	±2	LSB
			V _{ref} = AV _{CC} = 2.2 V	AN0 to AN11 input	—	—	±2	LSB
			V _{ref} = AV _{CC} = 1.8 V	AN0 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽¹⁾		1	—	20	MHz
			3.2 ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽¹⁾		1	—	16	MHz
			2.7 ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽¹⁾		1	—	10	MHz
			1.8 ≤ V _{ref} = AV _{CC} ≤ 5.5 V ⁽¹⁾		1	—	8	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	V _{ref} = AV _{CC} = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	V _{ref} = AV _{CC} = 5.0 V, φAD = 20 MHz		2.2	—	—	ms
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	V _{ref} current		V _{CC} = 5 V, XIN = f1 = φAD = 20 MHz		-	45	—	μA
V _{ref}	Reference voltage				1.8	—	AV _{CC}	V
VIA	Analog input voltage ⁽³⁾				0	—	V _{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.53	1.70	1.87	V

Notes:

1. The A/D conversion result will be undefined in wait mode, stop mode, power-off mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
2. This applies when the peripheral functions are stopped.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.33 Temperature Sensor Characteristics
($V_{SS} = 0$ V and $T_{opr} = -20$ to 85°C (N version)/ -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{TMP}	Temperature sensor output voltage	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25°C	550	600	650	mV
—	Temperature coefficient	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$ Ambient temperature = 25°C	—	-2.1	—	mV/ $^{\circ}\text{C}$
—	Start-up time	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	—	200	μs
I_{TMP}	Operating current	$1.8 \text{ V} \leq V_{ref} = AV_{CC} \leq 5.5 \text{ V}$ $\phi_{AD} = 1.0 \text{ MHz to } 5.0 \text{ MHz}$	—	100	—	μA

Table 5.48 DC Characteristics (2) [4.0 V ≤ V_{CC} ≤ 5.5 V]
(T_{opr} = −20 to 85°C (N version)/ −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition							Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max .	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	4.7	10	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	3.9	8	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	2.3	—	mA
			20 MHz	Off	Off	Off	No division	FMR27 = 1 MSTCR0 = BEh MSTCR1 = 3Fh	Flash memory off Program operation on RAM Module standby setting enabled	—	3.1	—	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.8	—	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.0	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—		—	5.0	11	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	—		—	2.1	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTCR0 = BEh MSTCR1 = 3Fh		—	0.9	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	No division	FMR27 = 1 VCA20 = 0		—	110	320	μA
			Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		—	63	220	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		—	60	220	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	—	46	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	—	9.0	50	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	—	2.8	33	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	—	4.6	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RH operation in real-time clock mode	—	2.4	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	While a WAIT instruction is executed Peripheral clock off	—	0.5	2.2	μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	0.5	2.2	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	1.2	—	μA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25°C	—	0.01	0.1	μA
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85°C	—	0.03	—	μA
Off	32 kHz		Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 25°C	—	1.8	6.4	μA		
Off	32 kHz		Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Power-off 2 Topr = 85°C	—	2.7	—	μA		

Notes:

1. V_{CC} = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are V_{SS}.
2. XIN is set to square wave input.
3. V_{CC} = 5.0 V
4. VLCD = V_{CC}, external division resistors are used for VL3 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG39 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.

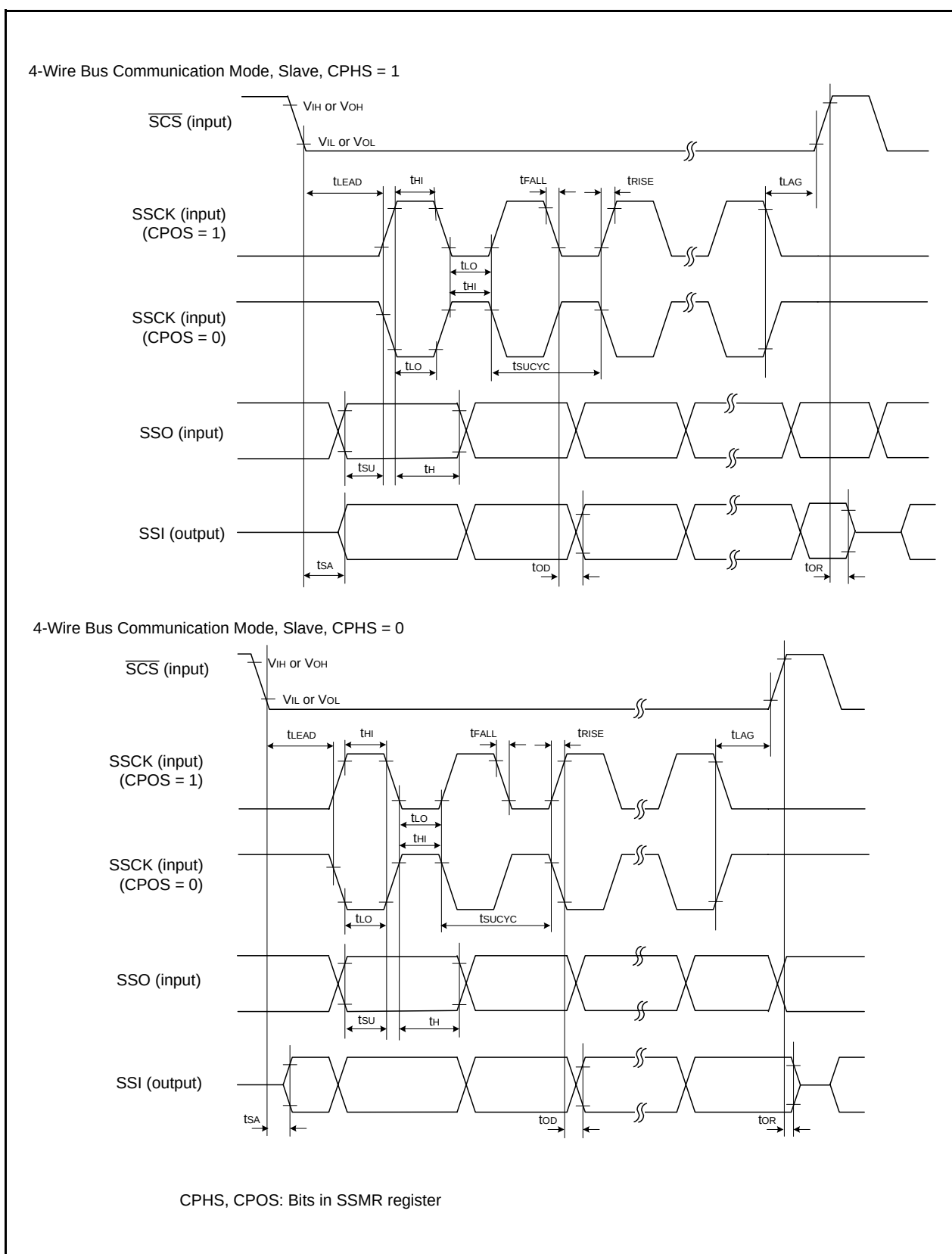


Figure 5.16 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

REVISION HISTORY

R8C/LA3A Group, R8C/LA5A Group, R8C/LA6A Group, R8C/LA8A Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Jan 18, 2010	—	First Edition issued
0.02	Jul 16, 2010	2	Table 1.1 revised
		3	Table 1.2 revised
		4	Tables 1.4 and 1.5 revised
		5	Table 1.6 revised
		6	Table 1.7 revised
		7	Table 1.8 revised
		8	Table 1.9 and Figure 1.1 revised
		9	Table 1.10 and Figure 1.2 revised
		10	Table 1.11 and Figure 1.3 revised
		11	Table 1.12 revised
		12	Figure 1.5 revised
		13	Figure 1.6 revised
		14	Figure 1.7 revised
		16	Figure 1.9 revised
		17	Figure 1.10 revised
		18	Table 1.13 revised
		19	Table 1.14 revised
		20	Figure 1.11 revised
		21	Figure 1.12 revised
		25	Table 1.18 revised
		26	Table 1.19 revised
		30	Figure 3.1 revised
		31	Table 4.1, Note 3 revised
		35	Table 4.5 revised
		41 to 44	Package Dimensions revised
1.00	Dec 21, 2010	All	“Preliminary” and “Under development” deleted
		2	Table 1.1 revised
		3	Tables 1.2 and 1.3 Note 2 revised
		4	Tables 1.4 and 1.5 Note 1 revised
		6	Table 1.7 revised
		7	Table 1.8 revised
		10	Table 1.11 and Figure 1.3 revised
		12	Figure 1.5 revised
		13	Figure 1.6 revised
		14	Figure 1.7 revised
		15	Figure 1.8 revised
		16	Figure 1.9 revised
		18	Table 1.13 revised
		19	Table 1.14 revised
		20	Figure 1.11 revised
		22	Table 1.15 revised
		23	Table 1.16 revised
		24	Table 1.17 revised
		25, 26	Tables 1.18 and 1.19 Pin Functions for R8C/LA5A Group added