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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	CPU32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68340cag16e

The primary features of the MC68340, illustrated in Figure 1-1, are as follows:

- High Functional Integration on a Single Piece of Silicon
- CPU32—MC68020-Derived 32-Bit Central Processor Unit
  — Upward Object-Code Compatible with MC68000 and MC68010
  — Additional MC68020 Instructions and Addressing Modes
  — Unique Embedded Control Instructions
  — Fast Two-Clock Register Instructions—10,045 Dhrystones
- Two-Channel Low-Latency DMA Controller for High-Speed Memory Transfers
  — Single- or Dual-Address Transfers
  — 32-Bit Addresses and Counters
  — 8-, 16-, and 32-Bit Data Transfers
  — 50 Mbyte/Sec Sustained Transfers (12.5 Mbyte/Sec Memory-to-Memory)
- Two-Channel Universal Synchronous/Asynchronous Receiver/Transmitter (USART)
  — Baud Rate Generators
  — Modem Control
  — MC68681/MC2681 Compatible
  — 9.8 Mbits/Sec Maximum Transfer Rate
- Two Independent Counter/Timers
  — 16-Bit Counter
  — Up to 8-Bit Prescaler
  — Multimode Operation
  — 80-ns Resolution
- System Integration Module Incorporates Many Functions Typically Relegated to External PALs, TTL, and ASIC, such as:
  — System Configuration
  — System Protection
  — Chip Select and Wait State Generation
  — Clock Generation
  — Dynamic Bus Sizing
  — Up to 16 Discrete I/O Lines
  — External Bus Interface
  — Periodic Interrupt Timer
  — Interrupt Response
  — Bus Arbitration
  — IEEE 1149.1 Boundary Scan (JTAG)
  — Power-On Reset
- 32 Address Lines, 16 Data Lines
- Power Consumption Control
  — Static HCMOS Technology Reduces Power in Normal Operation
  — Low Voltage Operation at 3.3 V ±0.3 V (MC68340V only)
  — Programmable Clock Generator Throttles Frequency
  — Unused Peripherals Can Be Turned Off
  — LPSTOP Provides an Idle State for Lowest Standby Current
- 0–16.78 MHz or 0–25.16 MHz Operation
- 144-Pin Ceramic Quad Flat Pack (CQFP) or 145-Pin Plastic Pin Grid Array (PGA)

As a low voltage part, the MC68340V can operate with a 3.3-V power supply. MC68340 is used throughout this manual to refer to both the low voltage and standard 5-V parts since both are functionally equivalent.

1.1 M68300 FAMILY

The MC68340 is one of a series of components in the M68300 family. Other members of the family include the MC68302, MC68330, MC68331, MC68332, and MC68333.

1.7 MORE INFORMATION

The following table lists available documentation related to the MC68340:

Document Number	Document Name
BR1114/D	*M68300 Integrated Processor Family*
MC68340/D	*MC68340 Technical Summary*
MC68340UM/AD	*MC68340 User's Manual*
M68000PM/AD	*M68000 Family Programmer's Reference Manual*
AN1063/D	*DRAM Controller for the MC68340*
AN453	*Software Implementation of SPI on the MC68340*
BR573/D	*M68340 Evaluation System Product Brief*
BR729/D	*The 68K Source*
BR1407/D	*3.3 Volt Logic and Interface Circuits*

Port B4, B2, B1, AVEC

This signal group functions as three bits of parallel I/O and the autovector input. AVEC requests an automatic vector during an interrupt acknowledge cycle.

2.6 INTERRUPT REQUEST LEVEL (IRQ7, IRQ6, IRQ5, IRQ3)

These pins can be programmed to be either prioritized interrupt request lines or port B parallel I/O.

IRQ7, IRQ6, IRQ5, IRQ3

IRQ7, the highest priority, is nonmaskable. IRQ6–IRQ1 are internally maskable interrupts. Refer to **Section 5 CPU32** for more information on interrupt request lines.

Port B7, B6, B5, B3

These pins can be used as port B parallel I/O. Refer to **Section 4 System Integration Module** for more information on parallel I/O signals.

2.7 BUS CONTROL SIGNALS

These signals control the bus transfer operations of the MC68340. Refer to **Section 3 Bus Operation** for more information on these signals.

2.7.1 Data and Size Acknowledge (DSACK1, DSACK0)

These two active-low input signals allow asynchronous data transfers and dynamic data bus sizing between the MC68340 and external devices as listed in Table 2-3. During bus cycles, external devices assert DSACK1 and/or DSACK0 as part of the bus protocol. During a read cycle, this signals the MC68340 to terminate the bus cycle and to latch the data. During a write cycle, this indicates that the external device has successfully stored the data and that the cycle may terminate.

Table 2-3. DSACK≈ Encoding

DSACK 1	DSACK 0	Result
1	1	Insert Wait States in Current Bus Cycle
1	0	Complete Cycle—Data Bus Port Size Is 8 Bits
0	1	Complete Cycle—Data Bus Port Size Is 16 Bits
0	0	Reserved—Defaults to 16-Bit Port Size Can Be Used for 32-Bit DMA Cycles

2.7.2 Address Strobe (AS)

AS is an output timing signal that indicates the validity of both an address on the address bus and many control signals. AS is asserted approximately one-half clock cycle after the beginning of a bus cycle.

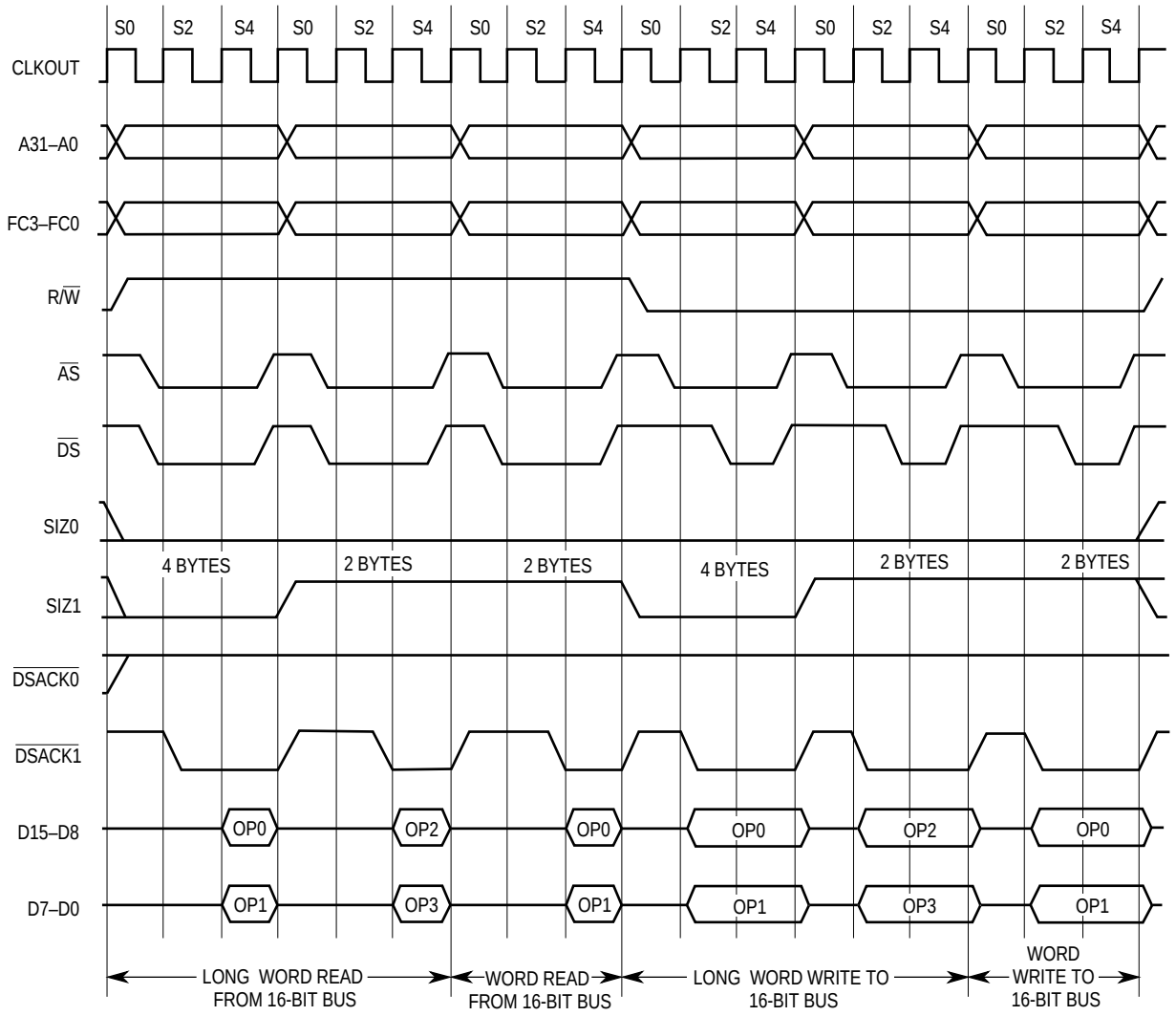


Figure 3-5. Long-Word and Word Read and Write Timing—16-Bit Port

The MC68340 drives the address bus with the desired address and drives the SIZx pins to indicate a long-word operand. For a read operation, the slave responds by placing the two most significant bytes of the operand on bits 15–0 of the data bus and asserting DSACK1 to indicate a 16-bit port. The MC68340 reads the two most significant bytes of the operand (bytes 0 and 1) from bits 15–0. The MC68340 then decrements the transfer size counter by 2, increments the address by 2, initiates a new cycle, and reads bytes 2 and 3 of the operand from bits 15–0 of the data bus.

For a write operation, the MC68340 drives the two most significant bytes of the operand on bits 15–0 of the data bus. The slave device then reads the two most significant bytes of the operand (bytes 0 and 1) from bits 15–0 of the data bus and asserts DSACK1 to indicate reception and a 16-bit port. The MC68340 then decrements the transfer size counter by 2, increments the address by 2, and writes bytes 2 and 3 of the operand to bits 15–0 of the data bus.

3.5 BUS EXCEPTION CONTROL CYCLES

The bus architecture requires assertion of DSACK≈ from an external device to signal that a bus cycle is complete. Neither DSACK≈ nor AVEC is asserted in the following cases:

- DSACK≈/AVEC is programmed to respond internally.
- The external device does not respond.
- Various other application-dependent errors occur.

The MC68340 provides BERR when no device responds by asserting DSACK≈/AVEC within an appropriate period of time after the MC68340 asserts AS. This mechanism allows the cycle to terminate and the MC68340 to enter exception processing for the error condition. HALT is also used for bus exception control. This signal can be asserted by an external device for debugging purposes to cause single bus cycle operation, or, in combination with BERR, a retry of a bus cycle in error. To properly control termination of a bus cycle for a retry or a bus error condition, DSACK≈, BERR, and HALT can be asserted and negated with the rising edge of the MC68340 clock. This assures that when two signals are asserted simultaneously, the required setup and hold time for both is met for the same falling edge of the MC68340 clock. This or an equivalent precaution should be designed into the external circuitry to provide these signals. Alternatively, the internal bus monitor could be used. The acceptable bus cycle terminations for asynchronous cycles are summarized in relation to DSACK≈ assertion as follows (case numbers refer to Table 3-4):

- Normal Termination: DSACK≈ is asserted; BERR and HALT remain negated (case 1).
- Halt Termination: HALT is asserted at the same time as or before DSACKx, and BERR remains negated (case 2).
- Bus Error Termination: BERR is asserted in lieu of, at the same time as, or before DSACK≈ (case 3) or after DSACK≈ (case 4), and HALT remains negated; BERR is negated at the same time as or after DSACK≈.
- Retry Termination: HALT and BERR are asserted in lieu of, at the same time as, or before DSACK≈ (case 5) or after DSACK≈ (case 6); BERR is negated at the same time as or after DSACK≈, and HALT may be negated at the same time as or after BERR.

Table 3-4 lists various combinations of control signal sequences and the resulting bus cycle terminations. To ensure predictable operation, BERR and HALT should be negated according to the specifications given in **Section 11 Electrical Characteristics**. DSACK≈ BERR, and HALT may be negated after AS. If DSACK≈ or BERR remain asserted into S2 of the next bus cycle, that cycle may be terminated prematurely.

EXAMPLE A: A system uses a bus monitor timer to terminate accesses to an unpopulated address space. The timer asserts BERR after timeout (case 3).

State 0—During state 0, the A31–A0 and FCx become valid, R/W is driven to indicate a show read or write cycle, and the SIZx pins indicate the number of bytes to transfer. During a read, the addressed peripheral is driving the data bus, and the user must take care to avoid bus conflicts.

State 41—One-half clock cycle later, DS (rather than AS) is asserted to indicate that address information is valid.

State 42—No action occurs in state 42. The bus controller remains in state 42 (wait states will be inserted) until the internal read cycle is complete.

State 43—When DS is negated, show data is valid on the next falling edge of the system clock. The external data bus drivers are enabled so that data becomes valid on the external bus as soon as it is available on the internal bus.

State 0—The A31–A0, FCx, R/W, and SIZx pins change to begin the next cycle. Data from the preceding cycle is valid through state 0.

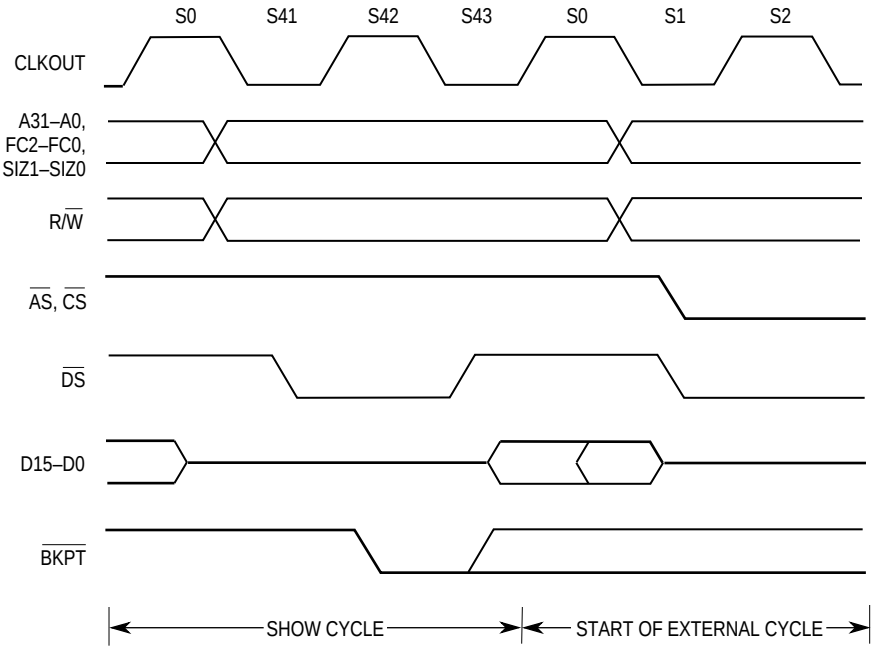


Figure 3-26. Show Cycle Timing Diagram

3.7 RESET OPERATION

The MC68340 has reset control logic to determine the cause of reset, synchronize it if necessary, and assert the appropriate reset lines. The reset control logic can independently drive three different lines:

1. EXTRST (external reset) drives the external RESET pin.
2. CLKRST (clock reset) resets the clock module.

4.3.1 Module Base Address Register (MBAR)

MBAR 1 $0003FF00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24	BA23	BA22	BA21	BA20	BA19	IBA18	BA17	BA16
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CPU Space Only

MBAR 2 $0003FF02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA15	BA14	BA13	BA12	0	0	AS8	AS7	AS6	AS5	AS4	AS3	AS2	AS1	AS0	V
RESET															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CPU Space Only

BA31–BA12—Base Address Bits 31–12

The base address field is the upper 20 bits of the MBAR that provides for block starting locations in increments of 4-Kbytes.

Bits 11, 10—Reserved

AS8–AS0—Address Space Bits 8–0

The address space field allows particular address spaces to be masked, placing the 4K module block into a particular address space(s). If an address space is masked, an access to the register block location in that address space becomes an external access. The module block is not accessed. The address space bits are as follows:

AS8—mask DMA Space	address space (FC3–FC0 = 1xxx)
AS7—mask CPU Space	address space (FC3–FC0 = 0111)
AS6—mask Supervisor Program	address space (FC3–FC0 = 0110)
AS5—mask Supervisor Data	address space (FC3–FC0 = 0101)
AS4—mask Reserved [Motorola]	address space (FC3–FC0 = 0100)
AS3—mask Reserved [User]	address space (FC3–FC0 = 0011)
AS2—mask User Program	address space (FC3–FC0 = 0010)
AS1—mask User Data	address space (FC3–FC0 = 0001)
AS0—mask Reserved [Motorola]	address space (FC3–FC0 = 0000)

For each address space bit:

1 = Mask this address space from the internal module selection. The bus cycle goes external.
0 = Decode for the internal module block.

V—Valid Bit

This bit indicates when the contents of the MBAR are valid. The base address value is not used; therefore, all internal module registers are not accessible until the V-bit is set.

1 = Contents are valid.
0 = Contents are not valid.

5.2 ARCHITECTURE SUMMARY

The CPU32 is upward source- and object-code compatible with the MC68000 and MC68010. It is downward source- and object-code compatible with the MC68020. Within the M68000 family, architectural differences are limited to the supervisory operating state. User state programs can be executed unchanged on upward-compatible devices.

The major CPU32 features are as follows:

- 32-Bit Internal Data Path and Arithmetic Hardware
- 32-Bit Address Bus Supported by 32-Bit Calculations
- Rich Instruction Set
- Eight 32-Bit General-Purpose Data Registers
- Seven 32-Bit General-Purpose Address Registers
- Separate User and Supervisor Stack Pointers
- Separate User and Supervisor State Address Spaces
- Separate Program and Data Address Spaces
- Many Data Types
- Flexible Addressing Modes
- Full Interrupt Processing
- Expansion Capability

5.2.1 Programming Model

The CPU32 programming model consists of two groups of registers that correspond to the user and supervisor privilege levels. User programs can only use the registers of the user model. The supervisor programming model, which supplements the user programming model, is used by CPU32 system programmers who wish to protect sensitive operating system functions. The supervisor model is identical to that of MC68010 and later processors.

The CPU32 has eight 32-bit data registers, seven 32-bit address registers, a 32-bit PC, separate 32-bit SSP and USP, a 16-bit SR, two alternate function code registers, and a 32-bit VBR (see Figures 5-3 and 5-4).

Table 5-14. Compressed Table Entries

Entry Number	X Value	Y Value
2	512	1311
3	786	1966

Since the table is reduced from 257 to 5 entries, independent variable X must be scaled appropriately. In this case the scaling factor is 64, and the scaling is done by a single instruction:

LSR.W #6,Dx

Thus, Dx now contains the following bit pattern:

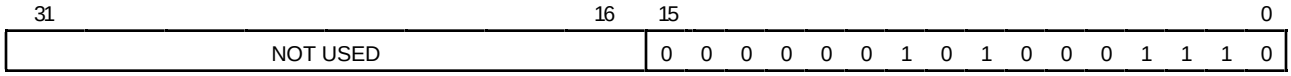


Table Entry Offset ⇒ Dx [8:15] = $02 = 2

Interpolation Fraction ⇒ Dx [0:7] = $8E = 142

Using this information, the table instruction calculates dependent variable Y:

Y = 1331 + (142 (1966 – 1311)) / 256 = 1674

The function chosen for Examples 1 and 2 is linear between data points. If another function had been been used, interpolated values might not have been identical.

5.3.4.3 TABLE EXAMPLE 3: 8-BIT INDEPENDENT VARIABLE. This example shows how to use a table instruction within an interpolation subroutine. Independent variable X is calculated as an 8-bit value, allowing 16 levels of interpolation on a 17-entry table. X is passed to the subroutine, which returns an 8-bit result. The subroutine uses the data listed in Table 5-15, based on the function shown in Figure 5-9.

Bus operation in progress at the time of a fault is conveyed by the SSW.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TP	MV	0	TR	B1	B0	RR	RM	IN	RW	LG	SIZ		FUNC		

The bus error stack frame is 12 words in length. There are three variations of the frame, each distinguished by different values in the SSW TP and MV fields.

An internal transfer count register appears at location SP + $14 in all bus error stack frames. The register contains an 8-bit microcode revision number, and, for type III faults, an 8-bit transfer count. Register format is shown in Figure 5-14.

15	8	7	0
MICROCODE REVISION NUMBER		TRANSFER COUNT	

Figure 5-14. Internal Transfer Count Register

The microcode revision number is checked before a bus error stack frame is restored via RTE. In a multiprocessor system, this check ensures that a processor using stacked information is at the same revision level as the processor that created it.

The transfer count is ignored unless the MV bit in the stacked SSW is set. If the MV bit is set, the least significant byte of the internal register is reloaded into the MOVEM transfer counter during RTE execution.

For faults occurring during normal instruction execution (both prefetches and non-MOVEM operand accesses) SSW TP, MV = 00. Stack frame format is shown in Figure 5-15.

Faults that occur during the operand portion of the MOVEM instruction are identified by SSW TP, MV = 01. Stack frame format is shown in Figure 5-16.

When a bus error occurs during exception processing, SSW TP, MV = 10. The frame shown in Figure 5-17 is written below the faulting frame. Stacking begins at the address pointed to by SP – 6 (SP value is the value before initial stacking on the faulted frame).

The frame can have either four or six words, depending on the type of error. Four-word stack frames do not include the faulted instruction PC (the internal transfer count register is located at SP + $10 and the SSW is located at SP + $12).

The fault address of a dynamically sized bus cycle is the address of the upper byte, regardless of the byte that caused the error.

DSCLK, the gated serial clock, is normally high, but it pulses low for each bit to be transferred. At the end of the seventeenth clock period, it remains high until the start of the next transmission. Clock frequency is implementation dependent and may range from DC to the maximum specified frequency. Although performance considerations might dictate a hardware implementation, software solutions can be used provided serial bus timing is maintained.

5.6.2.8 COMMAND SET. The following paragraphs describe the command set available in BDM.

5.6.2.8.1 Command Format. The following standard bit format is utilized by all BDM commands.

15 — 10	9	8	7 — 6	5	4	3	2 — 0
OPERATION	0	R/W	OP SIZE	0	0	A/D	REGISTER
EXTENSION WORD(S)							

Bits 15–0—Operation Field

The operation field specifies the commands. This 6-bit field provides for a maximum of 64 unique commands.

R/W Field

The R/W field specifies the direction of operand transfer. When the bit is set, the transfer is from CPU to development system. When the bit is cleared, data is written to the CPU or to memory from the development system.

Operand Size

For sized operations, this field specifies the operand data size. All addresses are expressed as 32-bit absolute values. The size field is encoded as listed in Table 5-22.

Table 5-22. Size Field Encoding

Encoding	Operand Size
00	Byte
01	Word
10	Long
11	Reserved

Address/Data (A/D) Field

The A/D field is used by commands that operate on address and data registers. It determines whether the register field specifies a data or address register. One indicates an address register; zero indicates a data register. For other commands, this field may be interpreted differently.

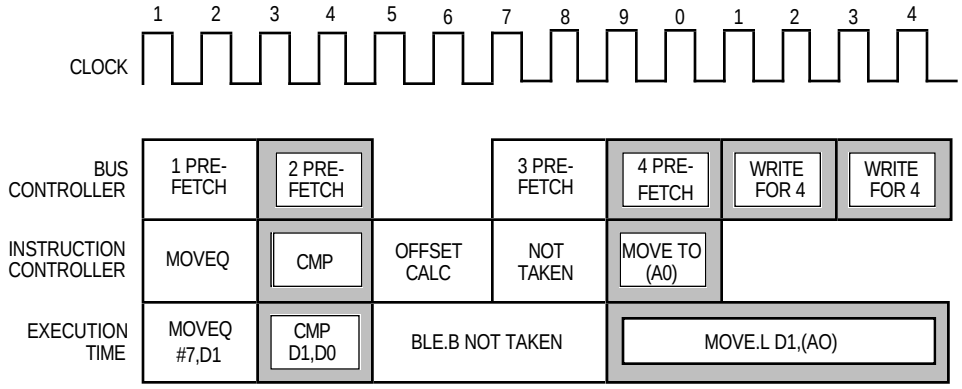


Figure 5-35. Example 2—Branch Not Taken

5.7.2.3 TIMING EXAMPLE 3—NEGATIVE TAILS. This example (see Figure 5-36) shows how to use negative tail figures for branches and other change-of-flow instructions. In this example, bus speed is assumed to be four clocks per access. Instruction three is at the branch destination.

Although the CPU32 has a two-word instruction pipeline, internal delay causes minimum branch instruction time to be three bus cycles. The negative tail is a reminder that an extra two clocks are available for prefetching a third word on a fast bus; on a slower bus, there is no extra time for the third word.

Instructions

MOVEQ	#7, D1
BRA.W	FARAWAY
MOVE.L	D1, D0

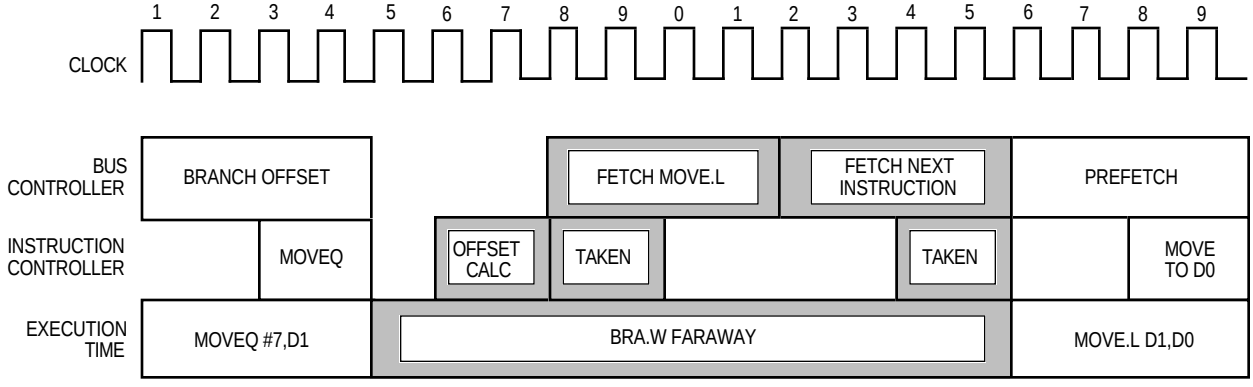


Figure 5-36. Example 3—Branch Negative Tail

S/D—Single-/Dual-Address Transfer

1 = The DMA channel runs single-address transfers from a peripheral to memory or from memory to a peripheral. The destination holding register is not used for these transfers because the data is transferred directly into the destination location. The MC68340 on-chip peripherals do not support single-address transfers.
0 = The DMA channel runs dual-address transfers.

STR—Start

This bit is cleared by a hardware/software reset, writing a logic zero, or setting one of the following CSR bits: DONE, BES, BED, CONF, or BRKP. The STR bit cannot be set when the CSR IRQ bit is set. The DMA channel cannot be started until the CSR DONE, BES, BED, CONF, and BRKP bits are cleared.

Internal Request Mode:

1 = The DMA transfer starts as soon as this bit is set.
0 = The DMA transfer can be stopped by clearing this bit.

External Request Mode:

1 = Setting this bit allows the DMA to start the transfer when a DREQ≈ input is received from an external device.
0 = The DMA transfer can be stopped by clearing this bit.

NOTE

If any fields in the CCR are modified while the channel is active, that change is effective immediately. To avoid any problems with changing the setup for the DMA channel, a zero should be written to the STR bit in the CCR to halt the DMA channel at the end of the current bus cycle.

6.7.4 Channel Status Register (CSR)

The CSR contains the channel status information. This register is accessible in either supervisor or user space. The CSR can always be read or written to when the DMA module is enabled (i.e., the STP bit in the MCR is cleared).

CSR1, CSR2 $78A, $7AA

7	6	5	4	3	2	1	0
IRQ	DONE	BES	BED	CONF	BRKP	0	0
RESET 0	0	0	0	0	0	0	0

Supervisor/User

IRQ—Interrupt Request

This bit is the logical OR of the DONE, BES, BED, CONF, and BRKP bits and is cleared when they are all cleared. IRQ is positioned to allow conditional testing as a signed binary integer. The state of this bit is not affected by the interrupt enable bits in the CCR. The STR bit in the CCR cannot be set when this bit is set; all error status bits, except the BRKP bit, must be cleared before the STR bit can be set.

1 = An interrupt condition has occurred.
0 = An interrupt condition has not occurred.

DONE—DMA Done

1 = The DMA channel has terminated normally.
0 = The DMA channel has not terminated normally. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

BES—Bus Error on Source

1 = The DMA channel has terminated with a bus error during the read bus cycle.
0 = The DMA channel has not terminated with a bus error during the read bus cycle. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

BED—Bus Error on Destination

1 = The DMA channel has terminated with a bus error during the write bus cycle.
0 = The DMA channel has not terminated with a bus error during the write bus cycle. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

CONF—Configuration Error

A configuration error results when either the SAR or the DAR contains an address that does not match the port size specified in the CCR and the BTC register does not match the larger port size or is zero.

1 = The CCR STR bit is set, and a configuration error is present.
0 = The CCR STR bit is set, and no configuration error exists. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

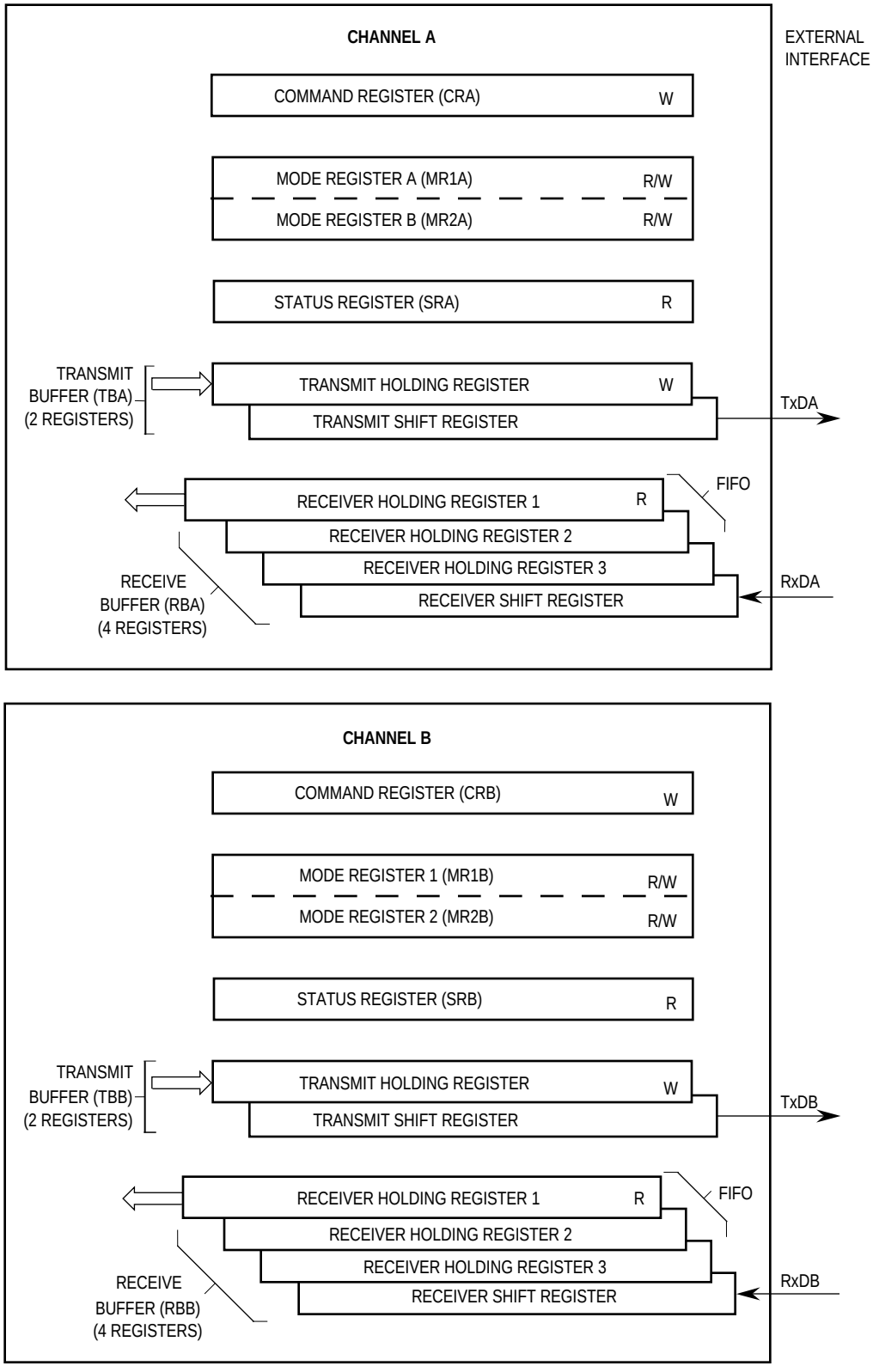
BRKP—Breakpoint

1 = The breakpoint signal was set during a DMA transfer.
0 = The breakpoint signal was not set during a DMA transfer. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

Bits 1, 0—Reserved

NOTE

The CSR is cleared by writing $7C to its location. The DMA channel cannot be started until the CSR DONE, BES, BED, CONF and BRKP bits are cleared.



NOTE:
R/W = READ/WRITE
R = READ
W = WRITE

Figure 7-4. Transmitter and Receiver Functional Diagram

OE—Overrun Error

1 = One or more characters in the received data stream have been lost. This bit is set upon receipt of a new character when the FIFO is full and a character is already in the shift register waiting for an empty FIFO position. When this occurs, the character in the receiver shift register and its break detect, framing error status, and parity error, if any, are lost. This bit is cleared by the reset error status command in the CR.

0 = No overrun has occurred.

TxEMP—Transmitter Empty

1 = The channel transmitter has underrun (both the transmitter holding register and transmitter shift registers are empty). This bit is set after transmission of the last stop bit of a character if there are no characters in the transmitter holding register awaiting transmission.

0 = The transmitter buffer is not empty. The transmitter holding register is loaded by the CPU32, or the transmitter is disabled. The transmitter is enabled/disabled by programming the TCx bits in the CR.

TxRDY—Transmitter Ready

This bit is duplicated in the ISR; bit 0 for channel A and bit 4 for channel B.

1 = The transmitter holding register is empty and ready to be loaded with a character. This bit is set when the character is transferred to the transmitter shift register. This bit is also set when the transmitter is first enabled. Characters loaded into the transmitter holding register while the transmitter is disabled are not transmitted and are lost.

0 = The transmitter holding register was loaded by the CPU32, or the transmitter is disabled.

FFULL—FIFO Full

1 = A character was transferred from the receiver shift register to the receiver FIFO and the transfer caused the FIFO to become full (all three FIFO holding register positions are occupied).

0 = The CPU32 has read the receiver buffer and one or more FIFO positions are available. Note that if there is a character in the receiver shift register because the FIFO is full, this character will be moved into the FIFO when a position is available, and the FIFO will remain full.

RxRDY—Receiver Ready

1 = A character has been received and is waiting in the FIFO to be read by the CPU32. This bit is set when a character is transferred from the receiver shift register to the FIFO.

0 = The CPU32 has read the receiver buffer, and no characters remain in the FIFO after this read.

SECTION 9
IEEE 1149.1 TEST ACCESS PORT

The MC68340 includes dedicated user-accessible test logic that is fully compatible with the *IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture*. Problems associated with testing high-density circuit boards have led to development of this proposed standard under the sponsorship of the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The MC68340 implementation supports circuit-board test strategies based on this standard.

The test logic includes a test access port (TAP) consisting of four dedicated signal pins, a 16-state controller, an instruction register, and two test data registers. A boundary scan register links all device signal pins into a single shift register. The test logic, implemented using static logic design, is independent of the device system logic. The MC68340 implementation provides the following capabilities:

a. Perform boundary scan operations to test circuit-board electrical continuity
b. Sample the MC68340 system pins during operation and transparently shift out the result in the boundary scan register
c. Bypass the MC68340 for a given circuit-board test by effectively reducing the boundary scan register to a single bit
d. Disable the output drive to pins during circuit-board testing

NOTE

Certain precautions must be observed to ensure that the IEEE 1149.1 test logic does not interfere with nontest operation. See **9.6 Non-IEEE 1149.1 Operation** for details.

9.1 OVERVIEW

NOTE

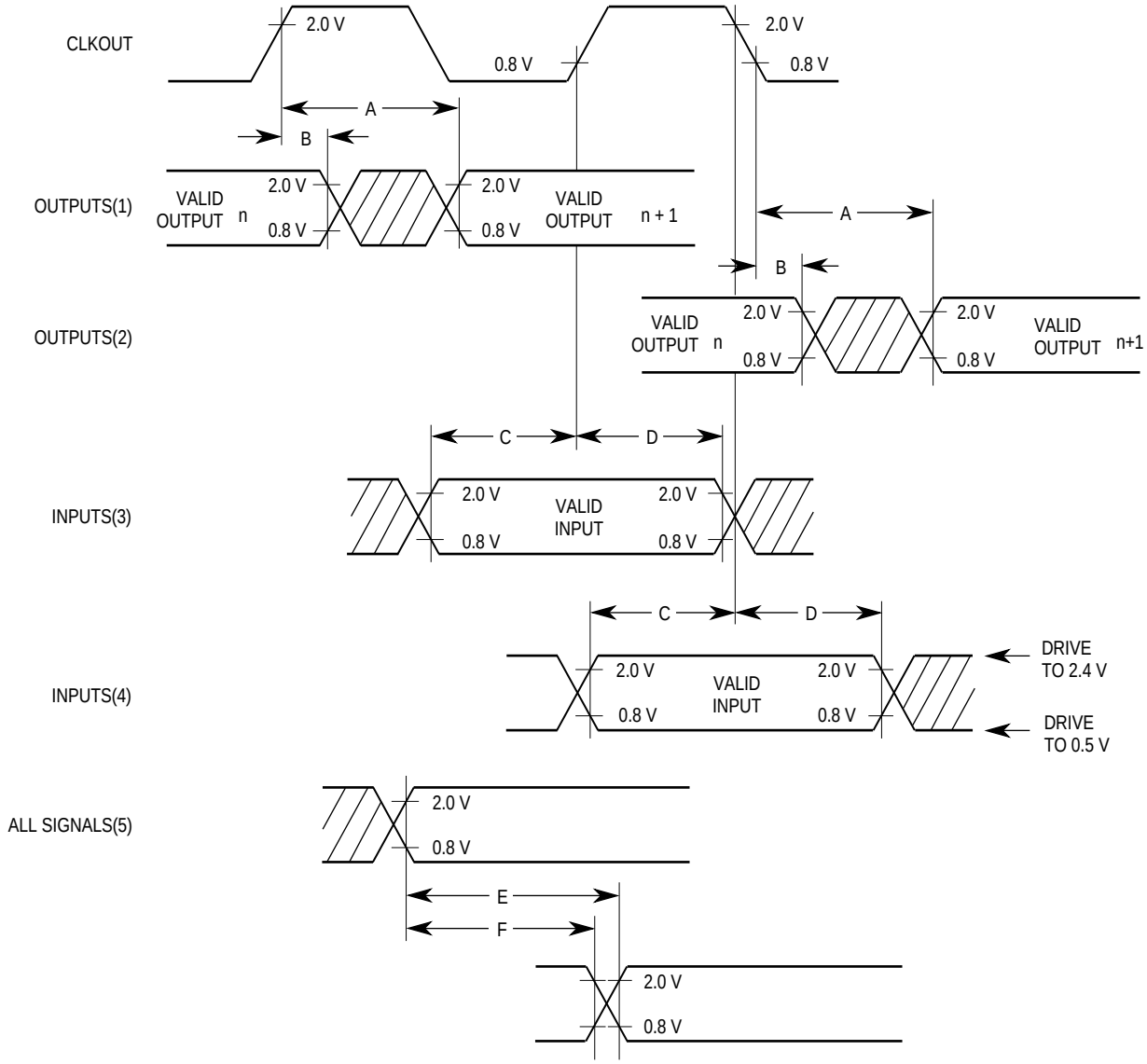
This description is not intended to be used without the supporting IEEE 1149.1 document.

The discussion includes those items required by the standard and provides additional information specific to the MC68340 implementation. For internal details and applications of the standard, refer to the IEEE 1149.1 document.

The MC68340V low voltage parts can operate up to 8.39 MHz or 16.78 MHz with a 3.3 V ±0.3 V supply. Separate part numbers are used to distinguish the operation of the parts according to the supply voltage. Refer to **Section 12 Ordering Information and Mechanical Data** for the part numbering schemes. MC68340 is used throughout this section to refer to the 16.78- or 25.16-MHz parts at 5.0 V ±5%. MC68340V is used throughout this section to refer to the 8.39- or 16.78-MHz parts at 3.3 V ±0.3 V.

NOTE

The electrical specifications in this section for the MC68340 25.16 MHz at 5.0 V ±5% and the 3.3 V ±0.3 V specifications for both the 8.39- and 16.78-MHz parts are preliminary.



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 11-1. Drive Levels and Test Points for AC Specifications

11.7 AC TIMING SPECIFICATIONS (Continued)

Num.	Characteristic	Symbol	3.3 V 8.39 MHz Min	3.3 V 8.39 MHz Max	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
30[4]	CLKOUT Low to Data-In Invalid (Fast Termination Hold)	t_{CLDI}	30	—	15	—	10	—	ns
30A[4]	CLKOUT Low to Data-In High Impendance	t_{CLDH}	—	180	—	90	—	60	ns
31[5]	DSACK≈ Asserted to Data-In Valid	t_{DADI}	—	100	—	50	—	32	ns
31A	DSACK≈ Asserted to DSACK≈ Valid (Skew)	t_{DADV}	—	60	—	30	—	20	ns
32	HALT and RESET Input Transition Time	t_{HRrf}	—	400	—	200	—	140	ns
33	CLKOUT Low to BG Asserted	t_{CLBA}	—	60	—	30	—	20	ns
34	CLKOUT Low to BG Negated	t_{CLBN}	—	60	—	30	—	20	ns
35[6]	BR Asserted to BG Asserted (RMC Not Asserted)	t_{BRAGA}	1	—	1	—	1	—	CLKOUT
37	BGACK Asserted to BG Negated	t_{GAGN}	1	2.5	1	2.5	1	2.5	CLKOUT
39	BG Width Negated	t_{GH}	2	—	2	—	2	—	CLKOUT
39A	BG Width Asserted	t_{GA}	1	—	1	—	1	—	CLKOUT
46	R/W Width Asserted (Write or Read)	t_{RWA}	300	—	150	—	100	—	ns
46A	R/W Width Asserted (Fast Termination Write or Read)	t_{RWAS}	180	—	90	—	60	—	ns
47A[8]	Asynchronous Input Setup Time	t_{AIST}	15	—	8, 5	—	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	30	—	15	—	10	—	ns
48[5,7]	DSACK≈ Asserted to BERR, HALT Asserted	t_{DABA}	—	60	—	30	—	20	ns
53	Data-Out Hold from CLKOUT High	t_{DOCH}	0	—	0	—	0	—	ns
54	CLKOUT High to Data-Out High Impedance	t_{CHDH}	—	60	—	30	—	20	ns
55	R/W Asserted to Data Bus Impedance Change	t_{RADC}	80	—	40	—	25	—	ns
56	RESET Pulse Width (Reset Instruction)	t_{HRPW}	512	—	512	—	512	—	CLKOUT
56A	RESET Pulse Width (Input from External Device)	t_{RPWI}	590	—	590	—	590	—	CLKOUT
57	BERR Negated to HALT Negated (Rerun)	t_{BNHN}	0	—	0	—	0	—	ns
70	CLKOUT Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	60	0	30	0	20	ns
71	Data Setup Time to CLKOUT Low (Show Cycle)	t_{SCLDS}	30	—	15	—	10	—	ns
72	Data Hold from CLKOUT Low (Show Cycle)	t_{SCLDH}	20	—	10	—	6	—	ns
80	DSI Input Setup Time	t_{DSISU}	30	—	15	—	10	—	ns
81	DSI Input Hold Time	t_{DSIH}	20	—	10	—	6	—	ns
82	DSCLK Setup Time	t_{DSCSU}	30	—	15	—	10	—	ns
83	DSCLK Hold Time	t_{DSCH}	20	—	10	—	6	—	ns
84	DSO Delay Time	t_{DSOD}	—	t_{cyc} + 50	—	t_{cyc} + 25	—	t_{cyc} + 16	ns