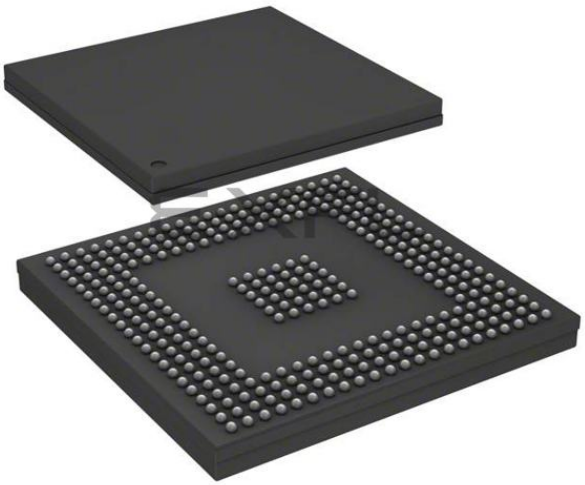

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70b4cfar

- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 System integration unit (SIU)

The SPC564A70 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin

2.2 LBGA208 ballmap[b]

Figure 3. 208-pin LBGA package ballmap (viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_SOUT	DSPI_B_PCS[3]	DSPI_B_SIN	DSPI_B_PCS[0]	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO[99]	DSPI_B_PCS[4]	DSPI_B_PCS[2]	DSPI_B_PCS[1]	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_PCS[5]	SCI_A_TX	GPIO[98]	DSPI_B_SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ETPUA19_O	VRC33	VSS	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO[207]	NC	EMIOS6	EMIOS8	MDO11_ETPUA29_O	MDO4_ETPUA2_O	MDO8_ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P

b. LBGA208 is available upon specific request. Please contact your ST sales office for details.

VSS	VSS	VSS					DSPI_A_ PCS[1]	DSPI_A_ PCS[0]	GPIO[98]	VDDREG	M
VSS	VSS	VSS					DSPI_A_ PCS[4]	SCI_A_TX	DSPI_A_ PCS[5]	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							WKPCFG	CAN_C_RX	SCI_B_TX	RESET	R
							SCI_B_RX	BOOTCFG1	VSS	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG0	EXTAL	U
							VDD	VRCCTL	PLLREF	XTAL	V
EMIOS2	EMIOS8	VDDEH4AB	EMIOS12	EMIOS21	VDDE12	SCI_C_TX	VSS	VDD	NC	VDDPLL	W
EMIOS6	EMIOS10	EMIOS15	EMIOS17	EMIOS22	CAN_A_TX	VDDE12	SCI_C_RX	VSS	VDD	VRC33	Y
EMIOS5	EMIOS9	EMIOS13	EMIOS16	EMIOS19	EMIOS23	CAN_A_RX	VDDE12	CLKOUT	VSS	VDD	AA
EMIOS4	EMIOS7	EMIOS11	EMIOS14	EMIOS18	EMIOS20	CAN_B_TX	CAN_B_RX	VDDE12	ENGCLK	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

Figure 7. 324-pin PBGA package ballmap (southeast, viewed from above)

2.4 Signal summary

Table 4. SPC564A70 signal properties

Name[1]	Function[2]	P / A / G[3]	PCR PA field (4)	PCR (5)	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
GPIO											
FR_A_TX GPIO[12]	FlexRay transmit data channel A GPIO	A1 G	010 000	12	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	P1
FR_A_TX_EN GPIO[13]	FlexRay ch. A tx data enable GPIO	A1 G	010 000	13	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	P2
FR_A_RX GPIO[14]	FlexRay receive data ch. A GPIO	A1 G	010 000	14	I I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	R1
FR_B_TX GPIO[15]	FlexRay transmit data ch. B GPIO	A1 G	010 000	15	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	R2
FR_B_TX_EN GPIO[16]	FlexRay tx data enable for ch. B GPIO	A1 G	010 000	16	O I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	T1
FR_B_RX GPIO[17]	FlexRay receive data channel B GPIO	A1 G	010 000	17	I I/O	VDDE-EH / Medium	— / Up	— / Up	—	—	T2
GPIO[206] ETRIG0	GPIO / eQADC Trigger Input	G	00	206	I/O[10]	VDDEH7 / Slow[11]	— / Up	— / Up	143	R4	AA7
GPIO[207] ETRIG1	GPIO / eQADC Trigger Input	G	00	207	I/O[10]	VDDEH7 / Slow	— / Up	— / Up	144	P5	Y9
GPIO[219]	GPIO	G	000	219 (12)	I/O	VDDEH7 / MultV	— / Up	— / Up	122	T6	—
Reset / Configuration											
$\overline{\text{RESET}}$	External Reset Input	P	—	—	I	VDDEH6 / Slow	$\overline{\text{RESET}}$ / Up	$\overline{\text{RESET}}$ / Up	97	L16	R22
$\overline{\text{RSTOUT}}$	External Reset Output	P	01	230	O	VDDEH6 / Slow	$\overline{\text{RSTOUT}}$ / Down	$\overline{\text{RSTOUT}}$ / Down	102	K15	P21
PLLREF IRQ[4] ETRIG2 GPIO[208]	FMPLL Mode Selection External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	208	I I I I/O	VDDEH6 / Slow	— / Up	PLLREF / Up	83	M14	V21

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
ETPUA4 ETPUA16_O — FR_B_TX GPIO[118]	eTPU A channel eTPU A channel (output only) — FlexRay transmit data channel B GPIO	P A1 A2 A3 G	0001 0010 — 1000 0000	118	I/O O — O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	56	N2	L1
ETPUA5 ETPUA17_O DSPI_B_SCK_LVDS– FR_B_TX_EN GPIO[119]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI clock FlexRay tx data enable for ch. B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	119	I/O O O O I/O	VDDEH4 / Slow + LVDS	— / WKPCFG	— / WKPCFG	54	M4	K4
ETPUA6 ETPUA18_O DSPI_B_SCK_LVDS+ FR_B_RX GPIO[120]	eTPU A channel eTPU A channel (output only) LVDS positive DSPI clock FlexRay receive data channel B GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	120	I/O O O I I/O	VDDEH4 / Medium + LVDS	— / WKPCFG	— / WKPCFG	53	L3	J3
ETPUA7 ETPUA19_O DSPI_B_SOUT_LVDS– ETPUA6_O GPIO[121]	eTPU A channel eTPU A channel (output only) LVDS negative DSPI data out eTPU A channel (output only) GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	121	I/O O O O I/O	VDDEH4 / Slow + LVDS	— / WKPCFG	— / WKPCFG	52	K3	K2
ETPUA8 ETPUA20_O DSPI_B_SOUT_LVDS+ GPIO[122]	eTPU A channel eTPU A channel (output only) LVDS positive DSPI data out GPIO	P A1 A2 G	001 010 100 000	122	I/O O O I/O	VDDEH4 / Slow + LVDS	— / WKPCFG	— / WKPCFG	51	N1	K1
ETPUA9 ETPUA21_O RCH1_B GPIO[123]	eTPU A channel eTPU A channel (output only) Reaction channel 1B GPIO	P A1 A2 G	001 010 100 000	123	I/O O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	50	M2	J4
ETPUA10 ETPUA22_O RCH1_C GPIO[124]	eTPU A channel eTPU A channel (output only) Reaction channel 1C GPIO	P A1 A2 G	001 010 100 000	124	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	49	M1	H3
ETPUA11 ETPUA23_O RCH4_B GPIO[125]	eTPU A channel eTPU A channel (output only) Reaction channel 4B GPIO	P A1 A2 G	001 010 100 000	125	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	48	L2	J2

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
EMIOS5 ETPUA5_O GPIO[184]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	184	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AA12
EMIOS6 ETPUA6_O GPIO[185]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	185	I/O O I/O	VDDEH4 / Slow	— / Down	— / Down	68	P7	Y12
EMIOS7 ETPUA7_O GPIO[186]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	186	I/O O I/O	VDDEH4 / Slow	— / Down	— / Down	69	—	AB13
EMIOS8 ETPUA8_O SCI_B_TX GPIO[187]	eMIOS channel eTPU A channel (output only) eSCI B transmit GPIO	P A1 A2 G	001 010 100 000	187	I/O O O I/O	VDDEH4 / Slow	— / Up	— / Up	70	P8	W13
EMIOS9 ETPUA9_O SCI_B_RX GPIO[188]	eMIOS channel eTPU A channel (output only) eSCI B receive GPIO	P A1 A2 G	001 010 100 000	188	I/O O I I/O	VDDEH4 / Slow	— / Up	— / Up	71	R7	AA13
EMIOS10 DSPI_D_PCS[3] RCH3_B GPIO[189]	eMIOS channel DSPI D peripheral chip select Reaction channel 3B GPIO	P A1 A2 G	001 010 100 000	189	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	73	N8	Y13
EMIOS11 DSPI_D_PCS[4] RCH3_C GPIO[190]	eMIOS channel DSPI D peripheral chip select Reaction channel 3C GPIO	P A1 A2 G	001 010 100 000	190	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	75	R8	AB14
EMIOS12 DSPI_C_SOUT ETPUA27_O GPIO[191]	eMIOS channel DSPI C data output eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	191	I/O O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	76	N10	W15
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 / Medium	— / WKPCFG	— / WKPCFG	77	T8	AA14

Table 6. Signal details (continued)

Signal	Module or function	Description
IRQ[0:5] IRQ[7:15]	SIU – External Interrupts	The IRQ[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the IRQ[0:15] pins as inputs to the IRQs. See reference manual section “External IRQ Input Select Register (SIU_EIISR)” for more information.
NMI	SIU – External Interrupts	Non-Maskable Interrupt
GPIO[12:17] GPIO[75:110] GPIO[113:145] GPIO[179:204] GPIO[206:213] GPIO[219] GPIO[244:245]	SIU – GPIO	Configurable general purpose I/O pins. Each GPIO input and output is separately controlled by an 8-bit input (GPDI) or output (GPDO) register. Additionally, each GPIO pin is configured using a dedicated SIU_PCR register. The GPIO pins are generally multiplexed with other I/O pin functions. See the following reference manual sections for more information: – “Pad Configuration Registers (SIU_PCR)” – “GPIO Pin Data Output Registers (SIU_GPDO0_3 – SIU_GPDO412_413)” – “GPIO Pin Data Input Registers (SIU_GPDI0_3 – SIU_GPDI_232)”
$\overline{\text{RESET}}$	SIU – Reset	The $\overline{\text{RESET}}$ pin is an active low input. The $\overline{\text{RESET}}$ pin is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the $\overline{\text{RESET}}$ pin asserts for 10 clock cycles. Assertion of the $\overline{\text{RESET}}$ pin while the device is in reset causes the reset cycle to start over. The $\overline{\text{RESET}}$ pin has a glitch detector which detects spikes greater than two clock cycles in duration that fall below the switch point of the input buffer logic of the VDDEH input pins. The switch point lies between the maximum VIL and minimum VIH specifications for the VDDEH input pins.
RSTCFG	SIU – Reset	Used to enable or disable the PLLREF and the BOOTCFG[0:1] configuration signals. 0:Get configuration information from BOOTCFG[0:1] and PLLREF 1:Use default configuration of booting from internal flash with crystal clock source For the 176-pin QFP and 208-ball BGA packages RSTCFG is always 0, so PLLREF and BOOTCFG signals are used.

Table 6. Signal details (continued)

Signal	Module or function	Description
$\overline{\text{RSTOUT}}$	SIU – Reset	The $\overline{\text{RSTOUT}}$ pin is an active low output that uses a push/pull configuration. The $\overline{\text{RSTOUT}}$ pin is driven to the low state by the MCU for all internal and external reset sources. There is a delay between initiation of the reset and the assertion of the $\overline{\text{RSTOUT}}$ pin. See reference manual section “RSTOUT” for details.

Table 7. Power/ground segmentation

Power segment	Voltage	I/O pins powered by segment
VDDE5	3.0 V – 3.6 V	DATA[0:15], CLKOUT, ENGCLK
VDDE12	3.0 V – 3.6 V	CAL_CS0, CAL_CS2, CAL_CS3, CAL_ADDR[12:30], CAL_DATA[0:15], CAL_RD_WR, CAL_WE0, CAL_WE1, CAL_OE, CAL_TS
VDDE-EH	3.0 V – 5.5 V	FR_A_TX, FR_A_TX_EN, FR_A_RX, FR_B_TX, FR_B_TX_EN, FR_B_RX
VDDEH1	3.3 V – 5.5 V	ETPUA[10:31]
VDDEH4	3.3 V – 5.5 V	EMIOS[0:23], TCRCLKA, ETPUA[0:9]
VDDEH6	3.3 V – 5.5 V	$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, PLLREF, PLLCFG1, RSTCFG, BOOTCFG0, BOOTCFG1, WKPCFG, CAN_A_TX, CAN_A_RX, CAN_B_TX, CAN_B_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_B_RX, SCI_C_TX, SCI_C_RX, DSPI_B_SCK, DSPI_B_SIN, DSPI_B_SOUT, DSPI_B_PCS[0:5], EXTAL, XTAL
VDDEH7	3.3 V – 5.5 V	EMIOS14, EMIOS15, GPIO[98:99], GPIO[203:204], GPIO[206], GPIO[207], GPIO[219], EVTI, EVTO, MDO[4:11], MSEO0, MSEO1, RDY, TCK, TDI, TDO, TMS, JCOMP, DSPI_A_SCK, DSPI_A_SIN, DSPI_A_SOUT, DSPI_A_PCS[0:1], DSPI_A_PCS[4:5], AN12-SDS, AN13-SDO, AN14-SDI, AN15-FCK
VDDA	5.0 V	AN[0:11], AN[16:39], VRH, VRL, REFBYBC
VRC33	3.3 V	MCKO, MDO[0:3]
Other power segments		
VDDREG	5.0 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.9 V – 6.0 V	—
VSS	—	—

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the SPC564A70 series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 16. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f – 35%	Por3.3V_f	Por3.3V_f + 35%	V
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply	—	4.290	—	V
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset	Lvi5p0 – 6%	Lvi5p0	Lvi5p0 + 6%	V
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset	Lvi5p0 – 3%	Lvi5p0	Lvi5p0 + 3%	V
8c	—	CC	C	Trimming step LVI 5 V	—	20	—	mV
8d	Lvi5p0_h	CC	C	LVI 5 V hysteresis	—	60	—	mV
9	Por5V_r	CC	C	Nominal POR for rising 5 V VDDREG supply	—	2.67	—	V
9a	—	CC	C	Variation of POR for rising 5 V VDDREG supply	Por5V_r – 35%	Por5V_r	Por5V_r + 35%	V
9b	Por5V_f	CC	C	Nominal POR for falling 5 V VDDREG supply	—	2.47	—	V
9c	—	CC	C	Variation of POR for falling 5 V VDDREG supply	Por5V_f – 35%	Por5V_f	Por5V_f + 35%	V

1. Using external ballast transistor.
2. Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.
3. LVI for falling supply is calculated as LVI rising – LVI hysteresis.
4. Lvi1p2 tracks DC target variation of internal V_{DD} regulator. Minimum and maximum Lvi1p2 correspond to minimum and maximum V_{DD} DC target respectively.
5. With internal load up to Idd3p3
6. The Lvi3p3 specs are also valid for the V_{DDEH} LVI
7. Lvi3p3 tracks DC target variation of internal V_{DD33} regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum V_{DD33} DC target respectively.
8. The 3.3V POR specs are also valid for the V_{DDEH} POR

3.6.1 Regulator example

In designs where the SPC564A70 microcontroller's internal regulators are used, a ballast is required for generation of the 1.2 V internal supply. No ballast is required when an external 1.2 V supply is used.

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IH_S}	SR	P	Slow/medium pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{IH_F}	SR	P	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE} + 0.3	
V_{IH_LS}	SR	P	Multi-voltage pad I/O input high voltage in low-swing-mode(7)(8)(9)(10)	Hysteresis enabled	2.5	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDE} + 0.3	
V_{IH_HS}	SR	P	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage(11)	—	—	—	0.2 * V_{DDEH}	V
V_{OL_F}	CC	P	Fast I/O output low voltage(11)	—	—	—	0.2 * V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode(7)(8)(9)(10)(11)	—	—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode(11)	—	—	—	0.2 V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium I/O output high voltage(11)	—	0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage(11)	—	0.8 V_{DDE}	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode(7)(8)(9)(10)(11)	—	2.3	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode(11)	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	P	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	P	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-swing-mode multi-voltage I/O input hysteresis	Hysteresis enabled	0.25	—	—	v

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$R_{PUPD100K}$	SR	C	Weak pull-up/down resistance(21), 100 kΩ option	—	65	—	140	kΩ
R_{PUPD5K}	SR	C	Weak pull-up/down resistance(21), 5 kΩ option	5 V ± 10% supply	1.4	—	5.2	kΩ
		C		3.3 V ± 10% supply	1.7	—	7.7	
R_{PUPD5K}	SR	C	Weak Pull-Up/Down Resistance(21), 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
$R_{PUPDMTCH}$	CC	C	Pull-up/Down Resistance matching ratios (100K/200K)	Pull-up and pull-down resistances both enabled and settings are equal.	–2.5	—	2.5	%
T_A (T_L to T_H)	SR	P	Operating temperature range - ambient (packaged)	—	–40.0	—	125.0	°C
—	SR	D	Slew rate on power supply pins	—	—	—	25	V/ms

1. These specifications are design targets and subject to change per device characterization.
2. These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).
3. ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no undesirable behavior, but the accuracy will be degraded.
4. The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.
5. V_{FLASH} is available in the calibration package only.
6. Regulator is functional, with derated performance, with supply voltage down to 4.0 V
7. Multi-voltage power supply cannot be below 4.5 V when in low-swing mode
8. The slew rate (SRC) setting must be 0b11 when in low-swing mode.
9. While in low-swing mode there are no restrictions in transitioning to high-swing mode.
10. Pin in low-swing mode can accept a 5 V input
11. All V_{OL}/V_{OH} values 100% tested with ± 2 mA load except where otherwise noted
12. Bypass mode, system clock @ 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 x PWM channels @ 1 kHz, all other modules stopped.
13. Bypass mode, system clock @ 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped
14. If 1.2V and 3.3V internal regulators are on,then iddreg=70mA

    If supply is external that is 3.3V internal regulator is off, then iddreg=15mA
15. Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See *Table 22* for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
16. Absolute value of current, measured at V_{IL} and V_{IH}
17. Weak pull-up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to all digital pad types.
18. Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to analog pads.
19. Applies to CLKOUT, external bus pins, and Nexus pins

Table 38. JTAG pin AC electrical characteristics[1] (continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	10	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	22[2]	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	22	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns
12	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	50	ns
13	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	50	ns
14	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	25[3]	—	ns
15	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	25[3]	—	ns

1. JTAG timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, C_L = 30 pF, SRC = 0b11. These specifications apply to JTAG boundary scan only. See *Table 39* for functional specifications.
2. Pad delay is 8–10 ns. Remainder includes TCK pad delay, clock tree delay logic delay and TDO output pad delay.
3. For 20 MHz TCK.

Note: The Nexus/JTAG Read/Write Access Control/Status Register (RWCS) write (to begin a read access) or the write to the Read/Write Access Data Register (RWD) (to begin a write access) does not actually begin its action until 1 JTAG clock (TCK) after leaving the JTAG Update-DR state. This prevents the access from being performed and therefore will not signal its completion via the READY (RDY) output unless the JTAG controller receives an additional TCK. In addition, EVTI is not latched into the device unless there are clock transitions on TCK.

Table 42. Calibration bus operation timing(1) (continued)

#	Symbol		C	Characteristic	66 MHz(2)		Unit
					Min	Max	
8	t_{CIH}	CC	P	CLKOUT Posedge to Input Signal Invalid (Hold Time) DATA[0:31]	1.0	—	ns
9	t_{APW}	CC	P	ALE Pulse Width(5)	6.5	—	ns
10	t_{AAI}	CC	P	ALE Negated to Address Invalid(5)	1.5(6)	—	ns

1. Calibration bus timing specified at f_{SYS} = 150 MHz and 100 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. The calibration bus is limited to half the speed of the internal bus. The maximum calibration bus frequency is 66 MHz. The bus division factor should be set accordingly based on the internal frequency being used.
3. Signals are measured at 50% V_{DDE}
4. Refer to fast pad timing in *Table 35* and *Table 36* (different values for 1.8 V vs. 3.3 V).
5. Measured at 50% of ALE
6. When CAL_TS pad is used for CAL_ALE function the hold time is 1 ns instead of 1.5 ns.

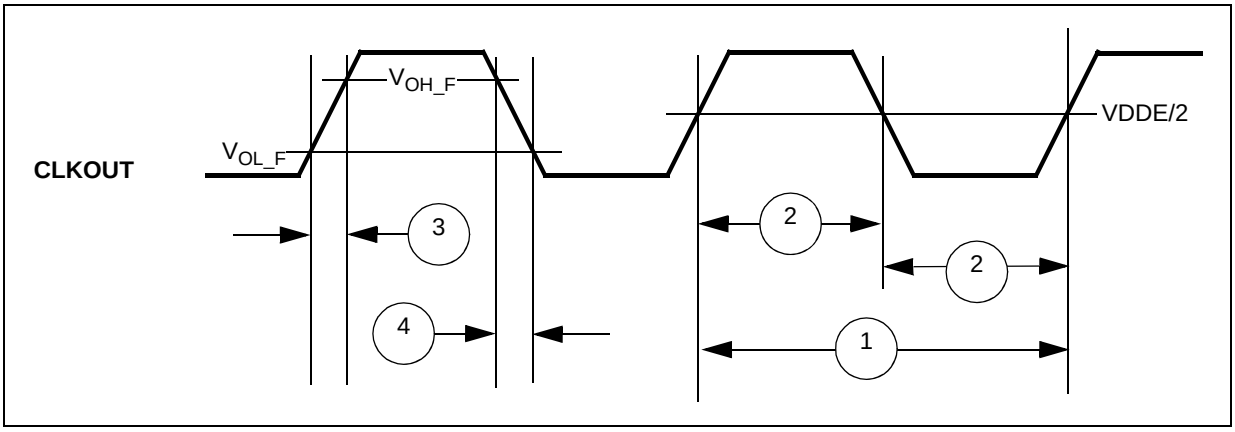

Figure 19. CLKOUT timing

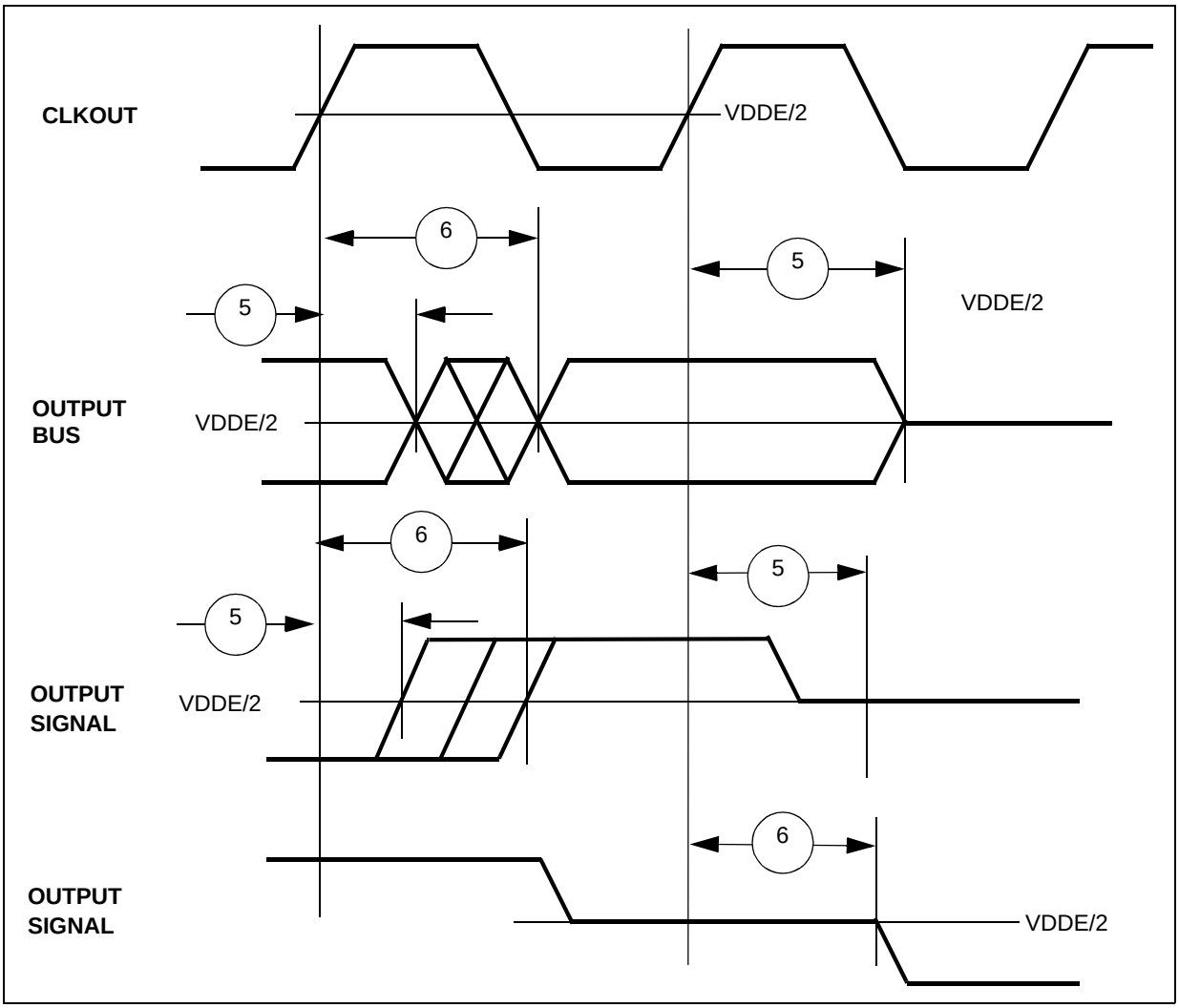

Figure 20. Synchronous output timing

Table 52. LBGA208 mechanical data[1] (continued)

Symbol	mm			inches[2]		
	Min	Typ	Max	Min	Typ	Max
A2	—	1.085	—	1.03	1.085	1.14
A3	—	0.30	—	0.26	0.30	0.34
A4	—	—	0.80	0.77	0.785	0.80
b[4]	0.50	0.60	0.70	0.55	0.60	0.65
D	16.80	17.00	17.20	16.90	17.00	17.10
D1	—	15.00	—	—	15.00	—
E	16.80	17.00	17.20	16.90	17.00	17.10
E1	—	15.00	—	—	15.00	—
e	—	1.00	—	—	1.00	—
F	—	1.00	—	—	1.00	—
ddd	—	—	0.20	—	—	0.0079
eee[5]	—	—	0.25	—	—	0.0098
fff[6],[7]	—	—	0.10	—	—	0.0039

1. Controlling dimension: millimeter
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. LBGA stands for **L**ow profile **B**all **G**rid **A**rray.
   - Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
   - The maximum total package height is calculated by the following methodology:
   A2 Typ + A1 Typ +√ ($A1^2$ + $A3^2$ + $A4^2$ tolerance values)
   - Low profile: 1.20 mm < A ≤ 1.70 mm
4. The typical ball diameter before mounting is 0.60 mm.
5. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
6. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.
7. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

4.2.3 PBGA324

6 Revision history

Table 54 summarizes customer facing revisions to this document.

Table 54. Document revision history

Date	Revision	Changes
07-Oct-2010	1	Initial release.
11-Apr-2012	2	*Figure 1 (SPC564A70 series block diagram)*, added ECSM block and its definition in the elegend. *Table 3 (SPC564A70 series block summary)*, added the following blocks: REACN, SIU, ECSM, FMPLL, PIT and SWT. Updated *Table 9 (Absolute maximum ratings)* In *3, Electrical characteristics*, deleted the “Recommended operating conditions” subsection. *Table 15 (PMC operating conditions and external regulators supply voltage)*, removed minimum value of V_{DDREG} and its footnote. Updated *Table 16 (PMC electrical characteristics)* Updated *Section 3.6.1, Regulator example* Updated *Table 21 (DC electrical specifications)* *Figure 8 (Core voltage regulator controller external components preferred configuration)*, added “T1” label to indicate the transistor. *Table 21 (DC electrical specifications)*, changed maximum value of V_{IL_LS} to 0.9, was 1.1 *Table 22 (I/O pad average IDDE specifications)*, in the V_{DDE} column changed all 5.5 to 5.25 *Table 25 (DSPI LVDS pad specification)*: Renamed V_{OC}, was V_{OD} Updated minimum and maximum value of V_{OC} deleted all footnote *Table 27 (Temperature sensor electrical characteristics)*, updated minimum and maximum value of accuracy Updated *Section 3.12, eQADC electrical characteristics* Added *Section 3.13, Configuring SRAM wait states* Updated *Table 32 (APC, RWSC, WWSC settings vs. frequency of operation)* Updated *Table 33 (Flash program and erase specifications)* *Table 32 (APC, RWSC, WWSC settings vs. frequency of operation)*, changed all values in the WWSC column to 0b01. Updated *Table 33 (Flash program and erase specifications)* *Table 34 (Flash EEPROM module life)*: updated temperature value in the Retention description (was 150 °C, is 85 °C) added values for Retention *Table 35 (Pad AC specifications (VDDE = 4.75 V))*: changed maximum value of Medium to 12/12 changed maximum value of Slow to 20/20 Updated *Table 36 (Pad AC specifications (VDDE = 3.0 V))* *Table 38 (JTAG pin AC electrical characteristics)*: changed all parameter classification to D changed minumum value of t_{TMSS}, t_{TDIS} to 10 Updated *Table 39 (Nexus debug port timing)*

Table 54. Document revision history (continued)

Date	Revision	Changes
11-Apr-2012	2 (continued)	Added *Table 40 (Nexus debug port operating frequency)* *Table 40 (Nexus debug port operating frequency)*, added a footnote near the value of t_{AAI} *Table 45 (eMIOS timing)*: changed minumum value of t_{MOPW} to 1 removed the footnote of t_{MOPW} Merged "DSPI timing (V_{DDEH} = 3.0 to 3.6 V)" and "DSPI timing (V_{DDEH} = 4.5 to 5.5V)" tables into *Table 47 (DSPI timing)* and changed all parameter classification to D *Table 48 (eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V))* changed all parameter classification to D *Table 52 (LBGA208 mechanical data)* deleted Notes column and moved all footnote next to relative references *Table 53 (PBGA324 package mechanical data)* deleted Notes column and moved all footnote next to relative references [[ST_Specific]] *Table 12 (Thermal characteristics for 324-pin PBGA)*, updated values In *Section 3.6, Power management control (PMC) and power on reset (POR) electrical specifications*, deleted the "Voltage regulator controller (V_{RC}) electrical specifications" Updated *Section 4.2.1, LQFP176*
06-Jun-2012	3	Minor editorial changes and improvements throughout. In *Section 2.4, Signal summary*, *Table 4 (SPC564A70 signal properties)*, updated the following properties for the Nexus pins: – Added a footnote to the "Nexus" title for this pin group. – Added a footnote to the "Name" entry for $\overline{\text{EVTO}}$. – Updated the "Status During reset" entry for $\overline{\text{EVTO}}$. In *Section 3.2, Maximum ratings*, *Table 9 (Absolute maximum ratings)*, removed the "TBD - To be defined" footnote. In *Section 3.8, DC electrical specifications*, *Table 21 (DC electrical specifications)*, removed the "TBD - To be defined" footnote. In *Section 3.9, I/O pad current specifications*, *Table 22 (I/O pad average IDDE specifications)*: – Updated values and replaced TBDs with numerical data. – Removed the "TBD - To be defined" footnote. In *Section 3.9.1, I/O pad VRC33 current specifications*, *Table 23 (I/O pad VRC33 average IDDE specifications)*: – Updated values and replaced TBDs with numerical data. – Removed the "TBD - To be defined" footnote. In *Section 3.14, Platform flash controller electrical characteristics*, *Table 32 (APC, RWSC, WWSC settings vs. frequency of operation)*, removed the "TBD - To be defined" footnote. In *Table 54 (Document revision history)*, removed extraneous text from the Revision 2 entry.
18-Sep-2013	4	Updated Disclaimer.