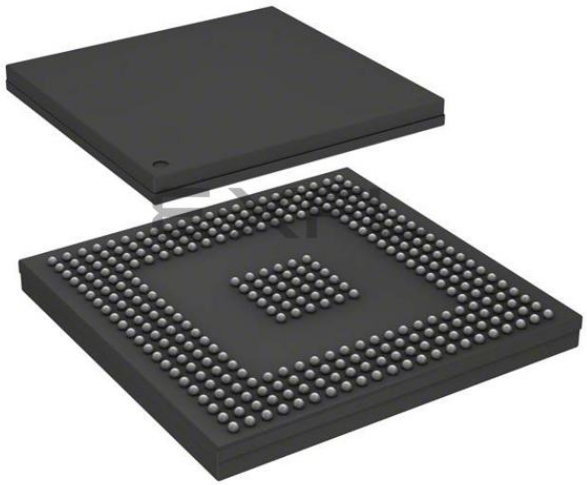

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70b4cobr

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- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- 1 interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts optionally enabled
- Support for scatter/gather DMA processing
- Ability to suspend channel transfers by a higher priority channel

1.5.4 Interrupt controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

The INTC provides the following features:

- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can assigned a specific priority by software
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—3 clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

1.5.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all

system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - 2 types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the preprogrammed memory region descriptors
  - An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
  - 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the 3 modes may be run with a crystal oscillator or an external clock reference

- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

1.5.14 Enhanced queued analog-to-digital converter (eQADC)

The eQADC block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog-to-digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of

comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.20 Software watchdog timer (SWT)

The SWT is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

1.5.21 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (*x*25 protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.22 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

2.2 LBGA208 ballmap[b]

Figure 3. 208-pin LBGA package ballmap (viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_SOUT	DSPI_B_PCS[3]	DSPI_B_SIN	DSPI_B_PCS[0]	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO[99]	DSPI_B_PCS[4]	DSPI_B_PCS[2]	DSPI_B_PCS[1]	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_PCS[5]	SCI_A_TX	GPIO[98]	DSPI_B_SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ETPUA19_O	VRC33	VSS	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO[207]	NC	EMIOS6	EMIOS8	MDO11_ETPUA29_O	MDO4_ETPUA2_O	MDO8_ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P

b. LBGA208 is available upon specific request. Please contact your ST sales office for details.

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
AN36	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[36] / —	174	F4	B4
AN37	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[37] / —	175	E3	A4
AN38	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[38] / —	—	—	C5
AN39	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[39] / —	8	D2	B5
VRH	Voltage Reference High	P	—	—	I	VDDA / —	I / —	—	163	A8	A10
VRL	Voltage Reference Low	P	—	—	I	VDDA / —	I / —	—	162	A9	A11
REFBYBC	Reference Bypass Capacitor Input	P	—	—	I	VDDA / Analog	I / —	—	164	B7	B10
eTPU2											
TCRCLKA IRQ[7] GPIO[113]	eTPU A TCR clock External interrupt request GPIO	P A1 G	01 10 00	113	I I I/O	VDDEH4 / Slow	— / Up	— / Up	—	L4	M2
ETPUA0 ETPUA12_O ETPUA19_O GPIO[114]	eTPU A channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	114	I/O O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	61	N3	L3
ETPUA1 ETPUA13_O GPIO[115]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	115	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	60	M3	L4
ETPUA2 ETPUA14_O GPIO[116]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	116	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	59	P2	K3
ETPUA3 ETPUA15_O GPIO[117]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	117	I/O O I/O	VDDEH4 / Slow	— / WKPCFG	GPIO / WKPCFG	58	P1	L2

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
ETPUA12 DSPI_B_PCS[1] RCH4_C GPIO[126]	eTPU A channel DSPI B peripheral chip select Reaction channel 4C GPIO	P A1 A2 G	001 010 100 000	126	I/O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	47	L1	J1
ETPUA13 DSPI_B_PCS[3] GPIO[127]	eTPU A channel DSPI B peripheral chip select GPIO	P A1 G	01 10 00	127	I/O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	46	J4	G4
ETPUA14 DSPI_B_PCS[4] ETPUA9_O RCH0_A GPIO[128]	eTPU A channel DSPI B peripheral chip select eTPU A channel (output only) Reaction channel 0A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	128	I/O O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	42	J3	G3
ETPUA15 DSPI_B_PCS[5] RCH1_A GPIO[129]	eTPU A channel DSPI B peripheral chip select Reaction channel 1A GPIO	P A1 A2 G	001 010 100 000	129	I/O O O I/O	VDDEH1 / Medium	— / WKPCFG	— / WKPCFG	40	K2	H2
ETPUA16 DSPI_D_PCS[1] RCH2_A GPIO[130]	eTPU A channel DSPI D peripheral chip select Reaction channel 2A GPIO	P A1 A2 G	001 010 100 000	130	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	39	K1	H1
ETPUA17 DSPI_D_PCS[2] RCH3_A GPIO[131]	eTPU A channel DSPI D peripheral chip select Reaction channel 3A GPIO	P A1 A2 G	001 010 100 000	131	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	38	H3	F3
ETPUA18 DSPI_D_PCS[3] RCH4_A GPIO[132]	eTPU A channel DSPI D peripheral chip select Reaction channel 4A GPIO	P A1 A2 G	001 010 100 000	132	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	37	H4	F4
ETPUA19 DSPI_D_PCS[4] RCH5_A GPIO[133]	eTPU A channel DSPI D peripheral chip select Reaction channel 5A GPIO	P A1 A2 G	001 010 100 000	133	I/O O O I/O	VDDEH1 / Slow	— / WKPCFG	— / WKPCFG	36	J2	G2

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
VDDEH1AB[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1AB[19]	—	K4	H4
VDDEH4[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4[20]	—	—	—
VDDEH4A[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4A[20]	55	—	—
VDDEH4B[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4B[20]	74	—	—
VDDEH4AB[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4AB[20]	—	N9	W14
VDDEH6[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6[21]	—	—	—
VDDEH6A[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6A[21]	95	—	—
VDDEH6B[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6B[21]	110	—	—
VDDEH6AB[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6AB[21]	—	F13	H19, U19
VDDEH7[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7	—	D12	D15
VDDEH7A[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7A	125	—	—
VDDEH7B[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D19, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M11, M12, M13, M14, N9, N10, N12, N13, N14, P9, P10, P12, P13, P14, T21, T22, W4, W19, Y3, Y20, AA2, AA21, AB1, AB22

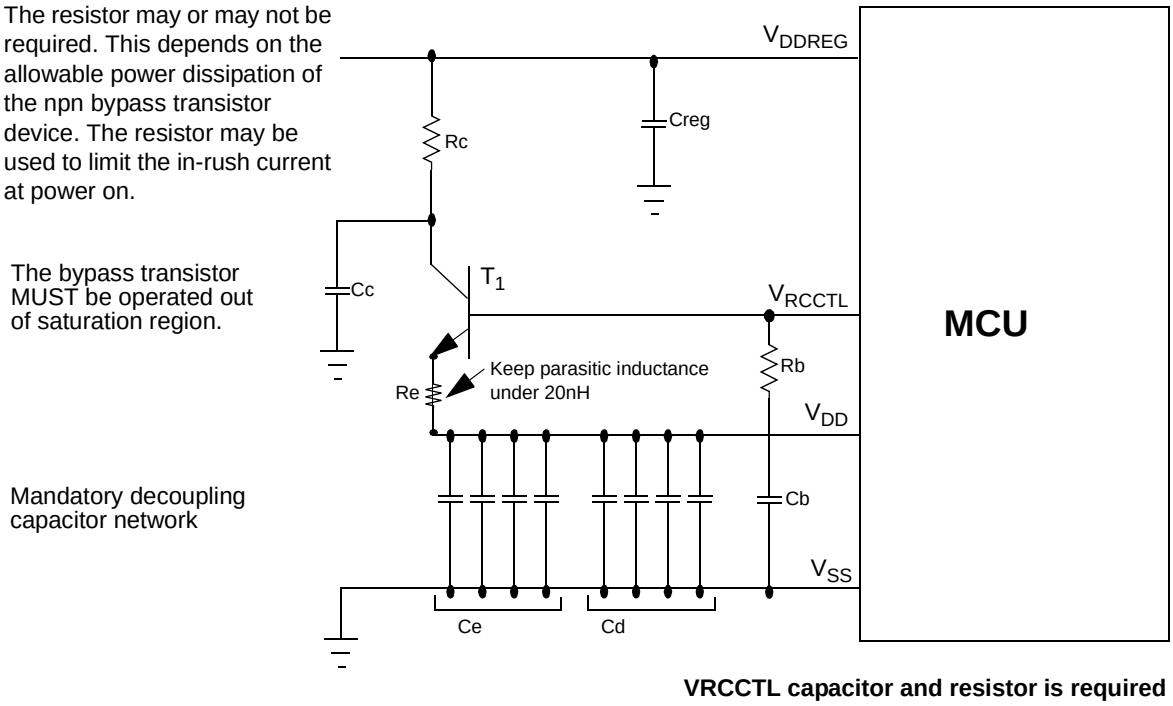

Figure 8. Core voltage regulator controller external components preferred configuration

Table 17. SPC564A70 External network specification

External Network Parameter	Min	Typ	Max	Comment
T1	—	—	—	NJD2873 or BCP68 only
Cb	1.1 µF	2.2µF	2.97µF	X7R,-50%/+35%
Ce	3*2.35µF+5µF	3*4.7µF+10µF	3*6.35µF+13.5µF	X7R, -50%/+35%
Equivalent ESR of Ce capacitors	5mΩ	—	50mΩ	—
Cd	4*50nF	4*100nF	4*135nF	X7R, -50%/+35%
Rb	9Ω	10Ω	11Ω	+/-10%
Re	0.252Ω	0.280Ω	0.308Ω	+/-10%
Creg	—	10µF	—	It depends on external Vreg.
Cc	5µF	10µF	13.5µF	X7R, -50%/+35%
Rc	1.1Ω	—	5.6Ω	May or may not be required. It depends on the allowable power dissipation of T1.

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IH_S}	SR	P	Slow/medium pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{IH_F}	SR	P	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE} + 0.3	
V_{IH_LS}	SR	P	Multi-voltage pad I/O input high voltage in low-swing-mode(7)(8)(9)(10)	Hysteresis enabled	2.5	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDE} + 0.3	
V_{IH_HS}	SR	P	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage(11)	—	—	—	0.2 * V_{DDEH}	V
V_{OL_F}	CC	P	Fast I/O output low voltage(11)	—	—	—	0.2 * V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode(7)(8)(9)(10)(11)	—	—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode(11)	—	—	—	0.2 V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium I/O output high voltage(11)	—	0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage(11)	—	0.8 V_{DDE}	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode(7)(8)(9)(10)(11)	—	2.3	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode(11)	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	P	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	P	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-swing-mode multi-voltage I/O input hysteresis	Hysteresis enabled	0.25	—	—	v

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{ACT_F}	CC	P	Fast I/O weak pull-up/down current(16)	1.62 V–1.98 V	36	—	120	µA
		P		2.25 V–2.75 V	34	—	139	
		P		3.0 V–3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pull-up current	V_{DDE} = 3.0 – 3.6 V(7), multi-voltage, high swing mode only	10	—	75	µA
		C		4.75 V–5.25 V	25	—	175	
$I_{ACT\_MV\_PD}$	CC	C	Multi-voltage pad weak pull-down current	V_{DDE} = 3.0 – 3.6 V(7), multi-voltage, all process corners, high swing mode only	10	—	60	µA
		C		4.75 V–5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current(17)	—	–2.5	—	2.5	µA
I_{IC}	SR	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	SR	P	Analog input current, channel off, AN[0:7](18)	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins18	—	–150	—	150	
C_L	CC	D	Load capacitance (fast I/O)(19)	DSC(PCR[8:9]) = 0b00	—	—	10	pF
		D		DSC(PCR[8:9]) = 0b01	—	—	20	
		D		DSC(PCR[8:9]) = 0b10	—	—	30	
		D		DSC(PCR[8:9]) = 0b11	—	—	50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—	—	7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—	—	10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins(20))	—	—	—	12	pF
$R_{PUPD200K}$	SR	C	Weak pull-up/down resistance(21), 200 kΩ option	—	130	—	280	kΩ

Table 22. I/O pad average I_{DDE} specifications(1) (continued)

Pad type	Symbol	C		Period (ns)	Load(2) (pF)	V_{DDE} (V)	Drive/Slew rate select	I_{DDE} Avg (mA)(3)	I_{DDE} RMS (mA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.25	11	9	—
		CC	D	30	50	5.25	01	6.1	—
		CC	D	117	50	5.25	00	2.3	—
		CC	D	212	200	5.25	00	5.8	—
MultiV (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.25	11	3.4	—

1. Numbers from simulations at best case process, 150 °C
2. All loads are lumped.
3. Average current is for pad configured as output only

3.9.1 I/O pad V_{RC33} current specifications

The power consumption of the V_{RC33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from *Table 23* based on the voltage, frequency, and load on all fast pins. The input pin V_{RC33} current can be calculated from *Table 23* based on the voltage, frequency, and load on all medium pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in *Table 23*.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1)

Max. Flash Operating Frequency (MHz)(2)	APC(3)	RWSC(3)	WWSC
20 MHz	0b000	0b000	0b01
61 MHz	0b001	0b001	0b01
90 MHz	0b010	0b010	0b01
123 MHz	0b011	0b011	0b01
153 MHz	0b100	0b100	0b01

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. Max frequencies including 2% PLL FM.
3. APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications(1)

#	Symbol		C	Parameter	Value				Unit
					Min	Typ	Initial max(2)	Max(3)	
1	$T_{dwprogram}$	CC	C	Double Word (64 bits) Program Time	—	30	—	500	µs
2	$T_{pprogram}$	CC	C	Page Program Time(4)	—	40	160	500	µs
3	$T_{16kpperase}$	CC	C	16 KB Block Pre-program and Erase Time	—	—	1000	5000	ms
5	$T_{64kpperase}$	CC	C	64 KB Block Pre-program and Erase Time	—	—	1800	5000	ms
6	$T_{128kpperase}$	CC	C	128 KB Block Pre-program and Erase Time	—	—	2600	7500	ms
7	$T_{256kpperase}$	CC	C	256 KB Block Pre-program and Erase Time	—	—	5200	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

Table 36. Pad AC specifications (V_{DDE} = 3.0 V)(1) (continued)

Pad type		C	Output delay (ns)(2)(3) Low-to-High / High-to-Low		Rise/Fall edge (ns)(3)(4)		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Fast	CC	D	—	2.5/2.5	—	1.2/1.2	10	00
	CC	D	—	2.5/2.5	—	1.2/1.2	20	01
	CC	D	—	2.5/2.5	—	1.2/1.2	30	10
	CC	D	—	2.5/2.5	—	1.2/1.2	50	11(8)
Standalone input buffer(12)	CC	D	0.5/0.5	3/3	0.4/0.4	±1.5/1.5	0.5	—

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V, V_{DDEH} = 3 V to 3.6 V, $T_A = T_L$ to T_H.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad V_{OL} and V_{OH} values are the same as those of the slew controlled output pads.
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
7. Output delay is shown in *Figure 9* and *Figure 10*. Add a maximum of one system clock to the output delay for delay with respect to system clock.
8. Can be used on the tester.
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
11. Selectable high/low swing I/O pad with selectable slew in high swing mode only.
12. Also has weak pull-up/pull-down.

Figure 16. Nexus output timing

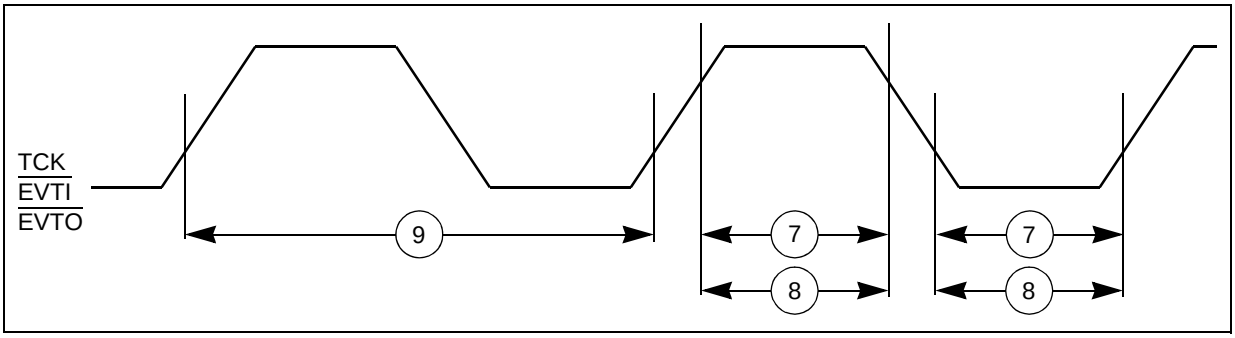

Figure 17. Nexus event trigger and test clock timings

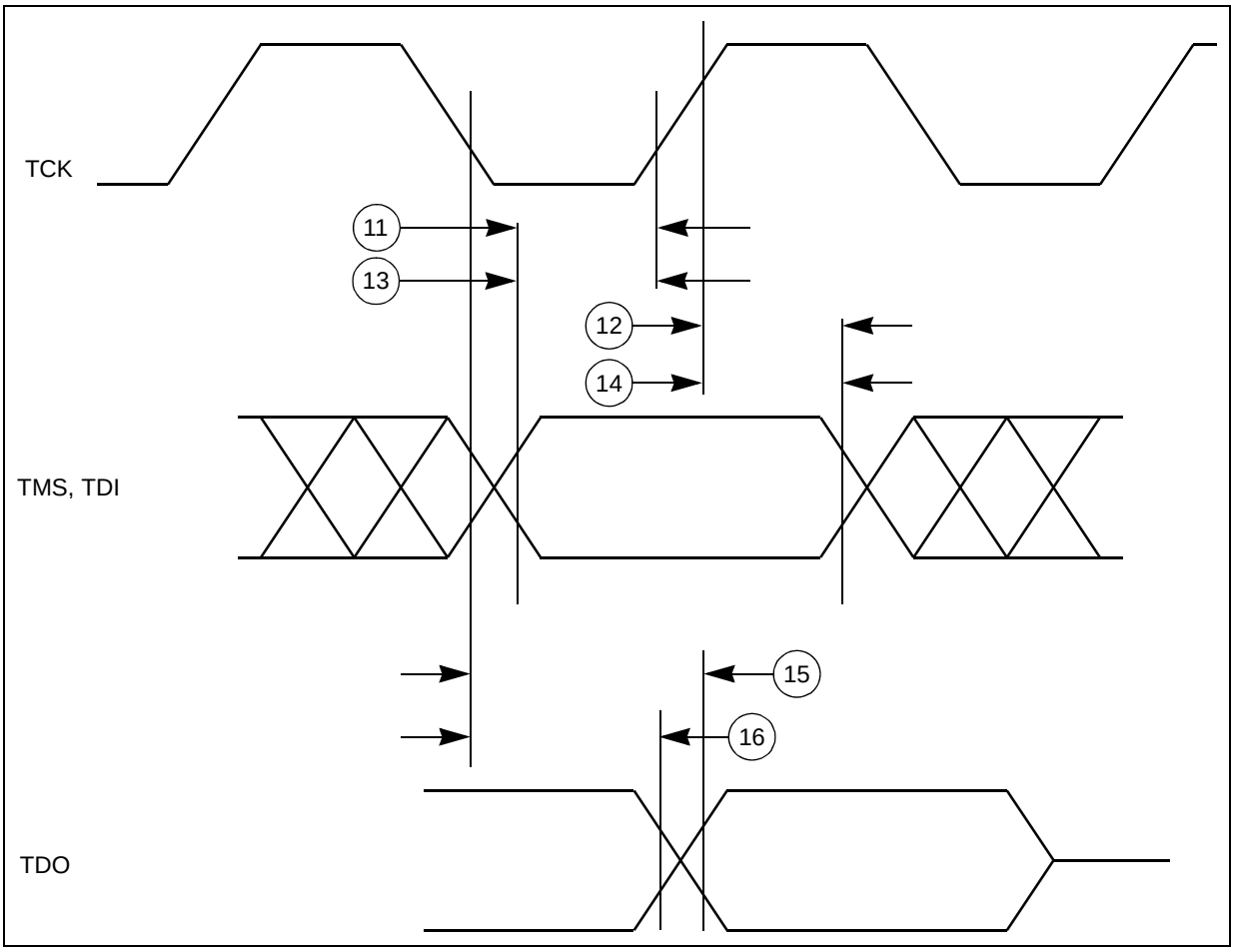

Figure 18. Nexus TDI, TMS, TDO timing

3.17.5 External interrupt timing (IRQ pin)

Table 43. External interrupt timing(1)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{IPWL}	IRQ Pulse Width Low	3	—	t_{CYC}
2	t_{IPWH}	IRQ Pulse Width High	3	—	t_{CYC}
3	t_{ICYC}	IRQ Edge to Edge Time(2)	6	—	t_{CYC}

1. IRQ timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

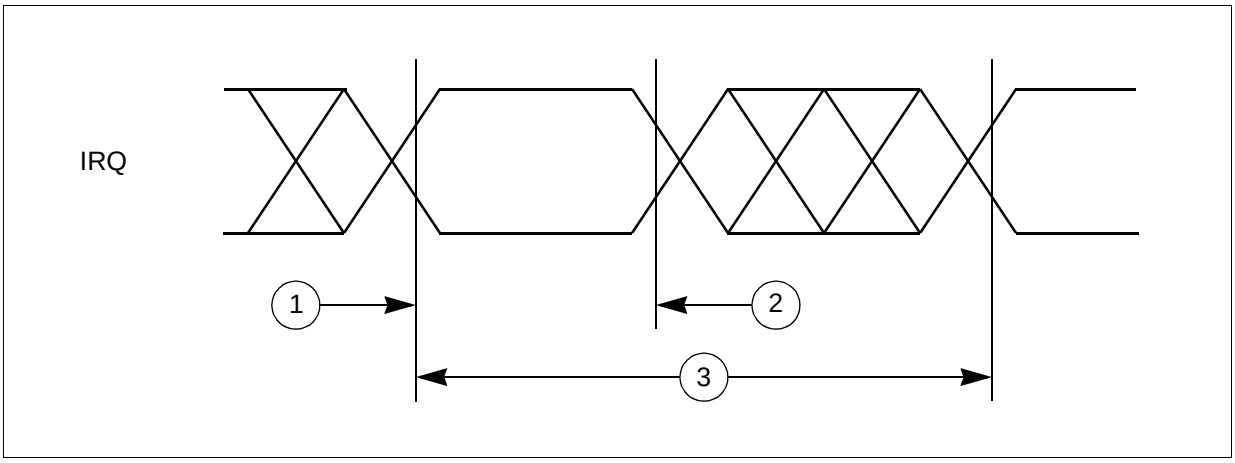

Figure 23. External interrupt timing

3.17.6 eTPU timing

Table 44. eTPU timing(1)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{ICPW}	eTPU Input Channel Pulse Width	4	—	t_{CYC}
2	t_{OCPW}	eTPU Output Channel Pulse Width(2)	2	—	t_{CYC}

1. eTPU timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.
2. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

3.17.7 eMIOS timing

Table 45. eMIOS timing(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

1. eMIOS timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

3.17.8 DSPI timing

DSPI channel frequency support for the SPC564A70 MCU is shown in *Table 46*. Timing specifications are in *Table 47*.

Table 46. DSPI channel frequency support

System clock (MHz)	DSPI Use Mode	Maximum usable frequency (MHz)	Notes
150	LVDS	37.5	Use sysclock /4 divide ratio
	Non-LVDS	18.75	Use sysclock /8 divide ratio
120	LVDS	40	Use sysclock /3 divide ratio. Gives 33/66 duty cycle. Use DSPI configuration DBR = 0b1 (double baud rate), BR = 0b0000 (scaler value 2) and PBR = 0b01 (prescaler value 3).
	Non-LVDS	20	Use sysclock /6 divide ratio
80	LVDS	40	Use sysclock /2 divide ratio
	Non-LVDS	20	Use sysclock /4 divide ratio

Table 47. DSPI timing(1)(2)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
1	t_{SCK}	CC	D	SCK Cycle Time(3)(4)(5)		24.4 ns	2.9 ms	—
2	t_{CSC}	CC	D	PCS to SCK Delay(6)		22(7)	—	ns
3	t_{ASC}	CC	D	After SCK Delay(8)		21(9)	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle		$(½t_{SC}) - 2$	$(½t_{SC}) + 2$	ns
5	t_A	CC	D	Slave Access Time ($\overline{SS}$ active to SOUT driven)		—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)		—	25	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time		4(10)	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time		5(11)	—	ns

Table 53. PBGA324 package mechanical data

Symbol	Databook (mm)			Drawing (mm)		
	Min	Typ	Max	Min	Typ	Max
A(1) (2) (3)	—	1.720	—	1.620	1.720	1.820
A1	0.270	—	—	0.350	0.400	0.450
A2	—	1.320	—	—	1.320	—
b	0.550	0.6000	0.650	0.550	0.600	0.650
D	22.80	23.00	23.200	22.900	23.000	23.100
D1	—	21.00	—	—	21.000	—
E	22.800	23.000	23.200	22.900	23.000	23.100
E1	—	21.000	—	—	21.000	—
e	0.950	1.000	1.050	0.950	1.000	1.050
f	0.875	1.000	1.125	0.875	1.000	1.125
ddd	—	—	0.200	—	—	0.200

1. Max mounted height is 1.77 mm. Based on 0.35 mm ball pad diameter. Solder paste is 0.15 mm thickness and 0.35 mm diameter.
2. PBGA stands for Plastic Ball Grid Array.
3. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1corner. Exact shape of each corner is optional.