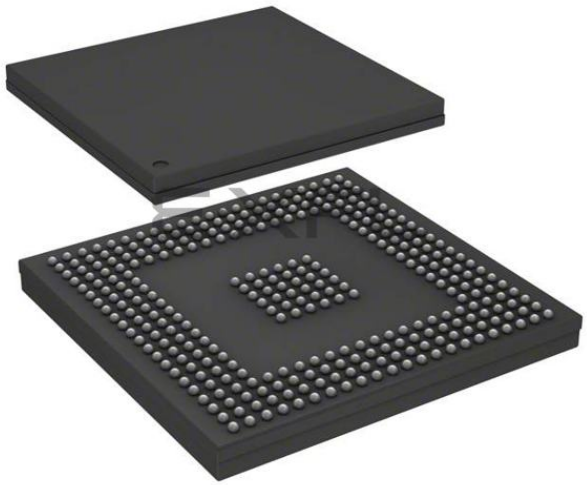

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70b4coby

List of tables

- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 System integration unit (SIU)

The SPC564A70 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin

1.5.16 Enhanced serial communications interface (eSCI)

Three eSCI modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Compatible with LIN slaves from revisions 1.x and 2.0 of the LIN standard
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.17 Controller area network (FlexCAN)

The SPC564A70 MCU includes three FlexCAN blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames

VSS	VSS	VSS					DSPI_A_ PCS[1]	DSPI_A_ PCS[0]	GPIO[98]	VDDREG	M
VSS	VSS	VSS					DSPI_A_ PCS[4]	SCI_A_TX	DSPI_A_ PCS[5]	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							WKPCFG	CAN_C_RX	SCI_B_TX	RESET	R
							SCI_B_RX	BOOTCFG1	VSS	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG0	EXTAL	U
							VDD	VRCCTL	PLLREF	XTAL	V
EMIOS2	EMIOS8	VDDEH4AB	EMIOS12	EMIOS21	VDDE12	SCI_C_TX	VSS	VDD	NC	VDDPLL	W
EMIOS6	EMIOS10	EMIOS15	EMIOS17	EMIOS22	CAN_A_TX	VDDE12	SCI_C_RX	VSS	VDD	VRC33	Y
EMIOS5	EMIOS9	EMIOS13	EMIOS16	EMIOS19	EMIOS23	CAN_A_RX	VDDE12	CLKOUT	VSS	VDD	AA
EMIOS4	EMIOS7	EMIOS11	EMIOS14	EMIOS18	EMIOS20	CAN_B_TX	CAN_B_RX	VDDE12	ENGCLK	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

Figure 7. 324-pin PBGA package ballmap (southeast, viewed from above)

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A1 G	01 10 00	107	O O I/O	VDDEH6 / Medium	— / Up	— / Up	107	H15	K22
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A1 G	01 10 00	108	O I I/O	VDDEH6 / Medium	— / Up	— / Up	114	G14	J20
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI B peripheral chip select SPI clock pin for DSPI module GPIO	P A1 G	01 10 00	109	O I/O I/O	VDDEH6 / Medium	— / Up	— / Up	105	H14	K20
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A1 G	01 10 00	110	O I/O I/O	VDDEH6 / Medium	— / Up	— / Up	104	J13	L19
eQADC											
AN0 DAN0+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[0] / —	172	B5	B8
AN1 DAN0–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[1] / —	171	A6	A8
AN2 DAN1+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[2] / —	170	D6	D10
AN3 DAN1–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[3] / —	169	C7	C9
AN4 DAN2+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[4] / —	168	B6	B9
AN5 DAN2–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[5] / —	167	A7	A9
AN6 DAN3+	Single Ended Analog Input Positive Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[6] / —	166	D7	D11

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
EMIOS14 IRQ[0] ETPUA29_O GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 / Slow	— / Down	— / Down	78	R9	AB15
EMIOS15 IRQ[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 / Slow	— / Down	— / Down	79	T9	Y14
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	AA15
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	Y15
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 / Slow	— / Up	— / Up	—	—	AB16
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AA16
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	AB17
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 / Slow	— / WKPCFG	— / WKPCFG	—	—	W16
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 / Slow	— / Down	— / Down	—	—	Y16
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 / Slow	— / Down	— / Down	80	R11	AA17
EMIOS14[16] GPIO[203]	eMIOS channel GPIO	P G	01 00	203	O I/O	VDDEH7 / Slow	— / Down	— / Down	—	—	H20
EMIOS15[16] GPIO[204]	eMIOS channel GPIO	P G	01 00	204	O I/O	VDDEH7 / Slow	— / Down	— / Down	—	—	H21
Clock Synthesizer											
XTAL	Crystal oscillator output	P	01	—	O	VDDEH6 / Analog	—	—	93	P16	V22
EXTAL	Crystal oscillator input	P	01	—	I	VDDEH6 / Analog	—	—	92	N16	U22

Table 6. Signal details (continued)

Signal	Module or function	Description
IRQ[0:5] IRQ[7:15]	SIU – External Interrupts	The IRQ[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the IRQ[0:15] pins as inputs to the IRQs. See reference manual section “External IRQ Input Select Register (SIU_EIISR)” for more information.
NMI	SIU – External Interrupts	Non-Maskable Interrupt
GPIO[12:17] GPIO[75:110] GPIO[113:145] GPIO[179:204] GPIO[206:213] GPIO[219] GPIO[244:245]	SIU – GPIO	Configurable general purpose I/O pins. Each GPIO input and output is separately controlled by an 8-bit input (GPDI) or output (GPDO) register. Additionally, each GPIO pin is configured using a dedicated SIU_PCR register. The GPIO pins are generally multiplexed with other I/O pin functions. See the following reference manual sections for more information: – “Pad Configuration Registers (SIU_PCR)” – “GPIO Pin Data Output Registers (SIU_GPDO0_3 – SIU_GPDO412_413)” – “GPIO Pin Data Input Registers (SIU_GPDI0_3 – SIU_GPDI_232)”
$\overline{\text{RESET}}$	SIU – Reset	The $\overline{\text{RESET}}$ pin is an active low input. The $\overline{\text{RESET}}$ pin is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the $\overline{\text{RESET}}$ pin asserts for 10 clock cycles. Assertion of the $\overline{\text{RESET}}$ pin while the device is in reset causes the reset cycle to start over. The $\overline{\text{RESET}}$ pin has a glitch detector which detects spikes greater than two clock cycles in duration that fall below the switch point of the input buffer logic of the VDDEH input pins. The switch point lies between the maximum VIL and minimum VIH specifications for the VDDEH input pins.
RSTCFG	SIU – Reset	Used to enable or disable the PLLREF and the BOOTCFG[0:1] configuration signals. 0:Get configuration information from BOOTCFG[0:1] and PLLREF 1:Use default configuration of booting from internal flash with crystal clock source For the 176-pin QFP and 208-ball BGA packages RSTCFG is always 0, so PLLREF and BOOTCFG signals are used.

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{ACT_F}	CC	P	Fast I/O weak pull-up/down current(16)	1.62 V–1.98 V	36	—	120	µA
		P		2.25 V–2.75 V	34	—	139	
		P		3.0 V–3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pull-up current	V_{DDE} = 3.0 – 3.6 V(7), multi-voltage, high swing mode only	10	—	75	µA
		C		4.75 V–5.25 V	25	—	175	
$I_{ACT\_MV\_PD}$	CC	C	Multi-voltage pad weak pull-down current	V_{DDE} = 3.0 – 3.6 V(7), multi-voltage, all process corners, high swing mode only	10	—	60	µA
		C		4.75 V–5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current(17)	—	–2.5	—	2.5	µA
I_{IC}	SR	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	SR	P	Analog input current, channel off, AN[0:7](18)	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins18	—	–150	—	150	
C_L	CC	D	Load capacitance (fast I/O)(19)	DSC(PCR[8:9]) = 0b00	—	—	10	pF
		D		DSC(PCR[8:9]) = 0b01	—	—	20	
		D		DSC(PCR[8:9]) = 0b10	—	—	30	
		D		DSC(PCR[8:9]) = 0b11	—	—	50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—	—	7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—	—	10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins(20))	—	—	—	12	pF
$R_{PUPD200K}$	SR	C	Weak pull-up/down resistance(21), 200 kΩ option	—	130	—	280	kΩ

Table 23. I/O pad V_{RC33} average I_{DDE} specifications(1)

Pad type	Symbol		C	Period (ns)	Load(2) (pF)	Drive select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV(3) (High swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	11	33.4	35.4
		CC	D	30	50	01	33.4	34.8
		CC	D	117	50	00	33.4	33.8
		CC	D	212	200	00	33.4	33.7
MultiV(4) (Low swing mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	11	33.4	33.7

1. These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
2. All loads are lumped.
3. Average current is for pad configured as output only
4. In low swing mode, multi-voltage pads must operate in highest slew rate setting, ipp_sre0 = 1, ipp_sre1 = 1.

Table 24. V_{RC33} pad average DC current(1)

Pad type	Symbol		C	Period (ns)	Load(2) (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1. These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
2. All loads are lumped.

Table 30. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)(5)	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2(5)	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1. Applies only to differential channels.
2. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.
3. At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.
4. Guaranteed 10-bit mono tonicity.
5. Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

(1)	SWSC Value
98	0
153	1

1. Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (V_{DDE} = 4.75 V)(1)

Name		C	Output delay (ns)(2)(3) Low-to-High / High-to-Low		Rise/Fall edge (ns)(3)(4)		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB, LSB
Medium(5)(6)(7)	CC	D	4.6/3.7	12/12	2.2/2.2	12/12	50	11(8)
	—							10(9)
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow(7)(10)	CC	D	7.3/5.7	19/18	4.4/4.3	20/20	50	11(8)
	—							10(9)
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV(11) (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11(8)
	—							10(9)
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11(8)
Fast(12)	—							
Standalone input buffer(13)	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	—

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, $T_A = T_L$ to T_H.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad V_{OL} and V_{OH} values are the same as those of the slew controlled output pads.
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
7. Output delay is shown in *Figure 9* and *Figure 10*. Add a maximum of one system clock to the output delay for delay with respect to system clock.

The tool/debugger must provide at least one TCK clock for the $\overline{EVTI}$ signal to be recognized by the MCU. When using the RDY signal to indicate the end of a Nexus read/write access, ensure that TCK continues to run for at least one TCK after leaving the Update-DR state. This can be just a TCK with TMS low while in the Run-Test/Idle state or by continuing with the next Nexus/JTAG command. Expect the effect of $\overline{EVTI}$ and RDY to be delayed by edges of TCK.

RDY is not available in all device packages.

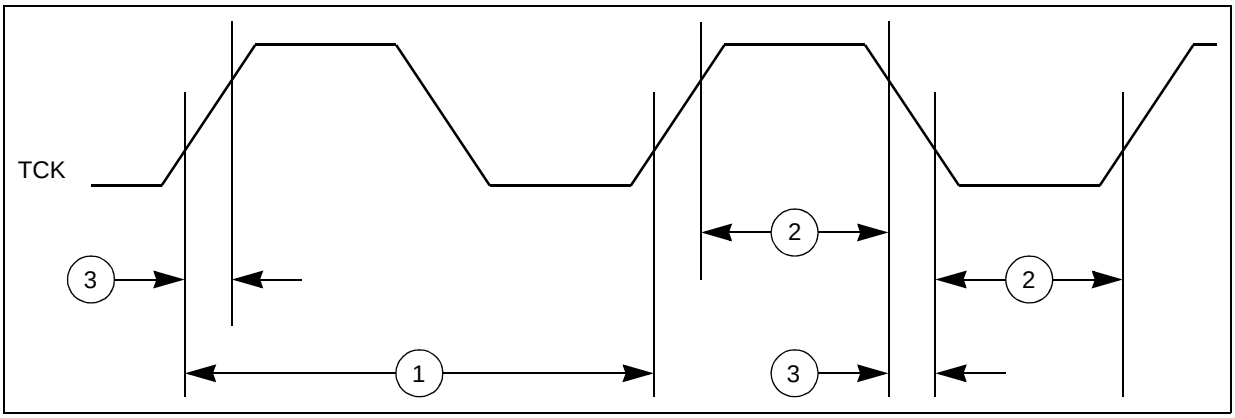

Figure 12. JTAG test clock input timing

3.17.4 Calibration bus interface timing

Table 41. Calibration bus interface maximum operating frequency

Port width	Multiplexed mode	Pin usage			Max. operating frequency
		CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	
16-bit	Yes	GPIO	GPIO	CAL_ADDR[12:30] CAL_DATA[0:15]	66 MHz(1)
16-bit	No	CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	66 MHz(1)
32-bit	Yes	CAL_WE/BE[2:3] CAL_DATA[31]	CAL_ADDR[16:30] CAL_DATA[16:30]	CAL_ADDR[0:15] CAL_DATA[0:15]	66 MHz(1)

1. Set SIU_ECCR[EBDF] to either divide by two or divide by four if the system frequency is greater than 66 MHz.

Table 42. Calibration bus operation timing(1)

#	Symbol		C	Characteristic	66 MHz(2)		Unit
					Min	Max	
1	T_C	CC	P	CLKOUT period(3)	15.2	—	ns
2	t_{CDC}	CC	T	CLKOUT duty cycle	45%	55%	T_C
3	t_{CRT}	CC	T	CLKOUT rise time	—	(4)	ns
4	t_{CFT}	CC	T	CLKOUT fall time	—	4	ns
5	t_{COH}	CC	P	CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	1.3	—	ns
6	t_{COV}	CC	P	CLKOUT Posedge to Output Signal Valid (Output Delay) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	—	9	ns
7	t_{CIS}	CC	P	Input Signal Valid to CLKOUT Posedge (Setup Time) DATA[0:31]	6.0	—	ns

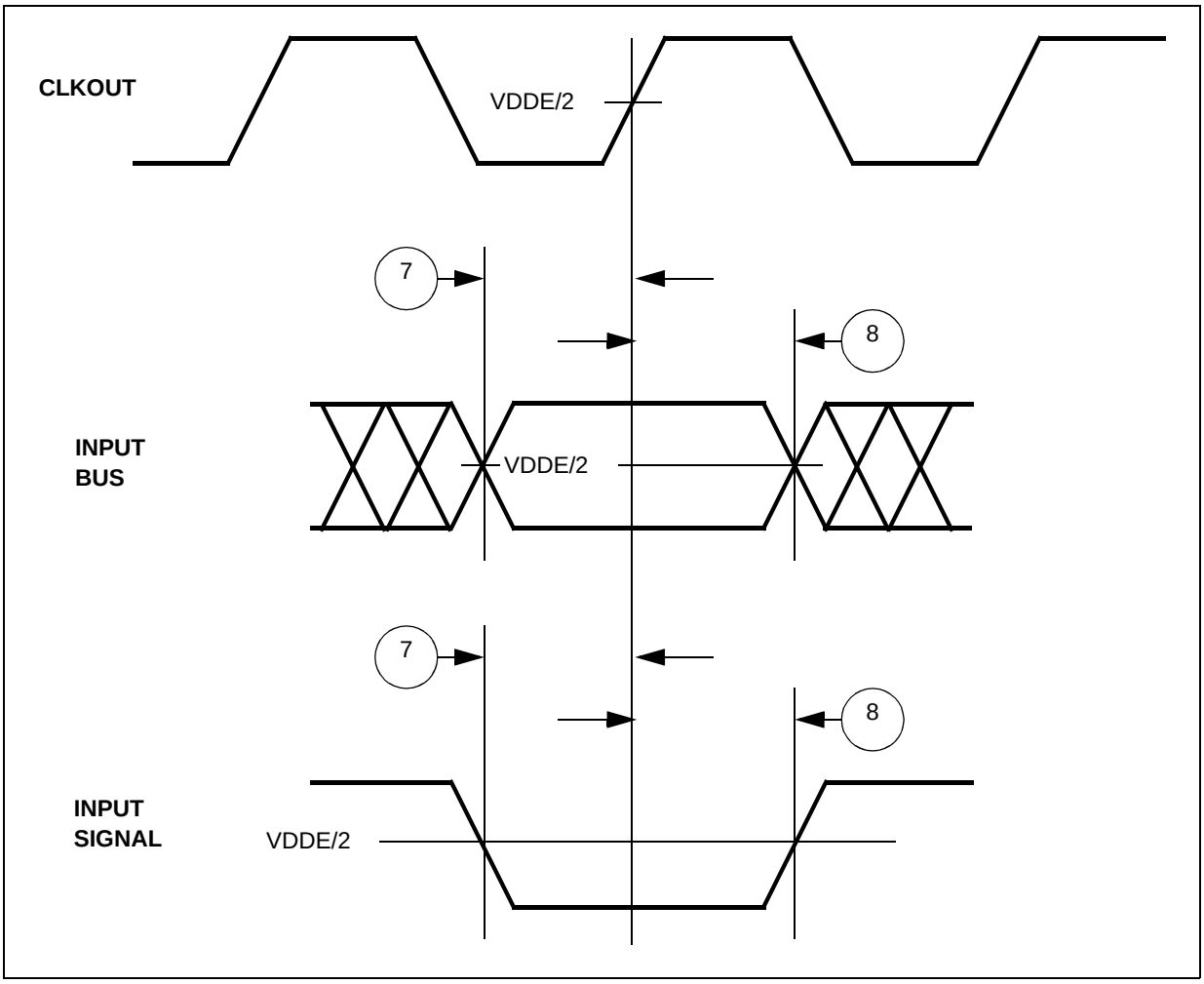

Figure 21. Synchronous input timing

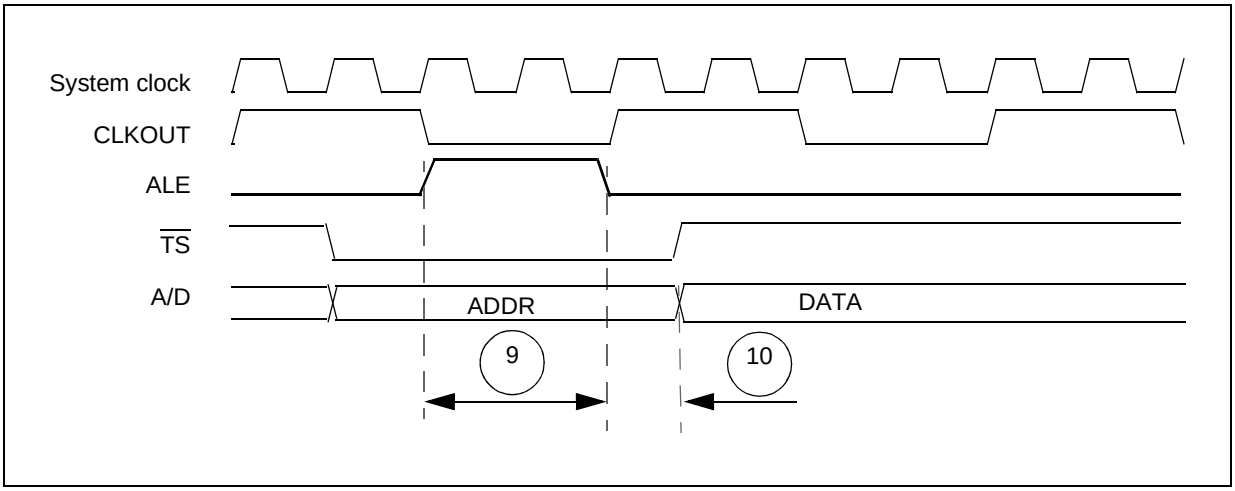

Figure 22. ALE signal timing

3.17.5 External interrupt timing (IRQ pin)

Table 43. External interrupt timing(1)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{IPWL}	IRQ Pulse Width Low	3	—	t_{CYC}
2	t_{IPWH}	IRQ Pulse Width High	3	—	t_{CYC}
3	t_{ICYC}	IRQ Edge to Edge Time(2)	6	—	t_{CYC}

1. IRQ timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

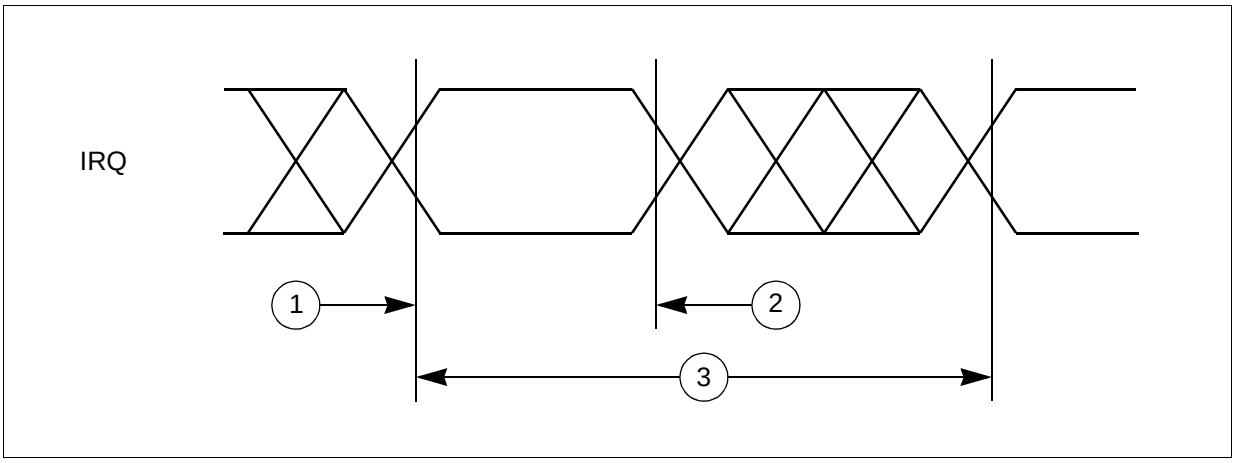

Figure 23. External interrupt timing

3.17.6 eTPU timing

Table 44. eTPU timing(1)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{ICPW}	eTPU Input Channel Pulse Width	4	—	t_{CYC}
2	t_{OCPW}	eTPU Output Channel Pulse Width(2)	2	—	t_{CYC}

1. eTPU timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.
2. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Table 48. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)(1) (continued)

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Value			Unit
					Min	Typ	Max	
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} – 6.5		9 * t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} – 6.5		8 * t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	–7.5		7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	–7.5		7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT} + t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1. SSI timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.
2. Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.
3. FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

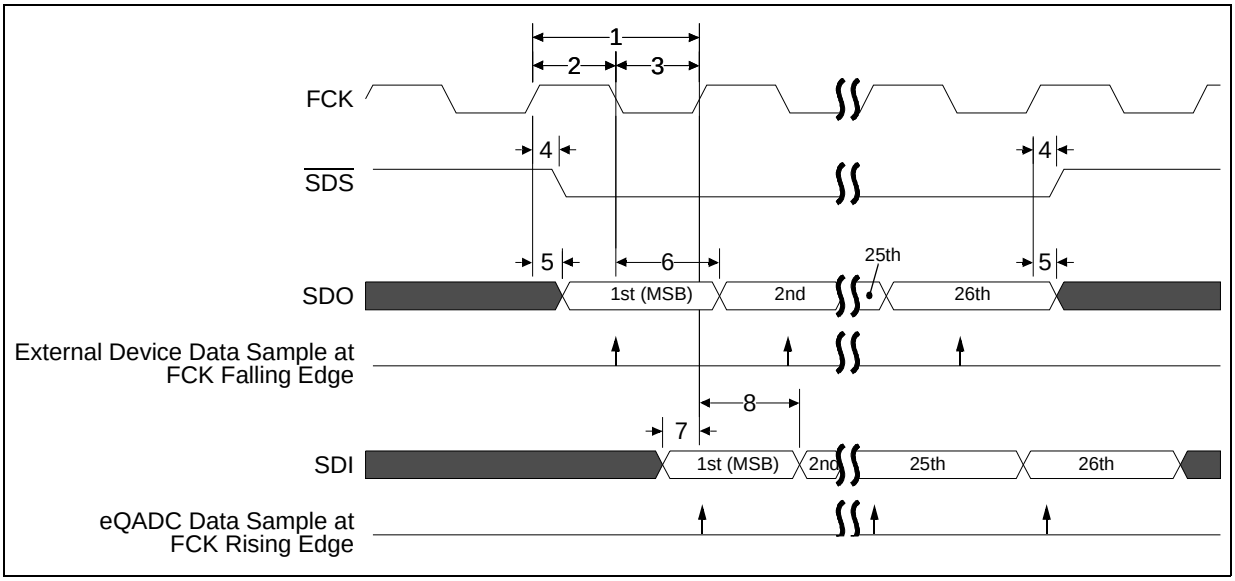

Figure 33. eQADC SSI timing

3.17.10 FlexCAN system clock source

Table 49. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	f_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

4 Packages

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP176

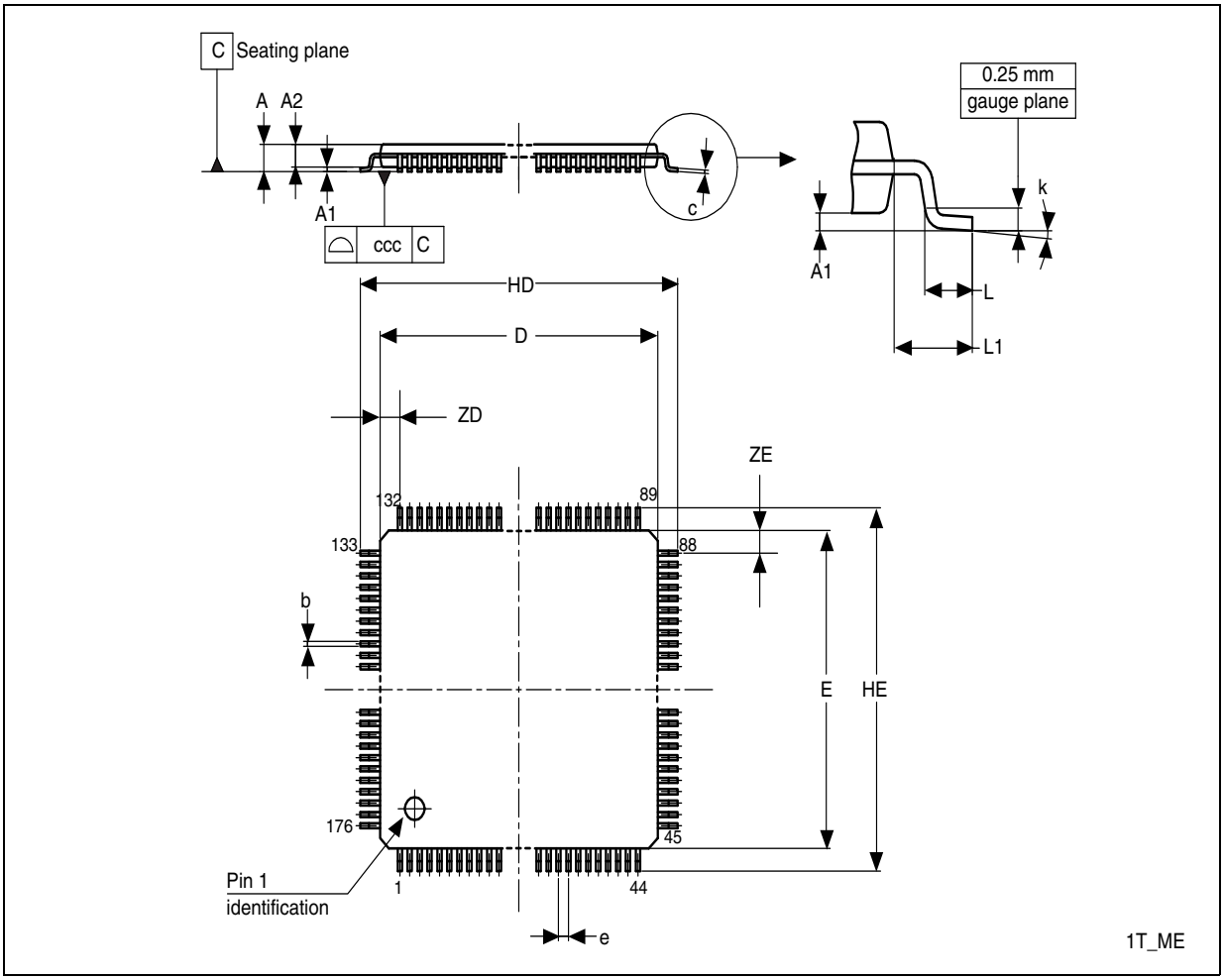

Figure 34. LQFP176 package mechanical drawing

Table 51. LQFP176 mechanical data[1]

Symbol	mm			inches[2]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.063
A1	0.050	—	0.150	0.002	—	—
A2	1.350	—	1.450	0.053	—	0.057
b	0.170	—	0.270	0.007	—	0.011
C	0.090	—	0.200	0.004	—	0.008
D	23.900	—	24.100	0.941	—	0.949
E	23.900	—	24.100	0.941	—	0.949
e	—	0.500	—	—	0.020	—
HD	25.900	—	26.100	1.020	—	1.028
HE	25.900	—	26.100	1.020	—	1.028
L[3]	0.450	—	0.750	0.018	—	0.030
L1	—	1.000	—	—	0.039	—
ZD	—	1.250	—	—	0.049	—
ZE	—	1.250	—	—	0.049	—
k	0 °	—	7 °	0 °	—	7 °
ccc	—	—	0.080	—	—	0.003

1. Controlling dimension: millimeter
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. L dimension is measured at gauge plane at 0.25 above the seating plane.

5 Ordering information

Figure 37. Product code structure