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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	150
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70l7cfbr

  - 1 reaction module (6 channels with 3 outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
  - 6 command queues
  - Trigger and DMA support
  - 688 ns minimum conversion time
- On-chip CAN/SCI Bootstrap loader with Boot Assist Module (BAM)
- Nexus: Class 3+ for core; Class 1 for eTPU
- JTAG (5-pin)
- Development Trigger Semaphore (DTS)
  - EVTO pin for communication with external tool
- Clock generation
  - On-chip 4–40 MHz main oscillator
  - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 112 general purpose I/O lines
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
- Power reduction modes: slow, stop, and standby
- Flexible supply scheme
  - 5 V single supply with external ballast
  - Multiple external supply: 5 V, 3.3 V, and 1.2 V

1.5 Feature details

1.5.1 e200z4 core

SPC564A70 devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability

  - Synthesizeable, MuxD scan design
  - ABIST/MBIST for arrays
  - Built-in Parallel Signature Unit
- Calibration support allowing an external tool to modify address mapping

1.5.2 Crossbar switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between four master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 4 master ports
  - CPU instruction bus
  - CPU data bus
  - eDMA
  - FlexRay
- 4 slave ports
  - Flash
  - Calibration bus interface
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the host processor. The hardware micro-architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation minimizes overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count

system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - 2 types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the preprogrammed memory region descriptors
  - An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
  - 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the 3 modes may be run with a crystal oscillator or an external clock reference

- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI
  - From a set of eTPU output channels, allows selection of source signals for decimation filter integrators

1.5.8 Flash memory

The SPC564A70 provides 2 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU 'loads', DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash
  - Configurable read buffering and line prefetch support
  - 4-entry 128-bit wide line read buffer
  - Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (4 words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is 2 consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

1.5.16 Enhanced serial communications interface (eSCI)

Three eSCI modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Compatible with LIN slaves from revisions 1.x and 2.0 of the LIN standard
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.17 Controller area network (FlexCAN)

The SPC564A70 MCU includes three FlexCAN blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC564A70.

The sources of the ECC errors are:

- Flash memory
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 parameter RAM)

1.5.23 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.24 Calibration bus interface

The calibration bus interface controls data transfer across the crossbar switch to/from memories or peripherals attached to the calibration tool connector in the calibration address space. The calibration bus interface is only available in the calibration tool.

Features include:

- 3.3 V ± 10% I/O (3.0 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.5.25 Power management controller (PMC)

The PMC contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1), and the 5 V supply of the regulators (VDDREG).

12	13	14	15	16	17	18	19	20	21	22	
AN27	AN28	AN35	VSSA	AN12_SDS	MDO11_ ETPUA29_O	MDO10_ ETPUA27_O	MDO8_ ETPUA21_O	VDD	VRC33	VSS	A
AN26	AN31	AN32	VSSA	AN13_SDO	MDO9_ ETPUA25_O	MDO7_ ETPUA19_O	MDO4_ ETPUA2_O	MDO0	VSS	NC2	B
AN25	AN30	AN33	VDDA	AN14_SDI	MDO5_ ETPUA4_O	MDO2	MDO1	VSS	NC2	VDD	C
AN24	AN29	AN34	VDDEH7	AN15_FCK	MDO6_ ETPUA13_O	MDO3	VSS	NC2	TCK	TDI	D
							NC2	TMS	TDO	NC	E
							NC2	JCOMP	EVTI	EVTO	F
							RDY	MCKO	MSEO0	MSEO1	G
							VDDEH6AB	GPIO[203]	GPIO[204]	DSPI_B_SIN	H
VSS	VSS	NC2					DSPI_B_ SOUT	DSPI_B_ PCS[3]	DSPI_B_ PCS[0]	DSPI_B_ PCS[1]	J
VSS	VSS	VSS					GPIO[99]	DSPI_B_ PCS[4]	DSPI_B_SCK	DSPI_B_ PCS[2]	K
VSS	VSS	VSS					DSPI_B_ PCS[5]	DSPI_A_ SOUT	DSPI_A_SIN	DSPI_A_SCK	L

Figure 6. 324-pin PBGA package ballmap (northeast, viewed from above)

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
MSEO[0]	Nexus message start/end out	P	01	224	O	VDDEH7 / MultiV	—	$\overline{\text{MSEO[0]}}$ / —	118	C15	G21
MSEO[1]	Nexus message start/end out	P	01	225	O	VDDEH7 / MultiV	—	$\overline{\text{MSEO[1]}}$ / —	117	E16	G22
RDY	Nexus ready output	P	01	226	O	VDDEH7 / MultiV	—	—	—	—	G19
JTAG											
TCK	JTAG test clock input	P	01	—	I	VDDEH7 / MultiV	TCK / Down	TCK / Down	128	C16	D21
TDI	JTAG test data input	P	01	232	I	VDDEH7 / MultiV	TDI / Up	TDI / Up	130	E14	D22
TDO	JTAG test data output	P	01	228	O	VDDEH7 / MultiV	TDO / Up	TDO / Up	123	F14	E21
TMS	JTAG test mode select input	P	01	—	I	VDDEH7 / MultiV	TMS / Up	TMS / Up	131	D14	E20
JCOMP	JTAG TAP controller enable	P	01	—	I	VDDEH7 / MultiV	JCOMP / Down	JCOMP / Down	121	F16	F20
FlexCAN											
CAN_A_TX SCI_A_TX GPIO[83]	FlexCAN A transmit eSCI A transmit GPIO	P A1 G	01 10 00	83	O O I/O	VDDEH6 / Slow	— / Up	— / Up	81	P12	Y17
CAN_A_RX SCI_A_RX GPIO[84]	FlexCAN A receive eSCI A receive GPIO	P A1 G	01 10 00	84	I I I/O	VDDEH6 / Slow	— / Up	— / Up	82	R12	AA18
CAN_B_TX DSPI_C_PCS[3] SCI_C_TX GPIO[85]	FlexCAN B transmit DSPI C peripheral chip select eSCI C transmit GPIO	P A1 A2 G	001 010 100 000	85	O O O I/O	VDDEH6 / Slow	— / Up	— / Up	88	T12	AB18
CAN_B_RX DSPI_C_PCS[4] SCI_C_RX GPIO[86]	FlexCAN B receive DSPI C peripheral chip select eSCI C receive GPIO	P A1 A2 G	001 010 100 000	86	I O I I/O	VDDEH6 / Slow	— / Up	— / Up	89	R13	AB19

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
VDDEH1AB[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1AB[19]	—	K4	H4
VDDEH4[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4[20]	—	—	—
VDDEH4A[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4A[20]	55	—	—
VDDEH4B[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4B[20]	74	—	—
VDDEH4AB[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4AB[20]	—	N9	W14
VDDEH6[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6[21]	—	—	—
VDDEH6A[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6A[21]	95	—	—
VDDEH6B[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6B[21]	110	—	—
VDDEH6AB[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6AB[21]	—	F13	H19, U19
VDDEH7[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7	—	D12	D15
VDDEH7A[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7A	125	—	—
VDDEH7B[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D19, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M11, M12, M13, M14, N9, N10, N12, N13, N14, P9, P10, P12, P13, P14, T21, T22, W4, W19, Y3, Y20, AA2, AA21, AB1, AB22

3.3 Thermal characteristics

Table 10. Thermal characteristics for 176-pin LQFP(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Single-layer board – 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Four-layer board – 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(2)	at 200 ft./min., single-layer board – 1s	30	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case(4)		5	°C/W
Ψ_{JT}	CC	D	Junction-to-package top, natural convection(5)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 208-pin LBGA(1)(2)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(3)	Single layer board – 1s(4)	39	°C/W
	CC	D		Four layer board – 2s2p(5)	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(3)	at 200 ft./min., single-layer board – 1s(5)	31	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(6)	Four-layer board – 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case(7)		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection(8)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. LBGA208 is available upon specific request. Please contact your ST sales office for details.
3. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
4. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal
5. Per JEDEC JESD51-6 with the board horizontal
6. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
7. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
8. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components that are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed-box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using *Equation 2*:

Equation 2 $T_J = T_B + (R_{\theta JB} * P_D)$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8S

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IH_S}	SR	P	Slow/medium pad I/O input high voltage	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{IH_F}	SR	P	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE} + 0.3	
V_{IH_LS}	SR	P	Multi-voltage pad I/O input high voltage in low-swing-mode(7)(8)(9)(10)	Hysteresis enabled	2.5	—	V_{DDE} + 0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDE} + 0.3	
V_{IH_HS}	SR	P	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH} + 0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH} + 0.3	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage(11)	—	—	—	0.2 * V_{DDEH}	V
V_{OL_F}	CC	P	Fast I/O output low voltage(11)	—	—	—	0.2 * V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode(7)(8)(9)(10)(11)	—	—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode(11)	—	—	—	0.2 V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium I/O output high voltage(11)	—	0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage(11)	—	0.8 V_{DDE}	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode(7)(8)(9)(10)(11)	—	2.3	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode(11)	—	0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	P	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	P	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-swing-mode multi-voltage I/O input hysteresis	Hysteresis enabled	0.25	—	—	v

20. Applies to the FCK, SDI, SDO, and SDS pins
21. This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from *Table 22* based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in *Table 22*.

Table 22. I/O pad average I_{DDE} specifications(1)

Pad type	Symbol		C	Period (ns)	Load(2) (pF)	V_{DDE} (V)	Drive/Slew rate select	I_{DDE} Avg (mA)(3)	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.25	11	9	—
		CC	D	130	50	5.25	01	2.5	—
		CC	D	650	50	5.25	00	0.5	—
		CC	D	840	200	5.25	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.25	11	14	—
		CC	D	62	50	5.25	01	5.3	—
		CC	D	317	50	5.25	00	1.1	—
		CC	D	425	200	5.25	00	3	—

8. Can be used on the tester
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
11. Selectable high/low swing I/O pad with selectable slew in high swing mode only
12. Fast pads are 3.3 V pads.
13. Also has weak pull-up/pull-down.

Table 36. Pad AC specifications (V_{DDE} = 3.0 V)(1)

Pad type		C	Output delay (ns)(2)(3) Low-to-High / High-to-Low		Rise/Fall edge (ns)(3)(4)		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium(5)(6)(7)	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11(8)
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	—							10(9)
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow(7)(10)	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	—							10(9)
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV(7)(11) (High Swing Mode)	CC	D	—	3.7/3.1	—	10/10	30	11(8)
	CC	D	—	46/49	—	42/42	200	
	—							10(9)
	CC	D	—	32	—	15/15	50	01
	CC	D	—	72	—	46/46	200	
	CC	D	—	210	—	100/100	50	00
	CC	D	—	295	—	134/134	200	
MultiV (Low Swing Mode)	Not a valid operational mode							

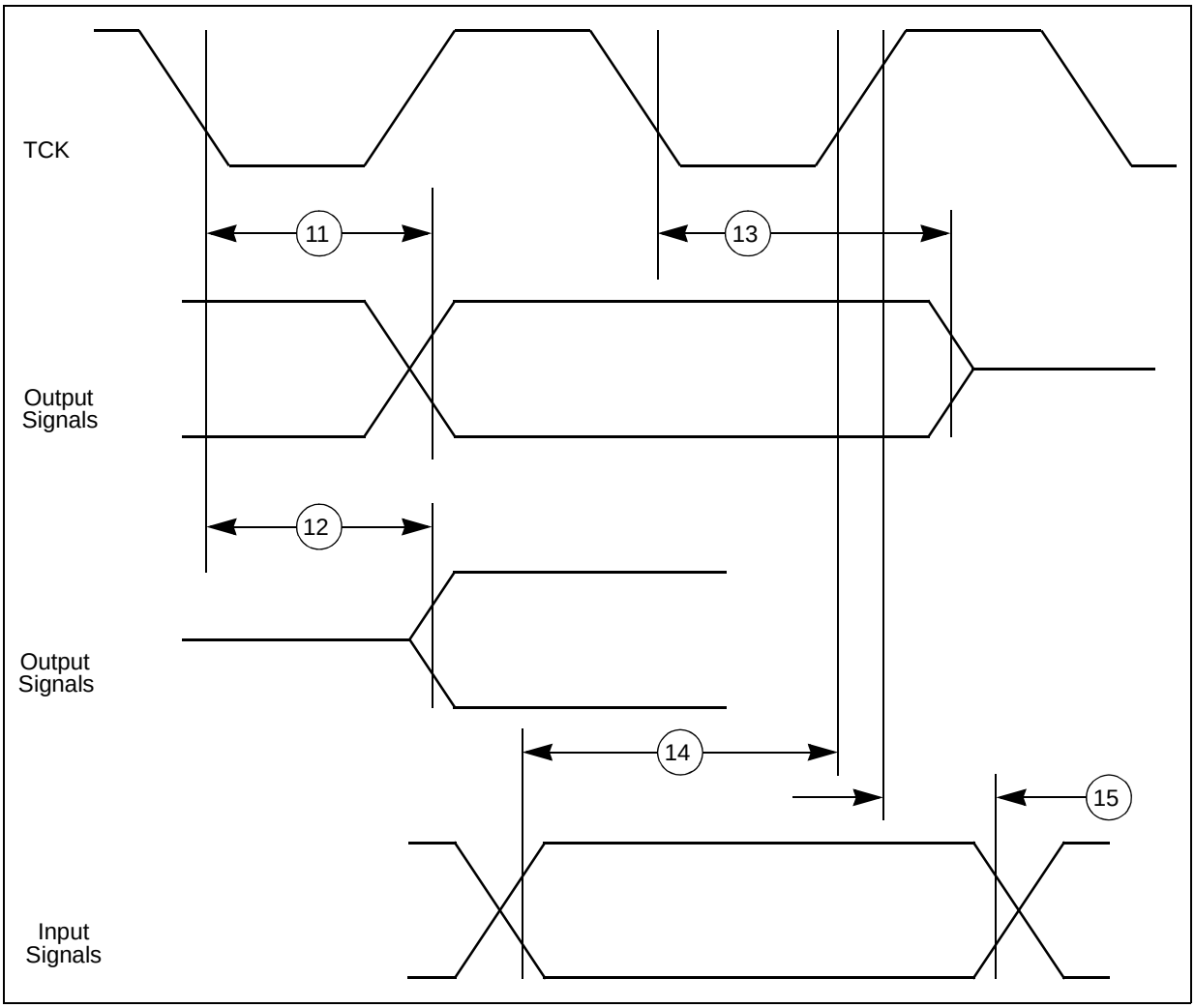

Figure 15. JTAG boundary scan timing

3.17.3 Nexus timing

Table 39. Nexus debug port timing(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{MCYC}	CC	D	MCKO Cycle Time	2(2)(3)	8	t_{CYC}
1a	t_{MCYC}	CC	D	Absolute Minimum MCKO Cycle Time	25(4)	—	ns
2	t_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid(5)	–0.1	0.35	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid(5)	–0.1	0.35	t_{MCYC}
6	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid(5)	–0.1	0.35	t_{MCYC}
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4.0	—	t_{TCYC}

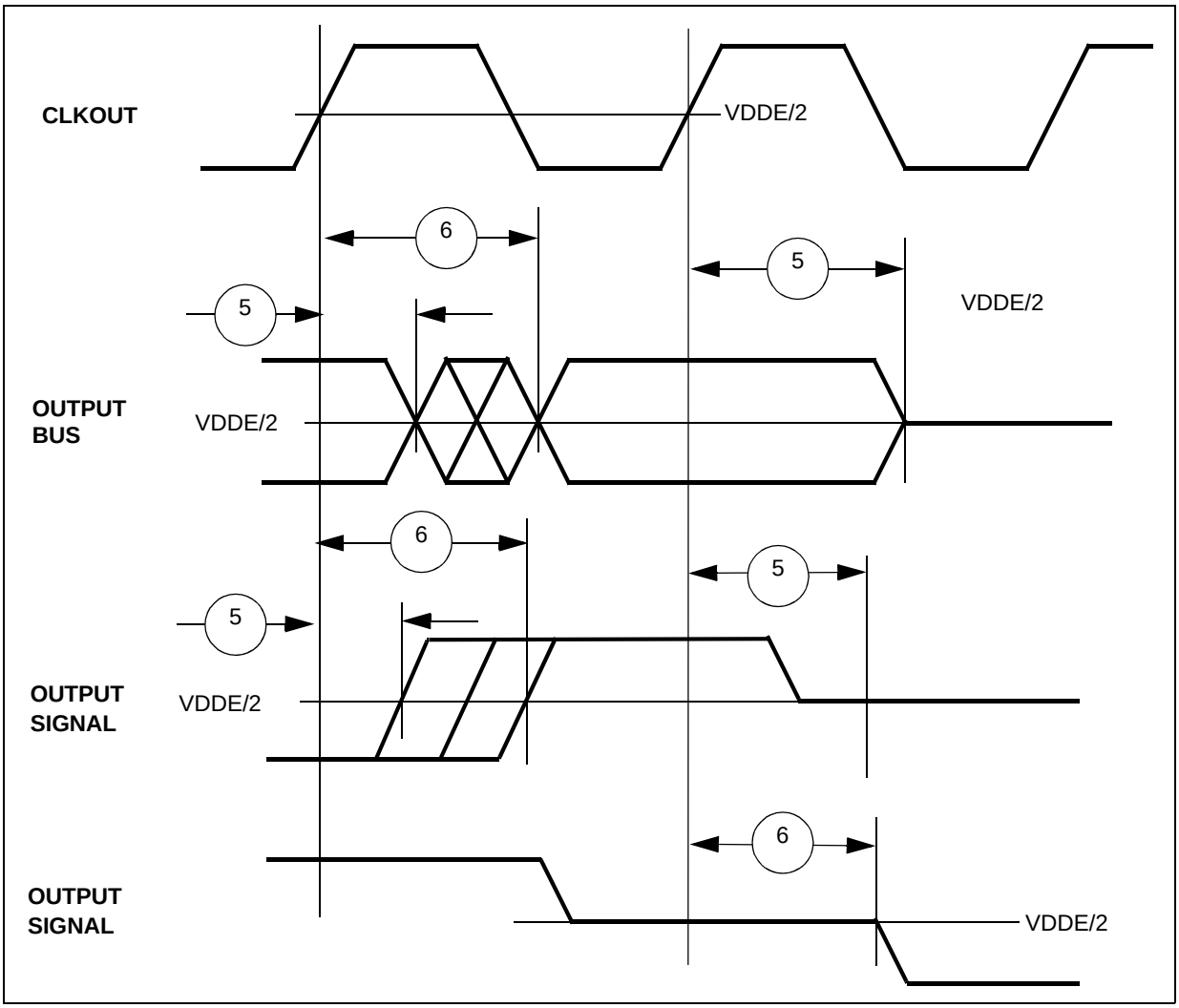

Figure 20. Synchronous output timing

Table 47. DSPI timing[1][2] (continued)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
9	t_{SUI}	CC	Data Setup Time for Inputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	20	—	ns
			D		V_{DDEH}=3–3.6 V	22	—	
			D	Slave		2	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		8	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	20	—	
			D		V_{DDEH}=3–3.6 V	22	—	
10	t_{HI}	CC	Data Hold Time for Inputs					
			D	Master (MTFE = 0)		–4	—	ns
			D	Slave		7	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		21	—	
			D	Master (MTFE = 1, CPHA = 1)		–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	—	5	ns
			D		V_{DDEH}=3–3.6 V	—	6.3	
			D	Slave	V_{DDEH}=4.75–5.25 V	—	25	
			D		V_{DDEH}=3–3.6 V	—	25.7	
			D	Master (MTFE = 1, CPHA = 0)		—	21	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	—	5	
			D		V_{DDEH}=3–3.6 V	—	6.3	
12	t_{HO}	CC	Data Hold Time for Outputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	–5	—	ns
			D		V_{DDEH}=3–3.6 V	–6.3	—	
			D	Slave		5.5	—	
			D	Master (MTFE = 1, CPHA = 0)		3	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	–5	—	
			D		V_{DDEH}=3–3.6 V	–6.3	—	

1. All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type pad_msr. DSPI signals using pad type of pad_ssr have an additional delay based on the slew rate. DSPI timing is specified at V_{DDEH} = 3.0 to 3.6 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b11.
2. Data is verified at f_{SYS} = 102 MHz and 153 MHz (100 MHz and 150 MHz + 2% frequency modulation).
3. The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two SPC564A70 devices communicating over a DSPI link.
4. The actual minimum SCK cycle time is limited by pad performance.
5. For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.
6. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].
7. Timing met when PCSSCK = 3 (01), and CSSCK = 2 (0000)

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