Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	150
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70l7cfby

1.5 Feature details

1.5.1 e200z4 core

SPC564A70 devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability

system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - 2 types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the preprogrammed memory region descriptors
  - An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
  - 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- 3 modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the 3 modes may be run with a crystal oscillator or an external clock reference

  - Prefill mode to precondition the filter before the sample window opens
  - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
  - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface (SSI) to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based queues
  - Supports 6 queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter

1.5.15 Deserial serial peripheral interface (DSPI)

The DSPI block provides a synchronous serial interface for communication between the SPC564A70 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the SPC564A70 MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHz for SOUT and SCK pins for DSPI_B and DSPI_C
- Support for downstream Micro Second Channel (MSC) with Timed Serial Bus (TSB) configuration on DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels, and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI module can generate and check parity in a serial frame

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC564A70.

The sources of the ECC errors are:

- Flash memory
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 parameter RAM)

1.5.23 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.24 Calibration bus interface

The calibration bus interface controls data transfer across the crossbar switch to/from memories or peripherals attached to the calibration tool connector in the calibration address space. The calibration bus interface is only available in the calibration tool.

Features include:

- 3.3 V ± 10% I/O (3.0 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.5.25 Power management controller (PMC)

The PMC contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1), and the 5 V supply of the regulators (VDDREG).

2.3 PBGA324 ballmap

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	VDD	VSTBY	AN37	AN11	VDDA	VSSA	AN1	AN5	VRH	VRL
B	VRC33	VSS	VDD	AN36	AN39	AN19	AN16	AN0	AN4	REFBYPC	AN23
C	ETPUA30	ETPUA31	VSS	VDD	AN38	AN17	AN20	AN21	AN3	AN7	AN22
D	ETPUA28	ETPUA29	ETPUA26	VSS	VDD	AN8	AN9	AN10	AN18	AN2	AN6
E	ETPUA24	ETPUA27	ETPUA25	ETPUA21							
F	ETPUA23	ETPUA22	ETPUA17	ETPUA18							
G	ETPUA20	ETPUA19	ETPUA14	ETPUA13							
H	ETPUA16	ETPUA15	ETPUA10	VDDEH1AB							
J	ETPUA12	ETPUA11	ETPUA6	ETPUA9					VSS	VSS	VSS
K	ETPUA8	ETPUA7	ETPUA2	ETPUA5					VSS	VSS	VSS
L	ETPUA4	ETPUA3	ETPUA0	ETPUA1					VSS	VSS	VSS

Figure 4. 324-pin PBGA package ballmap (northwest, viewed from above)

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CAN_C_TX DSPI_D_PCS[3] GPIO[87]	FlexCAN C transmit DSPI D peripheral chip select GPIO	P A1 G	01 10 00	87	O O I/O	VDDEH6 / Medium	— / Up	— / Up	101	K13	P19
CAN_C_RX DSPI_D_PCS[4] GPIO[88]	FlexCAN C receive DSPI D peripheral chip select GPIO	P A1 G	01 10 00	88	I O I/O	VDDEH6 / Slow	— / Up	— / Up	98	L14	R20
eSCI											
SCI_A_TX EMIOS13[16] GPIO[89]	eSCI A transmit eMIOS channel GPIO	P A1 G	01 10 00	89	O O I/O	VDDEH6 / Medium	— / Up	— / Up	100	J14	N20
SCI_A_RX EMIOS15[16] GPIO[90]	eSCI A receive eMIOS channel GPIO	P A1 G	01 10 00	90	I O I/O	VDDEH6 / Medium	— / Up	— / Up	99	K14	P20
SCI_B_TX DSPI_D_PCS[1] GPIO[91]	eSCI B transmit DSPI D peripheral chip select GPIO	P A1 G	01 10 00	91	O O I/O	VDDEH6 / Medium	— / Up	— / Up	87	L13	R21
SCI_B_RX DSPI_D_PCS[5] GPIO[92]	eSCI B receive DSPI D peripheral chip select GPIO	P A1 G	01 10 00	92	I O I/O	VDDEH6 / Medium	— / Up	— / Up	84	M13	T19
SCI_C_TX GPIO[244]	eSCI C transmit GPIO	P G	01 00	244	O I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	W18
SCI_C_RX GPIO[245]	eSCI C receive GPIO	P G	01 00	245	I I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	Y19
DSPI											
DSPI_A_SCK[17] DSPI_C_PCS[1] GPIO[93]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	93	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L22
DSPI_A_SIN[17] DSPI_C_PCS[2] GPIO[94]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	94	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L21
DSPI_A_SOUT[17] DSPI_C_PCS[5] GPIO[95]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	95	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L20

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
AN7 DAN3–	Single Ended Analog Input Negative Terminal Differential Input	P	—	—	I	VDDA / Analog Pull-up/down	I / —	AN[7] / —	165	C8	C10
AN8 ANW	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[8] / —	9	B3	D6
AN9 ANX	Single-ended Analog Input External Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[9] / —	5	A2	D7
AN10 ANY	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[10] / —	—	—	D8
AN11 ANZ	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA / Analog	I / —	AN[11] / —	4	A3	A5
AN12 - SDS MA0 ETPUA19_O $\overline{SDS}$	Single-ended Analog Input MUX Address 0 eTPU A channel (output only) eQADC Serial Data Select	P A1 A2 G	001 010 100 000	215	I O O I/O	VDDEH7 / Medium	I / —	AN[12] / —	148	A12	A16
AN13 - SDO MA1 ETPUA21_O SDO	Single-ended Analog Input MUX Address 1 eTPU A channel (output only) eQADC Serial Data Out	P A1 A2 G	001 010 100 000	216	I O O O	VDDEH7 / Medium	I / —	AN[13] / —	147	B12	B16
AN14 - SDI MA2 ETPUA27_O SDI	Single-ended Analog Input MUX Address 2 eTPU A channel (output only) eQADC Serial Data In	P A1 A2 G	001 010 100 000	217	I O O I	VDDEH7 / Medium	I / —	AN[14] / —	146	C12	C16
AN15 - FCK FCK ETPUA29_O	Single-ended Analog Input eQADC Free Running Clock eTPU A channel (output only)	P A1 A2	001 010 100	218	I O O	VDDEH7 / Medium	I / —	AN[15] / —	145	C13	D16
AN16	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[16] / —	3	C6	B7
AN17	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[17] / —	2	C4	C6
AN18	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[18] / —	1	D5	D9
AN19	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[19] / —	—	—	B6

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the SPC564A70 series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Thermal characteristics

Table 10. Thermal characteristics for 176-pin LQFP(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Single-layer board – 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Four-layer board – 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(2)	at 200 ft./min., single-layer board – 1s	30	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case(4)		5	°C/W
Ψ_{JT}	CC	D	Junction-to-package top, natural convection(5)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 208-pin LBGA(1)(2)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(3)	Single layer board – 1s(4)	39	°C/W
	CC	D		Four layer board – 2s2p(5)	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(3)	at 200 ft./min., single-layer board – 1s(5)	31	°C/W
	CC	D		at 200 ft./min., four-layer board – 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(6)	Four-layer board – 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case(7)		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection(8)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. LBGA208 is available upon specific request. Please contact your ST sales office for details.
3. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
4. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal
5. Per JEDEC JESD51-6 with the board horizontal
6. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
7. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
8. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.6 Power management control (PMC) and power on reset (POR) electrical specifications

Table 15. PMC operating conditions and external regulators supply voltage

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
1	T_J	SR	—	Junction temperature	–40	27	150	°C
2	V_{DDREG}	SR	—	PMC 5 V supply voltage VDDREG	4.75	5	5.25	V
3	V_{DD}	CC	C	Core supply voltage 1.2 V VDD when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)(1)	1.26 (2)	1.3	1.32	V
3a	—	CC	C	Core supply voltage 1.2 V VDD when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	I_{VDD}	CC	C	Voltage regulator core supply maximum required DC output current	400	—	—	mA
5	V_{DD33}	CC	C	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)(3)	3.3	3.45	3.6	V
5a	—	CC	C	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	CC	C	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

1. An internal regulator controller can be used to regulate the core supply.
2. The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.
3. An internal regulator can be used to regulate the 3.3 V supply.

Table 16. PMC electrical characteristics

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
1	V_{BG}	CC	C	Nominal bandgap voltage reference	—	1.219	—	V
1a	—	CC	C	Untrimmed bandgap reference voltage	V_{BG} – 7%	V_{BG}	V_{BG} + 6%	V
1b	—	CC	C	Trimmed bandgap reference voltage (5 V, 27 °C)	V_{BG} – 10mV	V_{BG}	V_{BG} + 10mV	V
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm/°C
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm/V
2	V_{DD}	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage(1)	—	1.28	—	V
2a	—	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage variation at power-on reset	V_{DD} – 6%	V_{DD}	V_{DD} + 10%	V
2b	—	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage variation after power-on reset	V_{DD} – 10%(2)	V_{DD}	V_{DD} + 3%	V

Table 16. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f – 35%	Por3.3V_f	Por3.3V_f + 35%	V
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V VDDREG supply	—	4.290	—	V
8a	—	CC	C	Variation of LVI for rising 5 V VDDREG supply at power-on reset	Lvi5p0 – 6%	Lvi5p0	Lvi5p0 + 6%	V
8b	—	CC	C	Variation of LVI for rising 5 V VDDREG supply power-on reset	Lvi5p0 – 3%	Lvi5p0	Lvi5p0 + 3%	V
8c	—	CC	C	Trimming step LVI 5 V	—	20	—	mV
8d	Lvi5p0_h	CC	C	LVI 5 V hysteresis	—	60	—	mV
9	Por5V_r	CC	C	Nominal POR for rising 5 V VDDREG supply	—	2.67	—	V
9a	—	CC	C	Variation of POR for rising 5 V VDDREG supply	Por5V_r – 35%	Por5V_r	Por5V_r + 35%	V
9b	Por5V_f	CC	C	Nominal POR for falling 5 V VDDREG supply	—	2.47	—	V
9c	—	CC	C	Variation of POR for falling 5 V VDDREG supply	Por5V_f – 35%	Por5V_f	Por5V_f + 35%	V

1. Using external ballast transistor.
2. Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.
3. LVI for falling supply is calculated as LVI rising – LVI hysteresis.
4. Lvi1p2 tracks DC target variation of internal V_{DD} regulator. Minimum and maximum Lvi1p2 correspond to minimum and maximum V_{DD} DC target respectively.
5. With internal load up to Idd3p3
6. The Lvi3p3 specs are also valid for the V_{DDEH} LVI
7. Lvi3p3 tracks DC target variation of internal V_{DD33} regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum V_{DD33} DC target respectively.
8. The 3.3V POR specs are also valid for the V_{DDEH} POR

3.6.1 Regulator example

In designs where the SPC564A70 microcontroller's internal regulators are used, a ballast is required for generation of the 1.2 V internal supply. No ballast is required when an external 1.2 V supply is used.

3.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 18. Transistor recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60–550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200–600(1)	mV
V_{BE}	Base-to-emitter voltage	0.4–1.0	V

1. Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}

3.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues such as latch-up or excessive current spikes, the state of the I/O pins during power up/down varies according to *Table 19* for all pins with pad type fast, and *Table 20* for all pins with pad type medium, slow, and multi-voltage.

Table 19. Power sequence pin states—Fast type pads

V_{DDE}	V_{RC33}	V_{DD}	Pin state
Low	X	X	Low
V_{DDE}	Low	X	High
V_{DDE}	V_{RC33}	Low	High impedance
V_{DDE}	V_{RC33}	V_{DD}	Functional

Table 20. Power sequence pin states—Medium, slow and multi-voltage type pads

V_{DDEH}	V_{DD}	Pin state
Low	X	Low
V_{DDEH}	Low	High impedance
V_{DDEH}	V_{DD}	Functional

Table 26. PLLMRFM electrical specifications(1)

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{LCK}	CC	D	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	D	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS}	CC	D	Modulation depth	Center spread	±0.25	±4.0	% f_{sys}
f_{DS}		D		Down spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency(16)	—	—	100	kHz

1. All values given are initial design targets and subject to change.
2. Considering operation with PLL not bypassed
3. All internal registers retain data at 0 Hz.
4. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
5. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
6. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
7. This value is determined by the crystal manufacturer and board design.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
9. Proper PC board layout procedures must be followed to achieve specifications.
10. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. Proper PC board layout procedures must be followed to achieve specifications.
13. This parameter is guaranteed by design rather than 100% tested.
14. V_{IHEXT} cannot exceed V_{RC33} in external reference mode.
15. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
16. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.11 Temperature sensor electrical characteristics

Table 27. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	C	Temperature monitoring range		–40	—	150	°C

3.17 AC timing

3.17.1 Reset and configuration pin timing

Table 37. Reset and configuration pin timing(1)

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{RPW}	$\overline{\text{RESET}}$ Pulse Width	10	—	t_{CYC}
2	t_{GPW}	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	2	—	t_{CYC}
3	t_{RCSU}	PLLREF, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	10	—	t_{CYC}
4	t_{RCH}	PLLREF, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	0	—	t_{CYC}

1. Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.14 V to 1.32 V, $T_A = T_L$ to T_H.

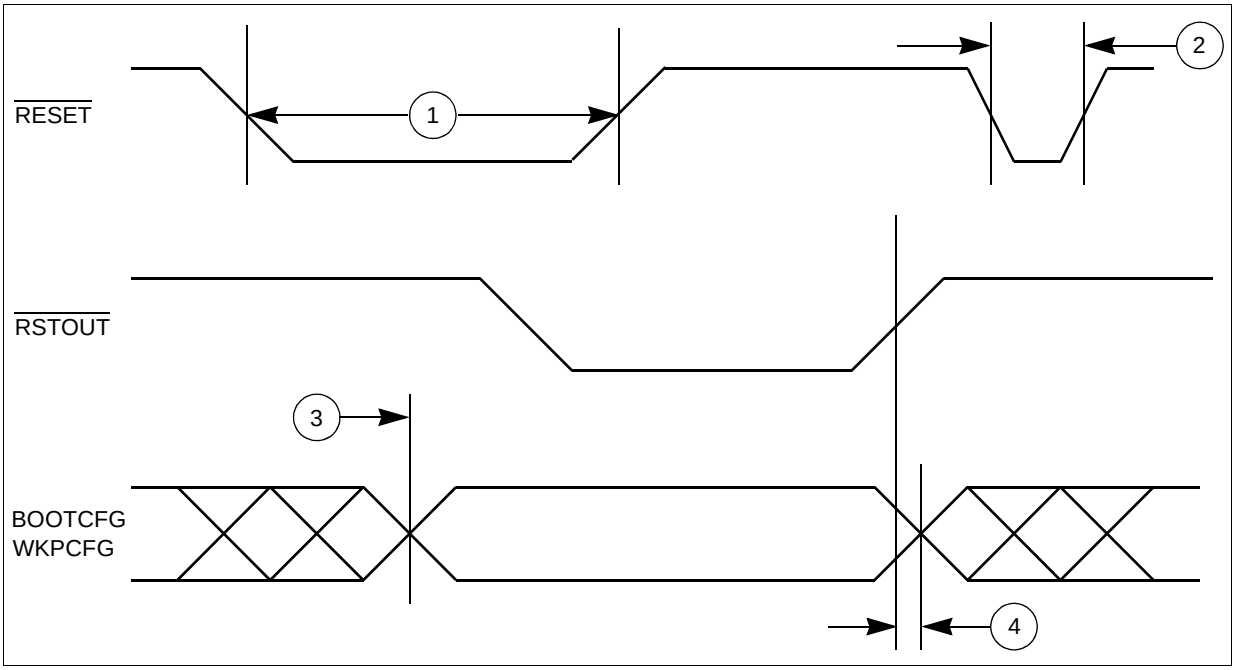

Figure 11. Reset and configuration pin timing

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns

3.17.4 Calibration bus interface timing

Table 41. Calibration bus interface maximum operating frequency

Port width	Multiplexed mode	Pin usage			Max. operating frequency
		CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	
16-bit	Yes	GPIO	GPIO	CAL_ADDR[12:30] CAL_DATA[0:15]	66 MHz(1)
16-bit	No	CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	66 MHz(1)
32-bit	Yes	CAL_WE/BE[2:3] CAL_DATA[31]	CAL_ADDR[16:30] CAL_DATA[16:30]	CAL_ADDR[0:15] CAL_DATA[0:15]	66 MHz(1)

1. Set SIU_ECCR[EBDF] to either divide by two or divide by four if the system frequency is greater than 66 MHz.

Table 42. Calibration bus operation timing(1)

#	Symbol		C	Characteristic	66 MHz(2)		Unit
					Min	Max	
1	T_C	CC	P	CLKOUT period(3)	15.2	—	ns
2	t_{CDC}	CC	T	CLKOUT duty cycle	45%	55%	T_C
3	t_{CRT}	CC	T	CLKOUT rise time	—	(4)	ns
4	t_{CFT}	CC	T	CLKOUT fall time	—	4	ns
5	t_{COH}	CC	P	CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	1.3	—	ns
6	t_{COV}	CC	P	CLKOUT Posedge to Output Signal Valid (Output Delay) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	—	9	ns
7	t_{CIS}	CC	P	Input Signal Valid to CLKOUT Posedge (Setup Time) DATA[0:31]	6.0	—	ns

3.17.7 eMIOS timing

Table 45. eMIOS timing(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

1. eMIOS timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

3.17.8 DSPI timing

DSPI channel frequency support for the SPC564A70 MCU is shown in *Table 46*. Timing specifications are in *Table 47*.

Table 46. DSPI channel frequency support

System clock (MHz)	DSPI Use Mode	Maximum usable frequency (MHz)	Notes
150	LVDS	37.5	Use sysclock /4 divide ratio
	Non-LVDS	18.75	Use sysclock /8 divide ratio
120	LVDS	40	Use sysclock /3 divide ratio. Gives 33/66 duty cycle. Use DSPI configuration DBR = 0b1 (double baud rate), BR = 0b0000 (scaler value 2) and PBR = 0b01 (prescaler value 3).
	Non-LVDS	20	Use sysclock /6 divide ratio
80	LVDS	40	Use sysclock /2 divide ratio
	Non-LVDS	20	Use sysclock /4 divide ratio

Table 47. DSPI timing(1)(2)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
1	t_{SCK}	CC	D	SCK Cycle Time(3)(4)(5)		24.4 ns	2.9 ms	—
2	t_{CSC}	CC	D	PCS to SCK Delay(6)		22(7)	—	ns
3	t_{ASC}	CC	D	After SCK Delay(8)		21(9)	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle		$(½t_{SC}) - 2$	$(½t_{SC}) + 2$	ns
5	t_A	CC	D	Slave Access Time ($\overline{SS}$ active to SOUT driven)		—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)		—	25	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time		4(10)	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time		5(11)	—	ns

Table 47. DSPI timing[1][2] (continued)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
9	t_{SUI}	CC	Data Setup Time for Inputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	20	—	ns
			D		V_{DDEH}=3–3.6 V	22	—	
			D	Slave		2	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		8	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	20	—	
			D		V_{DDEH}=3–3.6 V	22	—	
10	t_{HI}	CC	Data Hold Time for Inputs					
			D	Master (MTFE = 0)		–4	—	ns
			D	Slave		7	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		21	—	
			D	Master (MTFE = 1, CPHA = 1)		–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	—	5	ns
			D		V_{DDEH}=3–3.6 V	—	6.3	
			D	Slave	V_{DDEH}=4.75–5.25 V	—	25	
			D		V_{DDEH}=3–3.6 V	—	25.7	
			D	Master (MTFE = 1, CPHA = 0)		—	21	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	—	5	
			D		V_{DDEH}=3–3.6 V	—	6.3	
12	t_{HO}	CC	Data Hold Time for Outputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	–5	—	ns
			D		V_{DDEH}=3–3.6 V	–6.3	—	
			D	Slave		5.5	—	
			D	Master (MTFE = 1, CPHA = 0)		3	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	–5	—	
			D		V_{DDEH}=3–3.6 V	–6.3	—	

1. All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type pad_msr. DSPI signals using pad type of pad_ssr have an additional delay based on the slew rate. DSPI timing is specified at V_{DDEH} = 3.0 to 3.6 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b11.
2. Data is verified at f_{SYS} = 102 MHz and 153 MHz (100 MHz and 150 MHz + 2% frequency modulation).
3. The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two SPC564A70 devices communicating over a DSPI link.
4. The actual minimum SCK cycle time is limited by pad performance.
5. For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.
6. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].
7. Timing met when PCSSCK = 3 (01), and CSSCK = 2 (0000)

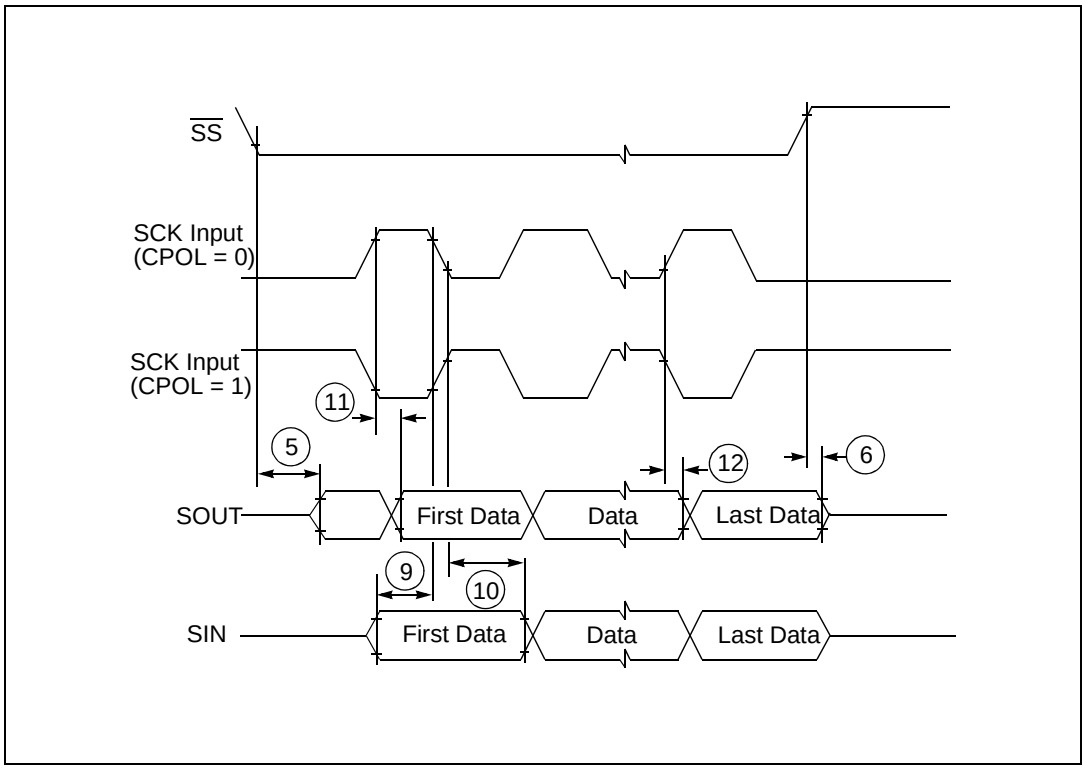

Figure 31. DSPI modified transfer format timing (slave, CPHA = 1)

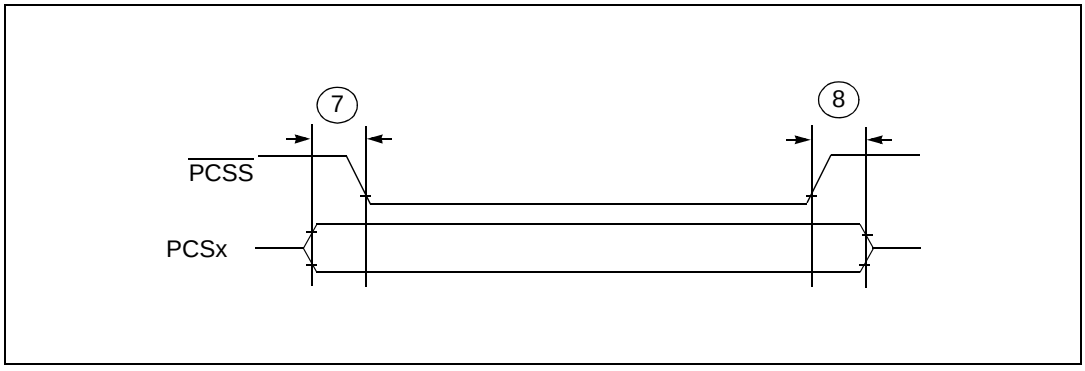

Figure 32. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.17.9 eQADC SSI timing

Table 48. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)(1)

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Value			Unit
					Min	Typ	Max	
1	f_{FCK}	CC	D	FCK Frequency (2)(3)	1/17		1/2	f_{SYS_CLK}
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2		17	t_{SYS_CLK}

4 Packages

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP176

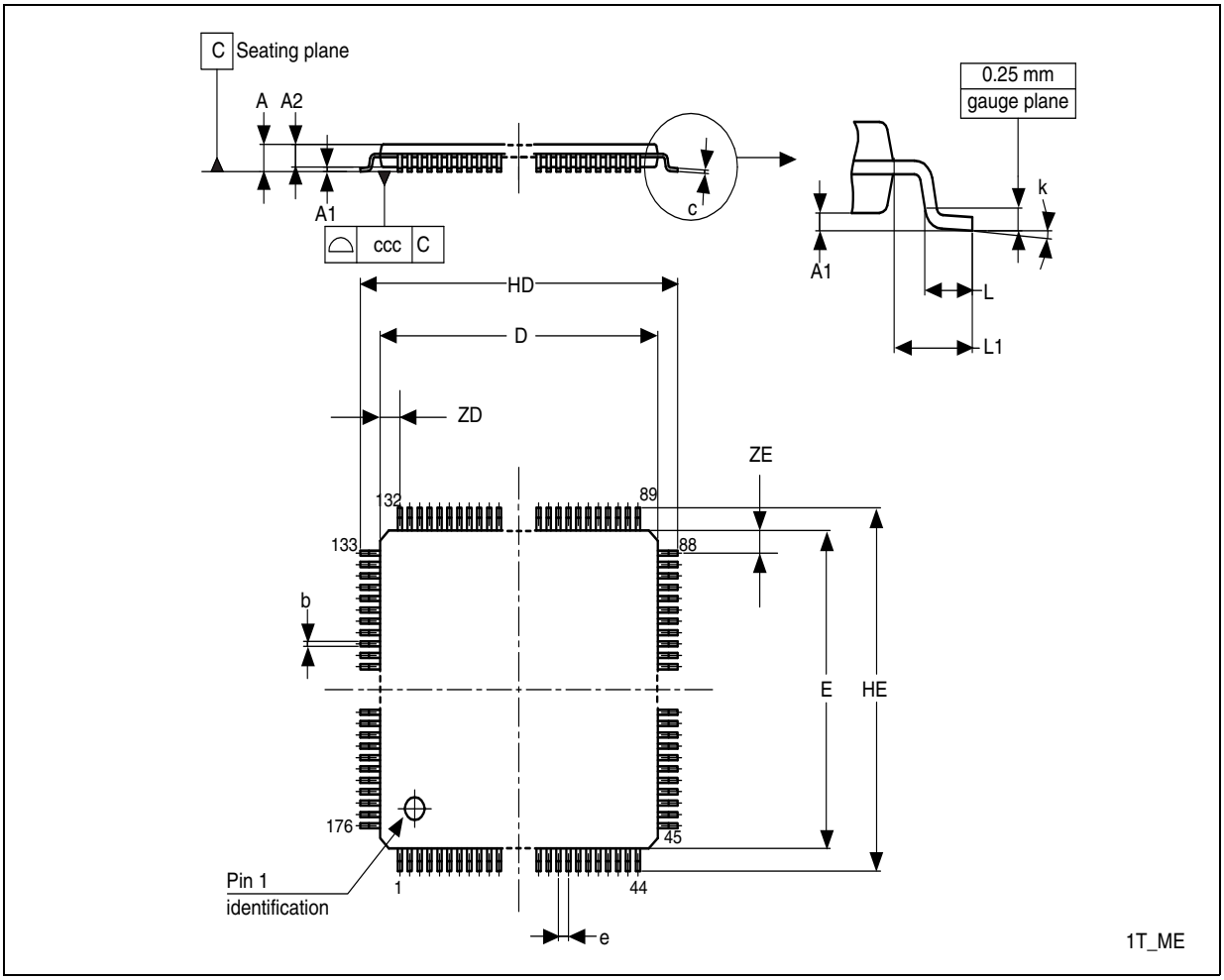

Figure 34. LQFP176 package mechanical drawing

Table 54. Document revision history (continued)

Date	Revision	Changes
11-Apr-2012	2 (continued)	Added *Table 40 (Nexus debug port operating frequency)* *Table 40 (Nexus debug port operating frequency)*, added a footnote near the value of t_{AAI} *Table 45 (eMIOS timing)*: changed minumum value of t_{MOPW} to 1 removed the footnote of t_{MOPW} Merged "DSPI timing (V_{DDEH} = 3.0 to 3.6 V)" and "DSPI timing (V_{DDEH} = 4.5 to 5.5V)" tables into *Table 47 (DSPI timing)* and changed all parameter classification to D *Table 48 (eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V))* changed all parameter classification to D *Table 52 (LBGA208 mechanical data)* deleted Notes column and moved all footnote next to relative references *Table 53 (PBGA324 package mechanical data)* deleted Notes column and moved all footnote next to relative references [[ST_Specific]] *Table 12 (Thermal characteristics for 324-pin PBGA)*, updated values In *Section 3.6, Power management control (PMC) and power on reset (POR) electrical specifications*, deleted the "Voltage regulator controller (V_{RC}) electrical specifications" Updated *Section 4.2.1, LQFP176*
06-Jun-2012	3	Minor editorial changes and improvements throughout. In *Section 2.4, Signal summary*, *Table 4 (SPC564A70 signal properties)*, updated the following properties for the Nexus pins: – Added a footnote to the "Nexus" title for this pin group. – Added a footnote to the "Name" entry for $\overline{\text{EVTO}}$. – Updated the "Status During reset" entry for $\overline{\text{EVTO}}$. In *Section 3.2, Maximum ratings*, *Table 9 (Absolute maximum ratings)*, removed the "TBD - To be defined" footnote. In *Section 3.8, DC electrical specifications*, *Table 21 (DC electrical specifications)*, removed the "TBD - To be defined" footnote. In *Section 3.9, I/O pad current specifications*, *Table 22 (I/O pad average IDDE specifications)*: – Updated values and replaced TBDs with numerical data. – Removed the "TBD - To be defined" footnote. In *Section 3.9.1, I/O pad VRC33 current specifications*, *Table 23 (I/O pad VRC33 average IDDE specifications)*: – Updated values and replaced TBDs with numerical data. – Removed the "TBD - To be defined" footnote. In *Section 3.14, Platform flash controller electrical characteristics*, *Table 32 (APC, RWSC, WWSC settings vs. frequency of operation)*, removed the "TBD - To be defined" footnote. In *Table 54 (Document revision history)*, removed extraneous text from the Revision 2 entry.
18-Sep-2013	4	Updated Disclaimer.