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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	150
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70l7cobr

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Table 2. SPC564A70 device feature summary (continued)

Feature		SPC564A70	SPC564A80
Core Nexus		Class 3+	
SRAM		128 KB	192 KB
Flash		2 MB	4 MB
Flash fetch accelerator		4 × 128-bit	4 × 256-bit
External bus		None	16-bit (incl. 32-bit muxed)
Calibration bus		16-bit (incl. 32-bit muxed)	
DMA		64 channels	
DMA Nexus		None	
Serial		3	
	eSCI_A	Yes (MSC uplink)	
	eSCI_B	Yes (MSC uplink)	
	eSCI_C	Yes	
CAN		3	
	CAN_A	64 message buffers	
	CAN_B	64 message buffers	
	CAN_C	64 message buffers	
SPI		3	
	Micro Second Channel (MSC) bus downlink	Yes	
	DSPI_A	No	
	DSPI_B	Yes (with LVDS)	
	DSPI_C	Yes (with LVDS)	
	DSPI_D	Yes	
FlexRay		Yes	
System timers		5 PIT channels 4 STM channels 1 Software Watchdog	
eMIOS		24 channels	
eTPU		32-channel eTPU2	
	Code memory	14 KB	
	Data memory	3 KB	
	Reaction module	6 channels	
Interrupt controller		485 channels(1)	
ADC		40 channels	

1.5 Feature details

1.5.1 e200z4 core

SPC564A70 devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability

- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test MISC (multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.13 Reaction module (REACM)

The REACM provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The REACM has the following features:

- 6 reaction channels with peak and hold control blocks
- Each channel output is a bus of 3 signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions.

1.5.14 Enhanced queued analog-to-digital converter (eQADC)

The eQADC block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog-to-digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of

  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of 0 to 8 bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full-featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wakeup on bus activity

1.5.18 FlexRay

The SPC564A70 includes one dual-channel FlexRay module that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev A. Features include:

- Single channel support
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 message buffers, each configurable as:
  - Receive message buffer
  - Single-buffered transmit message buffer
  - Double-buffered transmit message buffer (combines two single-buffered message buffers)
- 2 independent receive FIFOs
  - 1 receive FIFO per channel
  - Up to 255 entries for each FIFO
- ECC support

1.5.19 System timers

The system timers include two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

Periodic interrupt timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to provide system ‘tick’ signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock and one is clocked by the crystal clock. This one channel is also referred to as Real-Time Interrupt (RTI) and is used to wake up the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered; used to restart system clock after predefined time-out period
- Each channel optionally able to generate an interrupt request or a trigger event (to trigger eQADC queues) when timer reaches zero

System timer module (STM)

The STM is designed to implement the software task monitor as defined by AUTOSAR[(a)]. It consists of a single 32-bit counter, clocked by the system clock, and four independent timer

a. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CAL_RD_WR	Calibration data bus	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[0]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_WE[1]	Calibration write enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 / Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A1	01 10	343	O O	VDDE12 / Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[7] / —	—	—	—
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 / Fast	—	CAL_MDO[11] / —	—	—	—
NEXUS[14]											
$\overline{\text{EVTI}}$	Nexus event in	P	01	231	I	VDDEH7 / MultiV	— / Up	$\overline{\text{EVTI}}$ / Up	116	E15	F21
$\overline{\text{EVTO}}$[15]	Nexus event out	P	01	227	O	VDDEH7 / MultiV	ABR/Up	$\overline{\text{EVTO}}$ / —	120	D15	F22

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CLKOUT	System clock output	P	01	229	O	VDDE12 / Fast	—	CLKOUT	—	—	AA20
ENGCLK	Engineering clock output	P	01	214	O	VDDE12 / Fast	—	ENGCLK	—	T14	AB21
Power / Ground											
VDDREG	Voltage regulator supply	—		—	I	5 V	I / —	VDDREG	10	K16	M22
VRCCTL	Voltage regulator control output	—		—	O	—	O / —	VRCCTL	11	N14	V20
VRC33[18]	Internal regulator output	—		—	O	3.3 V	I/O / —	VRC33	13	A15, D1, N6, N12	A21, B1, P4, W7, Y22
	Input for external 3.3 V supply	—		—	I	3.3 V					
VDDA	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA	6	A4, B11	A6, C15
VSSA	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA	7	A5, A11	A7, A15, B15
VDDPLL	FMPLL supply voltage	—		—	I	1.2 V	I / —	VDDPLL	91	R16	W22
VSTBY	Power supply for standby RAM	—		—	I	0.9 V – 6 V	I / —	VSTBY	12	C1	A3
VDD	Core supply for input or decoupling	—		—	I	1.2 V	I / —	VDD	33, 45, 62, 103, 132, 149, 176	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15	A2, A20, B3, C4, C22, D5, V19, W5, W20, Y4, Y21, AA3, AA22, AB2
VDDE12	External supply input for calibration bus interfaces	—		—	I	3.0 V – 3.6 V	I / —	VDDE12	—	—	—
VDDE5	External supply input for ENGCLK and CLKOUT	—		—	I	3.0 V – 3.6 V	I / —	VDDE5	—	T13	W17, Y18, AA19, AB20
VDDE-EH	External supply for EBI interfaces	—		—	I	3.0 V – 5.0 V	I / —	VDDE-EH	—	—	R3, W2
VDDEH1A[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1A[19]	31	—	—
VDDEH1B[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1B[19]	41	—	—

Table 6. Signal details (continued)

Signal	Module or function	Description
DSPI_C_SCK_LVDS– DSPI_C_SCK_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
DSPI_C_SOUT_LVDS– DSPI_C_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
DSPI_B_PCS[0] DSPI_C_PCS[0] DSPI_D_PCS[0]	DSPI_B – DSPI_D	Peripheral chip select when device is in master mode—slave select when used in slave mode
DSPI_B_PCS[1:5] DSPI_C_PCS[1:5] DSPI_D_PCS[1:5]	DSPI_B – DSPI_D	Peripheral chip select when device is in master mode—not used in slave mode
DSPI_B_SCK DSPI_C_SCK DSPI_D_SCK	DSPI_B – DSPI_D	DSPI clock—output when device is in master mode; input when in slave mode
DSPI_B_SIN DSPI_C_SIN DSPI_D_SIN	DSPI_B – DSPI_D	DSPI data in
DSPI_B_SOUT DSPI_C_SOUT DSPI_D_SOUT	DSPI_B – DSPI_D	DSPI data out
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
AN[0:7]/DAN+	eQADC	Differential analog input pair for analog-to-digital converter with pull-up/pull-down functionality
AN[0:7]/DAN–	eQADC	Differential analog input pair for analog-to-digital converter with pull-up/pull-down functionality
FCK	eQADC	eQADC free running clock for eQADC SSI
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX SCI_C_RX	eSCI_A – eSCI_C	eSCI receive
SCI_A_TX SCI_B_TX SCI_C_TX	eSCI_A – eSCI_C	eSCI transmit

6. All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.
7. Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.
8. AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).
9. Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.
10. Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.
11. Total injection current for all pins (including both digital and analog) must not exceed 25 mA.
12. Total injection current for all analog input pins must not exceed 15 mA.
13. Lifetime operation at these specification limits is not guaranteed.
14. Solder profile per IPC/JEDEC J-STD-020D
15. Moisture sensitivity per JEDEC test method A112

Table 16. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
2c	—	CC	C	Trimming step V_{DD}	—	20	—	mV
2d	I_{VRCCTL}	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA
3	Lvi1p2	CC	C	Nominal LVI for rising core supply(3)	—	1.160	—	V
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset(4)	1.120	1.200	1.280	V
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset(4)	Lvi1p2 – 3%	Lvi1p2	Lvi1p2 + 3%	V
3c	—	CC	C	Trimming step LVI core supply	—	20	—	mV
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis	—	40	—	mV
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r – 35%	Por1.2V_r	Por1.2V_r + 35%	V
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f – 35%	Por1.2V_f	Por1.2V_f + 35%	V
5	V_{DD33}	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V
5a	—	CC	C	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset	V_{DD33} – 8.5%	V_{DD33}	V_{DD33} + 7%	V
5b	—	CC	C	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset(5)	V_{DD33} – 7.5%	V_{DD33}	V_{DD33} + 7%	V
5c	—	CC	C	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω
5d	Idd3p3	CC	C	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA
5e	Vdd33 ILim	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply(6)	—	3.090	—	V
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset(7)	Lvi3p3 – 6%	Lvi3p3	Lvi3p3 + 6%	V
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset(7)	Lvi3p3 – 3%	Lvi3p3	Lvi3p3 + 3%	V
6c	—	CC	C	Trimming step LVI 3.3 V	—	20	—	mV
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis	—	60	—	mV
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply(8)	—	2.07	—	V
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r – 35%	Por3.3V_r	Por3.3V_r + 35%	V

Table 21. DC electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{ACT_F}	CC	P	Fast I/O weak pull-up/down current(16)	1.62 V–1.98 V	36	—	120	µA
		P		2.25 V–2.75 V	34	—	139	
		P		3.0 V–3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pull-up current	V_{DDE} = 3.0 – 3.6 V(7), multi-voltage, high swing mode only	10	—	75	µA
		C		4.75 V–5.25 V	25	—	175	
$I_{ACT\_MV\_PD}$	CC	C	Multi-voltage pad weak pull-down current	V_{DDE} = 3.0 – 3.6 V(7), multi-voltage, all process corners, high swing mode only	10	—	60	µA
		C		4.75 V–5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current(17)	—	–2.5	—	2.5	µA
I_{IC}	SR	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	SR	P	Analog input current, channel off, AN[0:7](18)	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins18	—	–150	—	150	
C_L	CC	D	Load capacitance (fast I/O)(19)	DSC(PCR[8:9]) = 0b00	—	—	10	pF
		D		DSC(PCR[8:9]) = 0b01	—	—	20	
		D		DSC(PCR[8:9]) = 0b10	—	—	30	
		D		DSC(PCR[8:9]) = 0b11	—	—	50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—	—	7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—	—	10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins(20))	—	—	—	12	pF
$R_{PUPD200K}$	SR	C	Weak pull-up/down resistance(21), 200 kΩ option	—	130	—	280	kΩ

Table 30. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)(5)	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2(5)	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1. Applies only to differential channels.
2. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.
3. At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.
4. Guaranteed 10-bit mono tonicity.
5. Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

(1)	SWSC Value
98	0
153	1

1. Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1)

Max. Flash Operating Frequency (MHz)(2)	APC(3)	RWSC(3)	WWSC
20 MHz	0b000	0b000	0b01
61 MHz	0b001	0b001	0b01
90 MHz	0b010	0b010	0b01
123 MHz	0b011	0b011	0b01
153 MHz	0b100	0b100	0b01

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. Max frequencies including 2% PLL FM.
3. APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications(1)

#	Symbol		C	Parameter	Value				Unit
					Min	Typ	Initial max(2)	Max(3)	
1	$T_{dwprogram}$	CC	C	Double Word (64 bits) Program Time	—	30	—	500	µs
2	$T_{pprogram}$	CC	C	Page Program Time(4)	—	40	160	500	µs
3	$T_{16kpperase}$	CC	C	16 KB Block Pre-program and Erase Time	—	—	1000	5000	ms
5	$T_{64kpperase}$	CC	C	64 KB Block Pre-program and Erase Time	—	—	1800	5000	ms
6	$T_{128kpperase}$	CC	C	128 KB Block Pre-program and Erase Time	—	—	2600	7500	ms
7	$T_{256kpperase}$	CC	C	256 KB Block Pre-program and Erase Time	—	—	5200	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (V_{DDE} = 4.75 V)(1)

Name		C	Output delay (ns)(2)(3) Low-to-High / High-to-Low		Rise/Fall edge (ns)(3)(4)		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB, LSB
Medium(5)(6)(7)	CC	D	4.6/3.7	12/12	2.2/2.2	12/12	50	11(8)
	—							10(9)
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow(7)(10)	CC	D	7.3/5.7	19/18	4.4/4.3	20/20	50	11(8)
	—							10(9)
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV(11) (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11(8)
	—							10(9)
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11(8)
Fast(12)	—							
Standalone input buffer(13)	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	—

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V, $T_A = T_L$ to T_H.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad V_{OL} and V_{OH} values are the same as those of the slew controlled output pads.
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
7. Output delay is shown in *Figure 9* and *Figure 10*. Add a maximum of one system clock to the output delay for delay with respect to system clock.

3.17.4 Calibration bus interface timing

Table 41. Calibration bus interface maximum operating frequency

Port width	Multiplexed mode	Pin usage			Max. operating frequency
		CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	
16-bit	Yes	GPIO	GPIO	CAL_ADDR[12:30] CAL_DATA[0:15]	66 MHz(1)
16-bit	No	CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	66 MHz(1)
32-bit	Yes	CAL_WE/BE[2:3] CAL_DATA[31]	CAL_ADDR[16:30] CAL_DATA[16:30]	CAL_ADDR[0:15] CAL_DATA[0:15]	66 MHz(1)

1. Set SIU_ECCR[EBDF] to either divide by two or divide by four if the system frequency is greater than 66 MHz.

Table 42. Calibration bus operation timing(1)

#	Symbol		C	Characteristic	66 MHz(2)		Unit
					Min	Max	
1	T_C	CC	P	CLKOUT period(3)	15.2	—	ns
2	t_{CDC}	CC	T	CLKOUT duty cycle	45%	55%	T_C
3	t_{CRT}	CC	T	CLKOUT rise time	—	(4)	ns
4	t_{CFT}	CC	T	CLKOUT fall time	—	4	ns
5	t_{COH}	CC	P	CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	1.3	—	ns
6	t_{COV}	CC	P	CLKOUT Posedge to Output Signal Valid (Output Delay) CAL_ADDR[12:30] CAL_CS[0], CAL_CS[2:3] CAL_DATA[0:15] CAL_OE CAL_RD_$\overline{WR}$ CAL_TS CAL_$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	—	9	ns
7	t_{CIS}	CC	P	Input Signal Valid to CLKOUT Posedge (Setup Time) DATA[0:31]	6.0	—	ns

Table 42. Calibration bus operation timing(1) (continued)

#	Symbol		C	Characteristic	66 MHz(2)		Unit
					Min	Max	
8	t_{CIH}	CC	P	CLKOUT Posedge to Input Signal Invalid (Hold Time) DATA[0:31]	1.0	—	ns
9	t_{APW}	CC	P	ALE Pulse Width(5)	6.5	—	ns
10	t_{AAI}	CC	P	ALE Negated to Address Invalid(5)	1.5(6)	—	ns

1. Calibration bus timing specified at f_{SYS} = 150 MHz and 100 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. The calibration bus is limited to half the speed of the internal bus. The maximum calibration bus frequency is 66 MHz. The bus division factor should be set accordingly based on the internal frequency being used.
3. Signals are measured at 50% V_{DDE}
4. Refer to fast pad timing in *Table 35* and *Table 36* (different values for 1.8 V vs. 3.3 V).
5. Measured at 50% of ALE
6. When CAL_TS pad is used for CAL_ALE function the hold time is 1 ns instead of 1.5 ns.

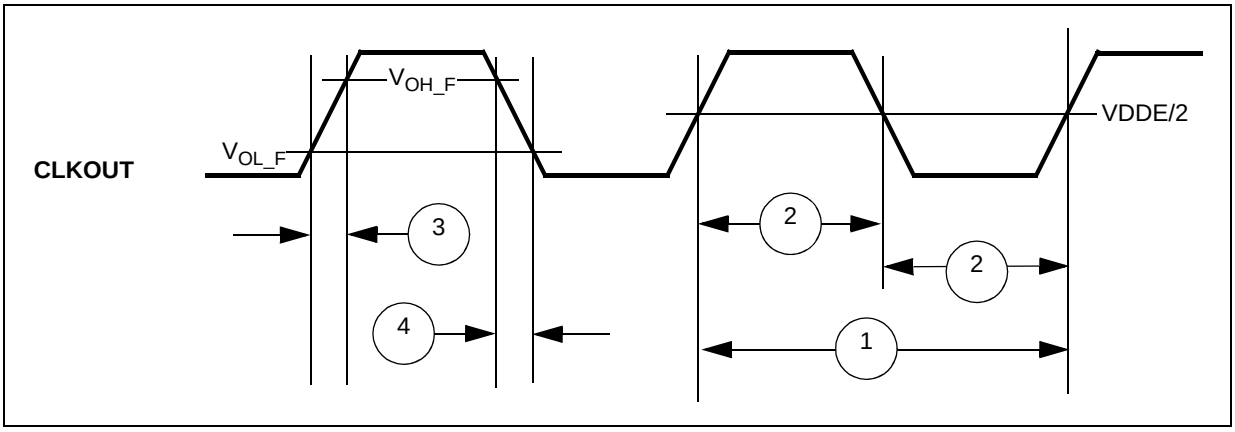

Figure 19. CLKOUT timing

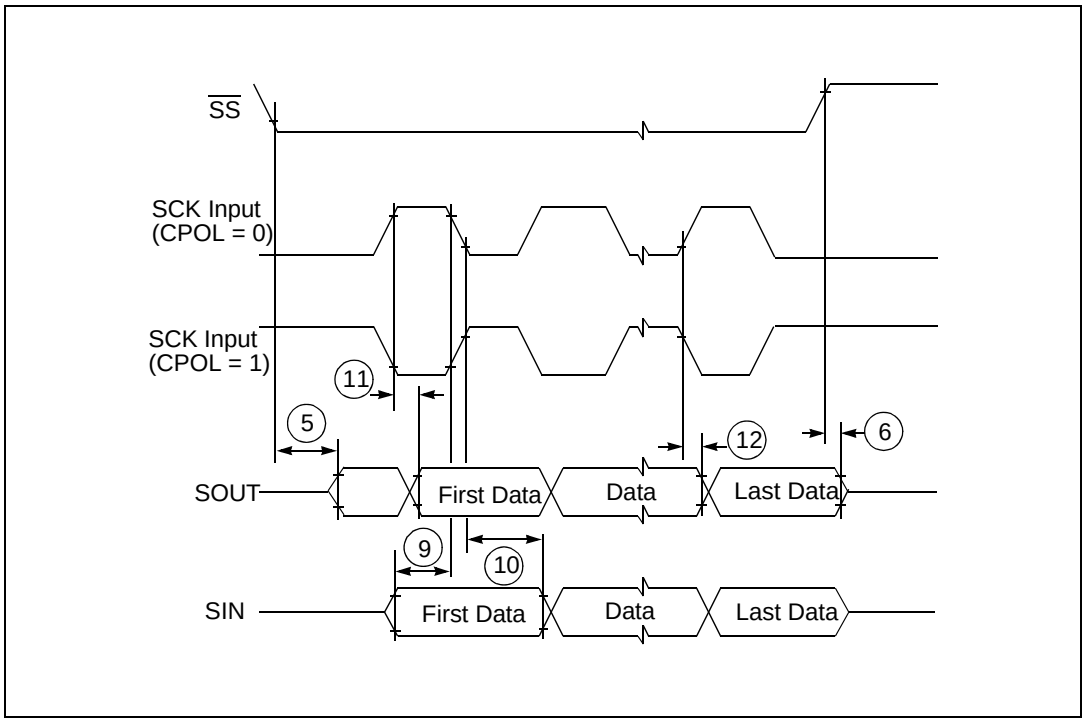

Figure 27. DSPI classic SPI timing (slave, CPHA = 1)

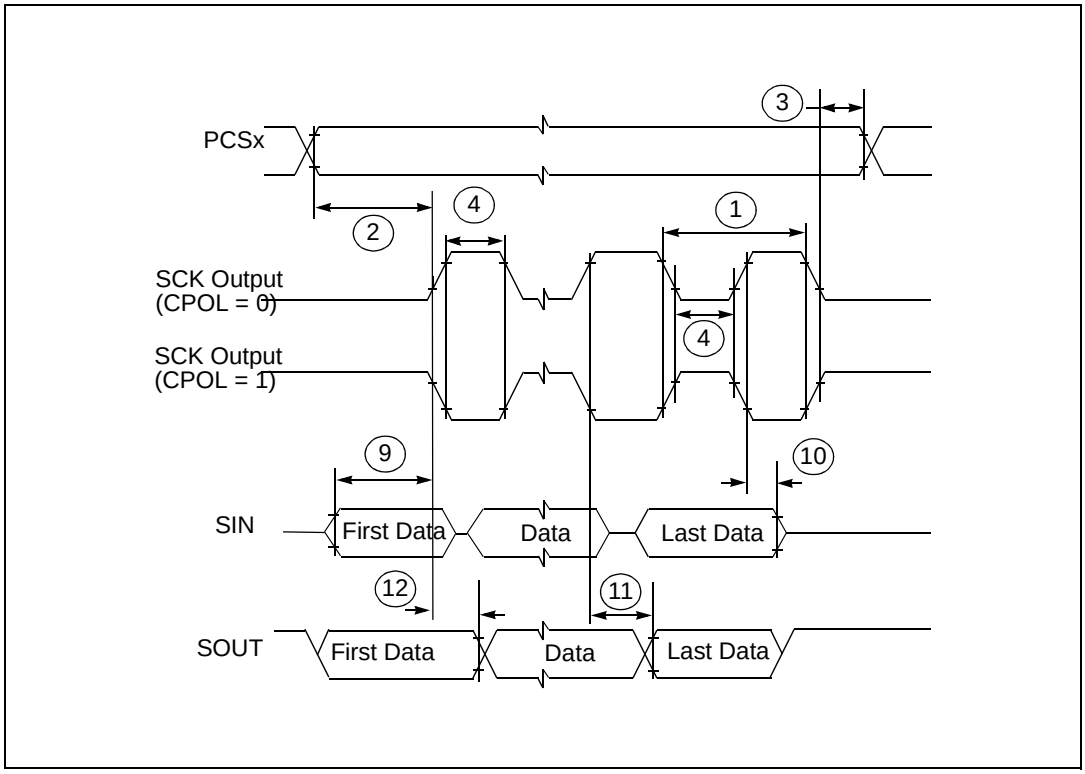

Figure 28. DSPI modified transfer format timing (master, CPHA = 0)

5 Ordering information

Figure 37. Product code structure