Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	150
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70l7coby

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC564A70 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This microcontroller is a 32-bit system-on-chip (SoC) device intended for use in mid-range engine control and automotive transmission control applications.

It is compatible with devices in ST's SPC56xx family and offers performance and capability above that of the SPC563M devices.

The microcontroller's e200z4 host processor core is built on the Power Architecture technology and designed specifically for embedded applications. In addition to the Power Architecture technology, this core supports instructions for digital signal processing (DSP).

The device has two levels of memory hierarchy consisting of 8 KB of instruction cache, backed by a 128 KB on-chip SRAM and a 2 MB internal flash memory.

For development, the device includes a calibration bus that is accessible only when using the STMicroelectronics calibration tool.

1.3 Device feature summary

Table 2 summarizes the SPC564A70 features and compares them to those of the SPC564A80.

Table 2. SPC564A70 device feature summary

Feature		SPC564A70	SPC564A80
Process		90 nm	
Core		e200z4	
	SIMD	Yes	
	VLE	Yes	
	Cache	8 KB instruction	
	Non-Maskable Interrupt (NMI)	NMI and Critical Interrupt	
	MMU	24-entry	
	MPU	16-entry	
	Crossbar switch	4 × 4	5 × 4
	Core performance	0–150 MHz	
Windowing software watchdog		Yes	

Table 2. SPC564A70 device feature summary (continued)

Feature		SPC564A70	SPC564A80
Core Nexus		Class 3+	
SRAM		128 KB	192 KB
Flash		2 MB	4 MB
Flash fetch accelerator		4 × 128-bit	4 × 256-bit
External bus		None	16-bit (incl. 32-bit muxed)
Calibration bus		16-bit (incl. 32-bit muxed)	
DMA		64 channels	
DMA Nexus		None	
Serial		3	
	eSCI_A	Yes (MSC uplink)	
	eSCI_B	Yes (MSC uplink)	
	eSCI_C	Yes	
CAN		3	
	CAN_A	64 message buffers	
	CAN_B	64 message buffers	
	CAN_C	64 message buffers	
SPI		3	
	Micro Second Channel (MSC) bus downlink	Yes	
	DSPI_A	No	
	DSPI_B	Yes (with LVDS)	
	DSPI_C	Yes (with LVDS)	
	DSPI_D	Yes	
FlexRay		Yes	
System timers		5 PIT channels 4 STM channels 1 Software Watchdog	
eMIOS		24 channels	
eTPU		32-channel eTPU2	
	Code memory	14 KB	
	Data memory	3 KB	
	Reaction module	6 channels	
Interrupt controller		485 channels(1)	
ADC		40 channels	

1.5 Feature details

1.5.1 e200z4 core

SPC564A70 devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability

- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 System integration unit (SIU)

The SPC564A70 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin

2 Pinout and signal description

This section contains the pinouts for all production packages for the SPC564A70 device. For pin signal descriptions, please refer to *Table 4*

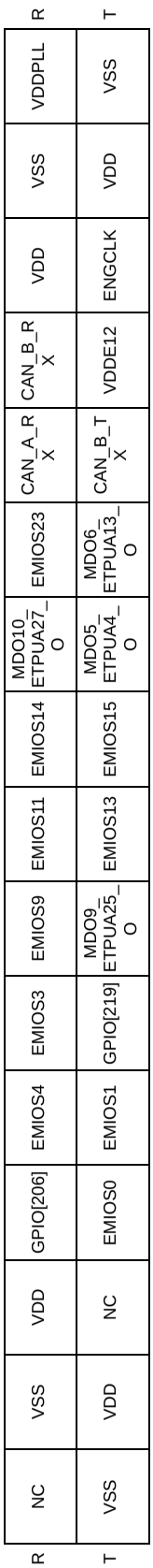
Note: Any pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

2.2 LBGA208 ballmap[b]

Figure 3. 208-pin LBGA package ballmap (viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_SOUT	DSPI_B_PCS[3]	DSPI_B_SIN	DSPI_B_PCS[0]	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO[99]	DSPI_B_PCS[4]	DSPI_B_PCS[2]	DSPI_B_PCS[1]	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_PCS[5]	SCI_A_TX	GPIO[98]	DSPI_B_SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ETPUA19_O	VRC33	VSS	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO[207]	NC	EMIOS6	EMIOS8	MDO11_ETPUA29_O	MDO4_ETPUA2_O	MDO8_ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P

b. LBGA208 is available upon specific request. Please contact your ST sales office for details.


R
T
NC
VSS
VDD
VSS
R
T
VSS
VDD
NC
EMIOS0
EMIOS1
GPIO[219]
ETPUA25_O
EMIOS15
EMIOS13
ETPUA4_O
ETPUA13_O
CAN_B_TX
VDDE12
ENGCLK
VDD
VDDPLL
VSS
VDD
GPIO[206]
EMIOS4
EMIOS3
MDO9_
EMIOS9
EMIOS11
EMIOS14
MDO10_
EMIOS23
CAN_A_RX
CAN_B_RX
VDD
VSS
R
T

VSS	VSS	VSS					DSPI_A_ PCS[1]	DSPI_A_ PCS[0]	GPIO[98]	VDDREG	M
VSS	VSS	VSS					DSPI_A_ PCS[4]	SCI_A_TX	DSPI_A_ PCS[5]	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							WKPCFG	CAN_C_RX	SCI_B_TX	RESET	R
							SCI_B_RX	BOOTCFG1	VSS	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG0	EXTAL	U
							VDD	VRCCTL	PLLREF	XTAL	V
EMIOS2	EMIOS8	VDDEH4AB	EMIOS12	EMIOS21	VDDE12	SCI_C_TX	VSS	VDD	NC	VDDPLL	W
EMIOS6	EMIOS10	EMIOS15	EMIOS17	EMIOS22	CAN_A_TX	VDDE12	SCI_C_RX	VSS	VDD	VRC33	Y
EMIOS5	EMIOS9	EMIOS13	EMIOS16	EMIOS19	EMIOS23	CAN_A_RX	VDDE12	CLKOUT	VSS	VDD	AA
EMIOS4	EMIOS7	EMIOS11	EMIOS14	EMIOS18	EMIOS20	CAN_B_TX	CAN_B_RX	VDDE12	ENGCLK	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

Figure 7. 324-pin PBGA package ballmap (southeast, viewed from above)

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CAL_ADDR[15] CAL_ALE	Calibration address bus Calibration address latch enable	P A1	01 10	340	I/O O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[16] CAL_DATA[16]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[17] CAL_DATA[17]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[18] CAL_DATA[18]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[19] CAL_DATA[19]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[20] CAL_DATA[20]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[21] CAL_DATA[21]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[22] CAL_DATA[22]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[23] CAL_DATA[23]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[24] CAL_DATA[24]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[25] CAL_DATA[25]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[26] CAL_DATA[26]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[27] CAL_DATA[27]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[28] CAL_DATA[28]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[29] CAL_DATA[29]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—
CAL_ADDR[30] CAL_DATA[30]	Calibration address bus Calibration data bus	P A1	01 10	345	I/O I/O	VDDE12 / Fast		— / —	—	—	—

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CAN_C_TX DSPI_D_PCS[3] GPIO[87]	FlexCAN C transmit DSPI D peripheral chip select GPIO	P A1 G	01 10 00	87	O O I/O	VDDEH6 / Medium	— / Up	— / Up	101	K13	P19
CAN_C_RX DSPI_D_PCS[4] GPIO[88]	FlexCAN C receive DSPI D peripheral chip select GPIO	P A1 G	01 10 00	88	I O I/O	VDDEH6 / Slow	— / Up	— / Up	98	L14	R20
eSCI											
SCI_A_TX EMIOS13[16] GPIO[89]	eSCI A transmit eMIOS channel GPIO	P A1 G	01 10 00	89	O O I/O	VDDEH6 / Medium	— / Up	— / Up	100	J14	N20
SCI_A_RX EMIOS15[16] GPIO[90]	eSCI A receive eMIOS channel GPIO	P A1 G	01 10 00	90	I O I/O	VDDEH6 / Medium	— / Up	— / Up	99	K14	P20
SCI_B_TX DSPI_D_PCS[1] GPIO[91]	eSCI B transmit DSPI D peripheral chip select GPIO	P A1 G	01 10 00	91	O O I/O	VDDEH6 / Medium	— / Up	— / Up	87	L13	R21
SCI_B_RX DSPI_D_PCS[5] GPIO[92]	eSCI B receive DSPI D peripheral chip select GPIO	P A1 G	01 10 00	92	I O I/O	VDDEH6 / Medium	— / Up	— / Up	84	M13	T19
SCI_C_TX GPIO[244]	eSCI C transmit GPIO	P G	01 00	244	O I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	W18
SCI_C_RX GPIO[245]	eSCI C receive GPIO	P G	01 00	245	I I/O	VDDEH6 / Medium	— / Up	— / Up	—	—	Y19
DSPI											
DSPI_A_SCK[17] DSPI_C_PCS[1] GPIO[93]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	93	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L22
DSPI_A_SIN[17] DSPI_C_PCS[2] GPIO[94]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	94	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L21
DSPI_A_SOUT[17] DSPI_C_PCS[5] GPIO[95]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	95	— O I/O	VDDEH7 / Medium	— / Up	— / Up	—	—	L20

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
CLKOUT	System clock output	P	01	229	O	VDDE12 / Fast	—	CLKOUT	—	—	AA20
ENGCLK	Engineering clock output	P	01	214	O	VDDE12 / Fast	—	ENGCLK	—	T14	AB21
Power / Ground											
VDDREG	Voltage regulator supply	—		—	I	5 V	I / —	VDDREG	10	K16	M22
VRCCTL	Voltage regulator control output	—		—	O	—	O / —	VRCCTL	11	N14	V20
VRC33[18]	Internal regulator output	—		—	O	3.3 V	I/O / —	VRC33	13	A15, D1, N6, N12	A21, B1, P4, W7, Y22
	Input for external 3.3 V supply	—		—	I	3.3 V					
VDDA	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA	6	A4, B11	A6, C15
VSSA	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA	7	A5, A11	A7, A15, B15
VDDPLL	FMPLL supply voltage	—		—	I	1.2 V	I / —	VDDPLL	91	R16	W22
VSTBY	Power supply for standby RAM	—		—	I	0.9 V – 6 V	I / —	VSTBY	12	C1	A3
VDD	Core supply for input or decoupling	—		—	I	1.2 V	I / —	VDD	33, 45, 62, 103, 132, 149, 176	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15	A2, A20, B3, C4, C22, D5, V19, W5, W20, Y4, Y21, AA3, AA22, AB2
VDDE12	External supply input for calibration bus interfaces	—		—	I	3.0 V – 3.6 V	I / —	VDDE12	—	—	—
VDDE5	External supply input for ENGCLK and CLKOUT	—		—	I	3.0 V – 3.6 V	I / —	VDDE5	—	T13	W17, Y18, AA19, AB20
VDDE-EH	External supply for EBI interfaces	—		—	I	3.0 V – 5.0 V	I / —	VDDE-EH	—	—	R3, W2
VDDEH1A[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1A[19]	31	—	—
VDDEH1B[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1B[19]	41	—	—

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using *Equation 4*:

Equation 4 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

- Semiconductor Equipment and Materials International
  3081 Zanker Road
  San Jose, CA 95134
  USA
  Phone (+1) 408-943-6900
- MIL-SPEC and EIA/JESD (JEDEC) specifications available from Global Engineering Documents (phone (+1) 800-854-7179 or (+1) 303-397-7956)
- JEDEC specifications available on the Web at www.jedec.org
- C.E. Triplett and B. Joiner, “*An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “*Thermal Modeling of a PBGA for Air-Cooled Applications*”, Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “*Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

Table 16. PMC electrical characteristics (continued)

ID	Name		C	Parameter	Value			Unit
					Min	Typ	Max	
2c	—	CC	C	Trimming step V_{DD}	—	20	—	mV
2d	I_{VRCCTL}	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA
3	Lvi1p2	CC	C	Nominal LVI for rising core supply(3)	—	1.160	—	V
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset(4)	1.120	1.200	1.280	V
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset(4)	Lvi1p2 – 3%	Lvi1p2	Lvi1p2 + 3%	V
3c	—	CC	C	Trimming step LVI core supply	—	20	—	mV
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis	—	40	—	mV
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r – 35%	Por1.2V_r	Por1.2V_r + 35%	V
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f – 35%	Por1.2V_f	Por1.2V_f + 35%	V
5	V_{DD33}	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V
5a	—	CC	C	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset	V_{DD33} – 8.5%	V_{DD33}	V_{DD33} + 7%	V
5b	—	CC	C	Nominal 3.3 V supply internal regulator DC output voltage variation after power-on reset(5)	V_{DD33} – 7.5%	V_{DD33}	V_{DD33} + 7%	V
5c	—	CC	C	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω
5d	Idd3p3	CC	C	Voltage regulator 3.3 V maximum DC output current	80	—	—	mA
5e	Vdd33 ILim	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply(6)	—	3.090	—	V
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset(7)	Lvi3p3 – 6%	Lvi3p3	Lvi3p3 + 6%	V
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset(7)	Lvi3p3 – 3%	Lvi3p3	Lvi3p3 + 3%	V
6c	—	CC	C	Trimming step LVI 3.3 V	—	20	—	mV
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis	—	60	—	mV
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply(8)	—	2.07	—	V
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r – 35%	Por3.3V_r	Por3.3V_r + 35%	V

3.8 DC electrical specifications

Table 21. DC electrical specifications(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{DD}	SR	P	Core supply voltage	—	1.14	—	1.32	V
V_{DDE}	SR	P	I/O supply voltage	—	3.0	—	3.6	V
V_{DDEH}	SR	P	I/O supply voltage	—	3.0	—	5.25	V
V_{DDE-EH}	SR	P	I/O supply voltage	—	3.0	—	5.25	V
V_{RC33}	SR	P	3.3 V regulated voltage(2)	—	3.0	—	3.6	V
V_{DDA}	SR	P	Analog supply voltage	—	4.75(3)	—	5.25	V
V_{INDC}	SR	C	Analog input voltage	—	V_{SSA} – 0.3	—	V_{DDA} + 0.3	V
$V_{SS} – V_{SSA}$	SR	D	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	D	Analog reference low voltage	—	V_{SSA}	—	V_{SSA} + 0.1	V
$V_{RL} – V_{SSA}$	SR	D	V_{RL} differential voltage	—	–100	—	100	mV
V_{RH}	SR	D	Analog reference high voltage	—	V_{DDA} – 0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	P	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	P	Flash operating voltage(4)	—	1.14	—	1.32	V
V_{FLASH}(5)	SR	P	Flash read voltage	—	3.0	—	3.6	V
V_{STBY}	SR	C	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
				Regulated mode	2.0	—	5.5	
V_{DDREG}	SR	P	Voltage regulator supply voltage(6)	—	4.75	—	5.25	V
V_{DDPLL}	SR	P	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	D	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	SR	P	Slow/medium I/O input low voltage	Hysteresis enabled	V_{SS} – 0.3	—	0.35 * V_{DDEH}	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.40 * V_{DDEH}	
V_{IL_F}	SR	P	Fast I/O input low voltage	Hysteresis enabled	V_{SS} – 0.3	—	0.35 * V_{DDE}	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.40 * V_{DDE}	
V_{IL_LS}	SR	P	Multi-voltage I/O pad input low voltage in Low-swing-mode(7)(8)(9)(10)	Hysteresis enabled	V_{SS} – 0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.9	
V_{IL_HS}	SR	P	Multi-voltage pad I/O input low voltage in high-swing-mode	Hysteresis enabled	V_{SS} – 0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS} – 0.3	—	0.4 V_{DDEH}	

Table 26. PLLMRFM electrical specifications(1)

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{LCK}	CC	D	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	D	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS}	CC	D	Modulation depth	Center spread	±0.25	±4.0	% f_{sys}
f_{DS}		D		Down spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency(16)	—	—	100	kHz

1. All values given are initial design targets and subject to change.
2. Considering operation with PLL not bypassed
3. All internal registers retain data at 0 Hz.
4. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
5. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
6. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
7. This value is determined by the crystal manufacturer and board design.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
9. Proper PC board layout procedures must be followed to achieve specifications.
10. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. Proper PC board layout procedures must be followed to achieve specifications.
13. This parameter is guaranteed by design rather than 100% tested.
14. V_{IHEXT} cannot exceed V_{RC33} in external reference mode.
15. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
16. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.11 Temperature sensor electrical characteristics

Table 27. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	C	Temperature monitoring range		–40	—	150	°C

8. Can be used on the tester
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
11. Selectable high/low swing I/O pad with selectable slew in high swing mode only
12. Fast pads are 3.3 V pads.
13. Also has weak pull-up/pull-down.

Table 36. Pad AC specifications (V_{DDE} = 3.0 V)(1)

Pad type		C	Output delay (ns)(2)(3) Low-to-High / High-to-Low		Rise/Fall edge (ns)(3)(4)		Drive load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium(5)(6)(7)	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11(8)
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	—							10(9)
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow(7)(10)	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	—							10(9)
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV(7)(11) (High Swing Mode)	CC	D	—	3.7/3.1	—	10/10	30	11(8)
	CC	D	—	46/49	—	42/42	200	
	—							10(9)
	CC	D	—	32	—	15/15	50	01
	CC	D	—	72	—	46/46	200	
	CC	D	—	210	—	100/100	50	00
	CC	D	—	295	—	134/134	200	
MultiV (Low Swing Mode)	Not a valid operational mode							

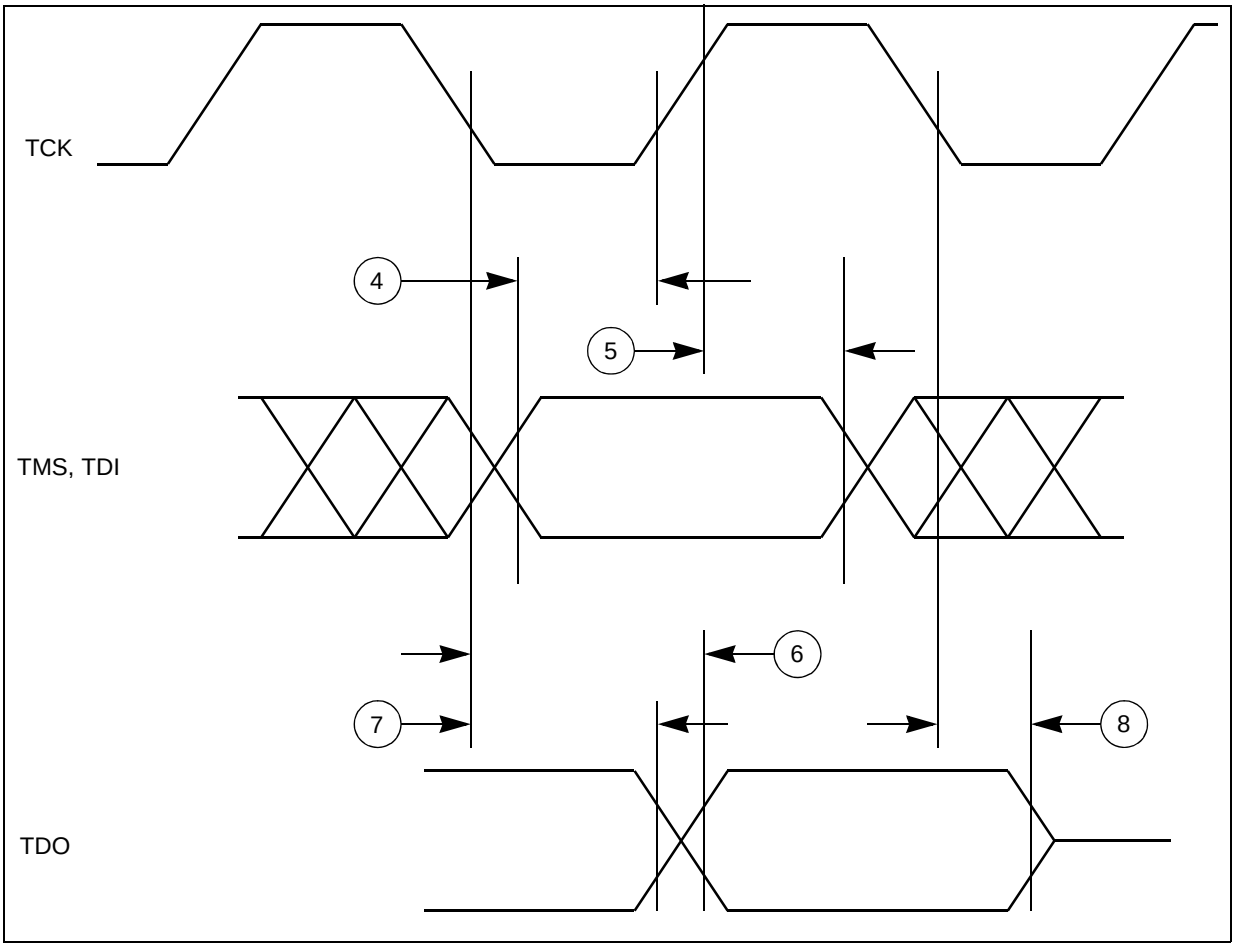


Figure 13. JTAG test access port timing

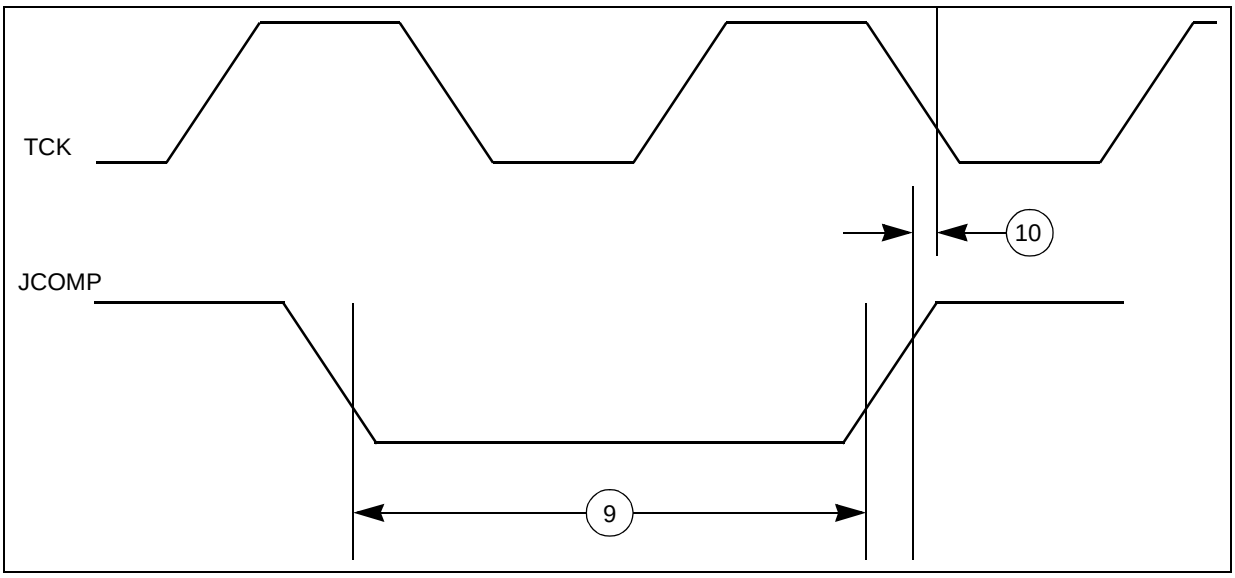


Figure 14. JTAG JCOMP timing

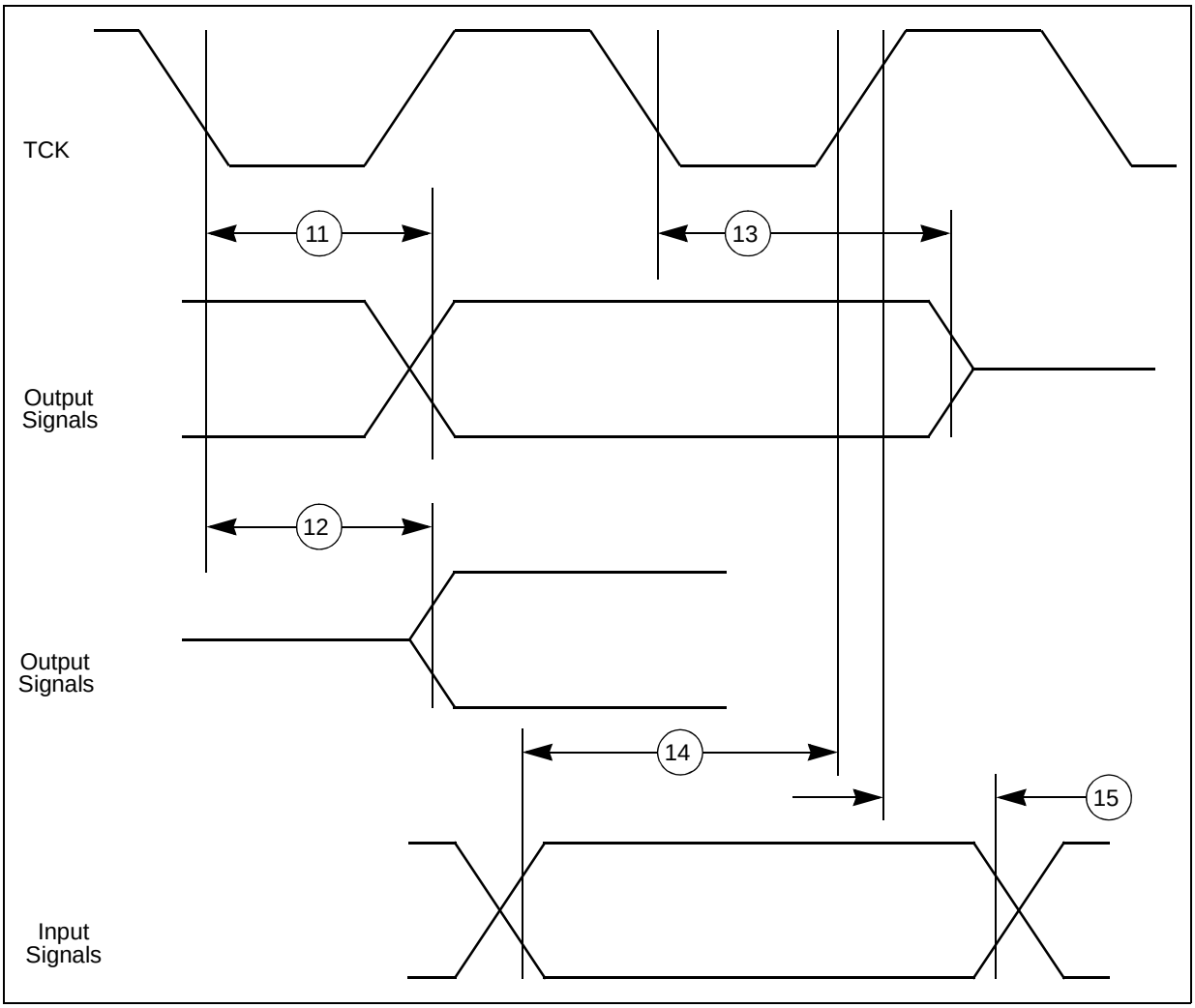


Figure 15. JTAG boundary scan timing

3.17.3 Nexus timing

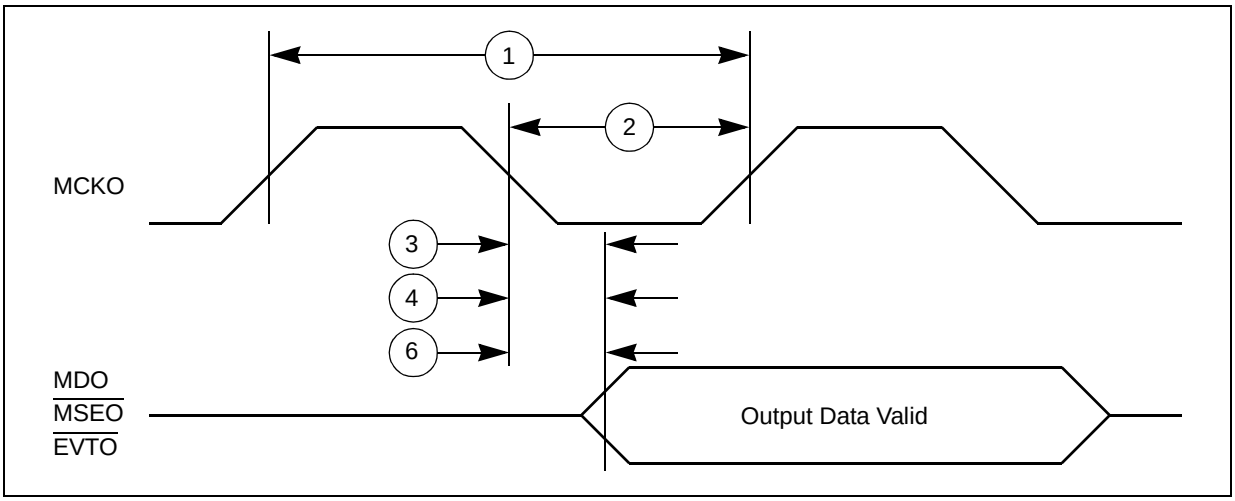
Table 39. Nexus debug port timing(1)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
1	t_{MCYC}	CC	D	MCKO Cycle Time	2(2)(3)	8	t_{CYC}
1a	t_{MCYC}	CC	D	Absolute Minimum MCKO Cycle Time	25(4)	—	ns
2	t_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid(5)	–0.1	0.35	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid(5)	–0.1	0.35	t_{MCYC}
6	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid(5)	–0.1	0.35	t_{MCYC}
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4.0	—	t_{TCYC}

Table 39. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
8	t_{EVTOPW}	CC	D	$\overline{EVTO}$ Pulse Width	1	—	t_{MCYC}
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6],[7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%
11	t_{NTDIS}	CC	D	TDI Data Setup Time	10	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	10	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK	—	19.5	ns
16	—	CC	D	TDO hold time wrt TCK falling edge (minimum TDO propagation delay)	5.25	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.75 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.
3. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.
4. This may require setting the MCO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.
5. MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
6. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
8. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.



4 Packages

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP176

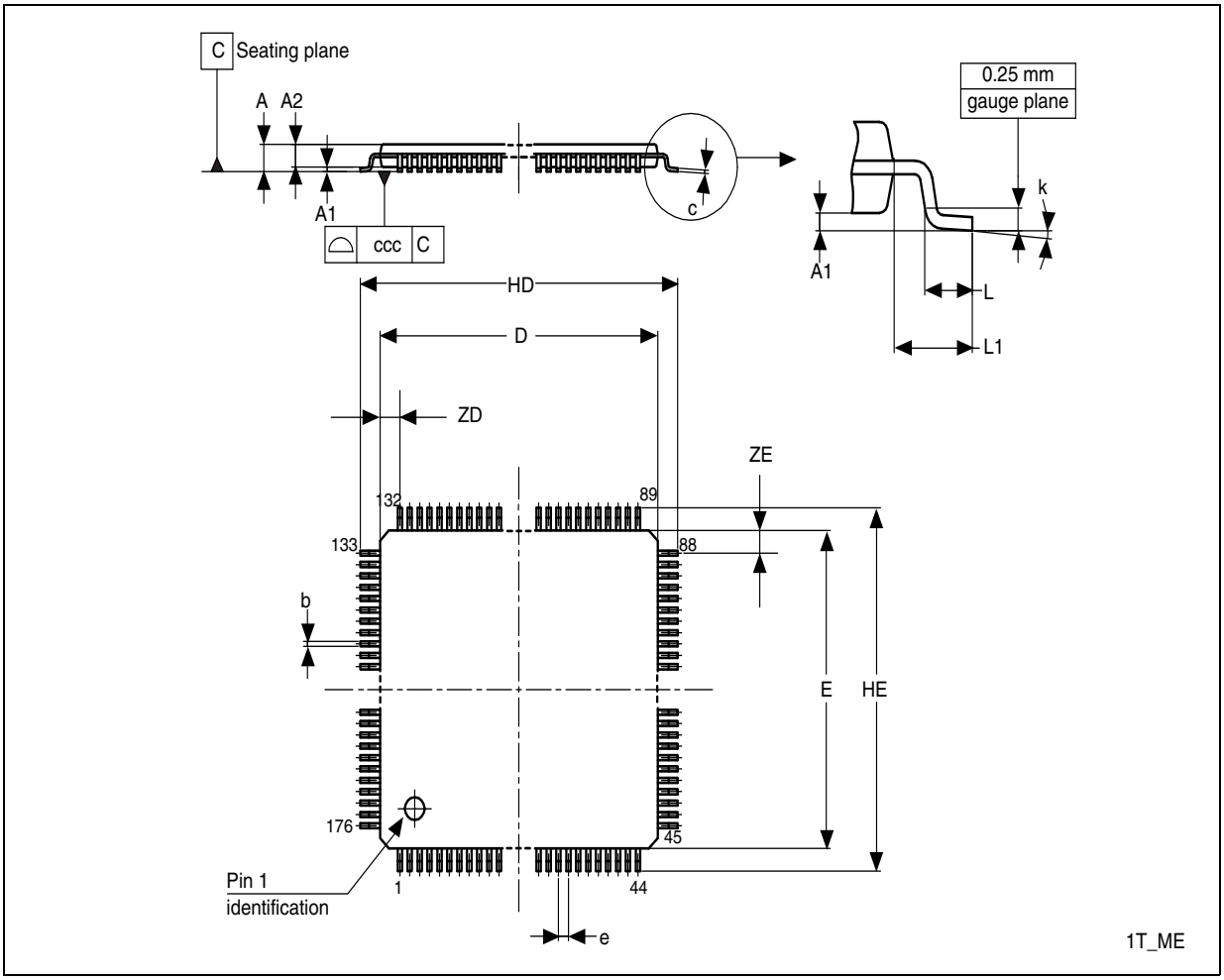


Figure 34. LQFP176 package mechanical drawing