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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z4 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, LINbus, SCI, SPI |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 150 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.14V ~ 1.32V |
| Data Converters | A/D 34x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-LQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70l7cocr |

# List of tables

  - 1 reaction module (6 channels with 3 outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
  - 6 command queues
  - Trigger and DMA support
  - 688 ns minimum conversion time
- On-chip CAN/SCI Bootstrap loader with Boot Assist Module (BAM)
- Nexus: Class 3+ for core; Class 1 for eTPU
- JTAG (5-pin)
- Development Trigger Semaphore (DTS)
  - EVTO pin for communication with external tool
- Clock generation
  - On-chip 4–40 MHz main oscillator
  - On-chip FMPLL (frequency-modulated phase-locked loop)
- Up to 112 general purpose I/O lines
  - Individually programmable as input, output or special function
  - Programmable threshold (hysteresis)
- Power reduction modes: slow, stop, and standby
- Flexible supply scheme
  - 5 V single supply with external ballast
  - Multiple external supply: 5 V, 3.3 V, and 1.2 V

## 1.5 Feature details

### 1.5.1 e200z4 core

SPC564A70 devices have a high performance e200z4 core processor:

- 32-bit Power Architecture technology programmer's model
- Variable Length Encoding (VLE) enhancements
- Dual issue, 32-bit Power Architecture technology compliant CPU
- 8 KB, 2/4-way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory Management Unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New 'Wait for Interrupt' instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and flash memory via independent Instruction and Data BIUs
- Load/store unit
  - 2-cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Power management
  - Low power design – extensive clock gating
  - Power saving modes: wait
  - Dynamic power management of execution units, cache and MMU
- Testability

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to 2 parameters by host

  - Prefill mode to precondition the filter before the sample window opens
  - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
  - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface (SSI) to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based queues
  - Supports 6 queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter

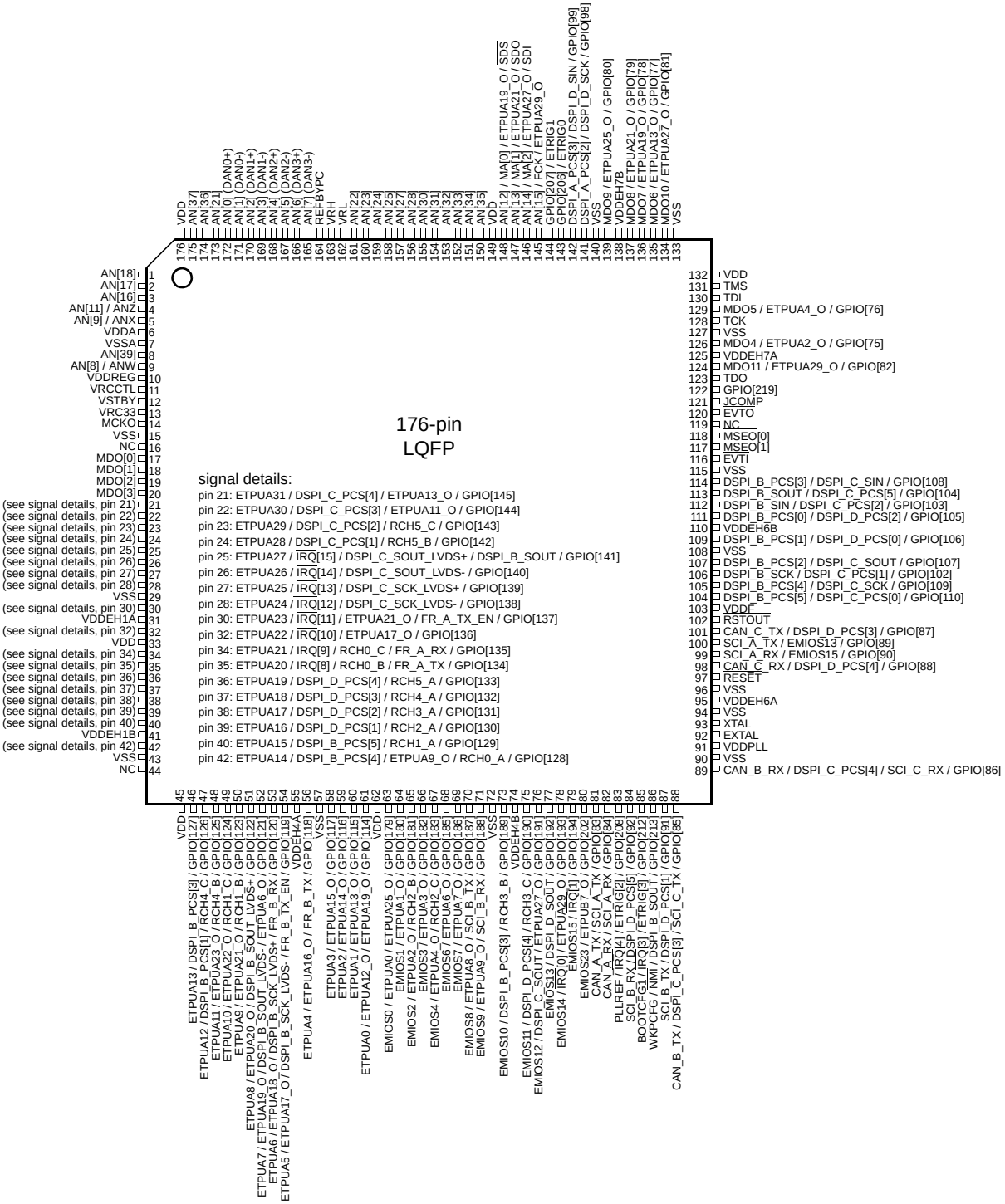
### 1.5.15 Deserial serial peripheral interface (DSPI)

The DSPI block provides a synchronous serial interface for communication between the SPC564A70 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the SPC564A70 MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHz for SOUT and SCK pins for DSPI_B and DSPI_C
- Support for downstream Micro Second Channel (MSC) with Timed Serial Bus (TSB) configuration on DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels, and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI module can generate and check parity in a serial frame

## 2.1 LQFP176 pinout




**Note:** Pin 96 (VSS) should be tied low.

**Figure 2. 176-pin LQFP pinout (top view)**

## 2.3 PBGA324 ballmap

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | VDD | VSTBY | AN37 | AN11 | VDDA | VSSA | AN1 | AN5 | VRH | VRL |
| B | VRC33 | VSS | VDD | AN36 | AN39 | AN19 | AN16 | AN0 | AN4 | REFBYPC | AN23 |
| C | ETPUA30 | ETPUA31 | VSS | VDD | AN38 | AN17 | AN20 | AN21 | AN3 | AN7 | AN22 |
| D | ETPUA28 | ETPUA29 | ETPUA26 | VSS | VDD | AN8 | AN9 | AN10 | AN18 | AN2 | AN6 |
| E | ETPUA24 | ETPUA27 | ETPUA25 | ETPUA21 | | | | | | | |
| F | ETPUA23 | ETPUA22 | ETPUA17 | ETPUA18 | | | | | | | |
| G | ETPUA20 | ETPUA19 | ETPUA14 | ETPUA13 | | | | | | | |
| H | ETPUA16 | ETPUA15 | ETPUA10 | VDDEH1AB | | | | | | | |
| J | ETPUA12 | ETPUA11 | ETPUA6 | ETPUA9 | | | | | VSS | VSS | VSS |
| K | ETPUA8 | ETPUA7 | ETPUA2 | ETPUA5 | | | | | VSS | VSS | VSS |
| L | ETPUA4 | ETPUA3 | ETPUA0 | ETPUA1 | | | | | VSS | VSS | VSS |

**Figure 4. 324-pin PBGA package ballmap (northwest, viewed from above)**

**Table 4. SPC564A70 signal properties (continued)**

| Name[1] | Function[2] | P / A / G[3] | PCR PA field[4] | PCR[5] | I/O type | Voltage[6] / Pad type[7] | Status[8] | | Package pin No. | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | During reset | After reset | 176 | 208[9] | 324 |
| CAL_DATA[0] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[1] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[2] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[3] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[4] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[5] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[6] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[7] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[8] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[9] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[10] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[11] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[12] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[13] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[14] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |
| CAL_DATA[15] | Calibration data bus | P | 01 | 341 | I/O | VDDE12 / Fast | — / Up | — / Up | — | — | — |

**Table 4. SPC564A70 signal properties (continued)**

| Name[1] | Function[2] | P / A / G[3] | PCR PA field[4] | PCR[5] | I/O type | Voltage[6] / Pad type[7] | Status[8] | | Package pin No. | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | During reset | After reset | 176 | 208[9] | 324 |
| DSPI_B_PCS[2]<br>DSPI_C_SOUT<br>GPIO[107] | DSPI B peripheral chip select<br>DSPI C data output<br>GPIO | P<br>A1<br>G | 01<br>10<br>00 | 107 | O<br>O<br>I/O | VDDEH6 / Medium | — / Up | — / Up | 107 | H15 | K22 |
| DSPI_B_PCS[3]<br>DSPI_C_SIN<br>GPIO[108] | DSPI B peripheral chip select<br>DSPI C data input<br>GPIO | P<br>A1<br>G | 01<br>10<br>00 | 108 | O<br>I<br>I/O | VDDEH6 / Medium | — / Up | — / Up | 114 | G14 | J20 |
| DSPI_B_PCS[4]<br>DSPI_C_SCK<br>GPIO[109] | DSPI B peripheral chip select<br>SPI clock pin for DSPI module<br>GPIO | P<br>A1<br>G | 01<br>10<br>00 | 109 | O<br>I/O<br>I/O | VDDEH6 / Medium | — / Up | — / Up | 105 | H14 | K20 |
| DSPI_B_PCS[5]<br>DSPI_C_PCS[0]<br>GPIO[110] | DSPI B peripheral chip select<br>DSPI C peripheral chip select<br>GPIO | P<br>A1<br>G | 01<br>10<br>00 | 110 | O<br>I/O<br>I/O | VDDEH6 / Medium | — / Up | — / Up | 104 | J13 | L19 |
| **eQADC** | | | | | | | | | | | |
| AN0<br>DAN0+ | Single Ended Analog Input<br>Positive Terminal Differential Input | P | — | — | I | VDDA / Analog Pull-up/down | I / — | AN[0] / — | 172 | B5 | B8 |
| AN1<br>DAN0– | Single Ended Analog Input<br>Negative Terminal Differential Input | P | — | — | I | VDDA / Analog Pull-up/down | I / — | AN[1] / — | 171 | A6 | A8 |
| AN2<br>DAN1+ | Single Ended Analog Input<br>Positive Terminal Differential Input | P | — | — | I | VDDA / Analog Pull-up/down | I / — | AN[2] / — | 170 | D6 | D10 |
| AN3<br>DAN1– | Single Ended Analog Input<br>Negative Terminal Differential Input | P | — | — | I | VDDA / Analog Pull-up/down | I / — | AN[3] / — | 169 | C7 | C9 |
| AN4<br>DAN2+ | Single Ended Analog Input<br>Positive Terminal Differential Input | P | — | — | I | VDDA / Analog Pull-up/down | I / — | AN[4] / — | 168 | B6 | B9 |
| AN5<br>DAN2– | Single Ended Analog Input<br>Negative Terminal Differential Input | P | — | — | I | VDDA / Analog Pull-up/down | I / — | AN[5] / — | 167 | A7 | A9 |
| AN6<br>DAN3+ | Single Ended Analog Input<br>Positive Terminal Differential Input | P | — | — | I | VDDA / Analog Pull-up/down | I / — | AN[6] / — | 166 | D7 | D11 |

## 3.2 Maximum ratings

**Table 9. Absolute maximum ratings(1)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{DD}$ | SR | 1.2 V core supply voltage(2) | | –0.3 | 1.32 | V |
| $V_{FLASH}$ | SR | Flash core voltage(3)(4) | | –0.3 | 3.6 | V |
| $V_{STBY}$ | SR | SRAM standby voltage(5) | | –0.3 | 6.0 | V |
| $V_{DDPLL}$ | SR | Clock synthesizer voltage(3) | | –0.3 | 1.32 | V |
| $V_{RC33}$ | SR | Voltage regulator control input voltage(4) | | –0.3 | 3.6 | V |
| $V_{DDA}$ | SR | Analog supply voltage(5) | Reference to $V_{SSA}$ | –0.3 | 5.5 | V |
| $V_{DDE}$ | SR | I/O supply voltage(4)(6) | | –0.3 | 3.6 | V |
| $V_{DDEH}$ | SR | I/O supply voltage(5)(7) | | –0.3 | 5.5 | V |
| $V_{IN}$ | SR | DC input voltage(8) | $V_{DDEH}$ powered I/O pads | –1.0[10] | $V_{DDEH}$ + 0.3 V(9) | V |
| | | | $V_{DDE}$ powered I/O pads | –1.0[14] | $V_{DDE}$ + 0.3 V(10) | |
| | | | $V_{DDA}$ powered I/O pads | –1.0 | 5.5 | |
| $V_{DDREG}$ | SR | Voltage regulator supply voltage | | –0.3 | 5.5 | V |
| $V_{RH}$ | SR | Analog reference high voltage | Reference to VRL | –0.3 | 5.5 | V |
| $V_{SS} – V_{SSA}$ | SR | $V_{SS}$ differential voltage | | –0.1 | 0.1 | V |
| $V_{RH} – V_{RL}$ | SR | $V_{REF}$ differential voltage | | –0.3 | 5.5 | V |
| $V_{RL} – V_{SSA}$ | SR | $V_{RL}$ to $V_{SSA}$ differential voltage | | –0.3 | 0.3 | V |
| $V_{SSPLL} – V_{SS}$ | SR | $V_{SSPLL}$ to $V_{SS}$ differential voltage | | –0.1 | 0.1 | V |
| $I_{MAXD}$ | SR | Maximum DC digital input current(11) | Per pin, applies to all digital pins | –3 | 3 | mA |
| $I_{MAXA}$ | SR | Maximum DC analog input current(12) | Per pin, applies to all analog pins | — | 5(13) | mA |
| $T_J$ | SR | Maximum operating temperature range — die junction temperature | | –40.0 | 150.0 | °C |
| $T_{STG}$ | SR | Storage temperature range | | –55 | 150 | °C |
| $T_{SDR}$ | SR | Maximum solder temperature(14) | | — | 260 | °C |
| MSL | SR | Moisture sensitivity level(15) | | — | 3 | — |

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Allowed 2 V for 10 hours cumulative time, remaining time at 1.2 V + 10%
3. The $V_{FLASH}$ supply is connected to $V_{RC33}$ in the package substrate. This specification applies to calibration package devices only.
4. Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V + 10%
5. Allowed 5.9 V for 10 hours cumulative time, remaining time at 5 V + 10%

6. All functional non-supply I/O pins are clamped to $V_{SS}$ and $V_{DDE}$, or $V_{DDEH}$.
7. Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.
8. AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).
9. Internal structures hold the input voltage less than the maximum voltage on all pads powered by $V_{DDEH}$ supplies, if the maximum injection current specification is met (2 mA for all pins) and $V_{DDEH}$ is within the operating voltage specifications.
10. Internal structures hold the input voltage less than the maximum voltage on all pads powered by $V_{DDE}$ supplies, if the maximum injection current specification is met (2 mA for all pins) and $V_{DDE}$ is within the operating voltage specifications.
11. Total injection current for all pins (including both digital and analog) must not exceed 25 mA.
12. Total injection current for all analog input pins must not exceed 15 mA.
13. Lifetime operation at these specification limits is not guaranteed.
14. Solder profile per IPC/JEDEC J-STD-020D
15. Moisture sensitivity per JEDEC test method A112

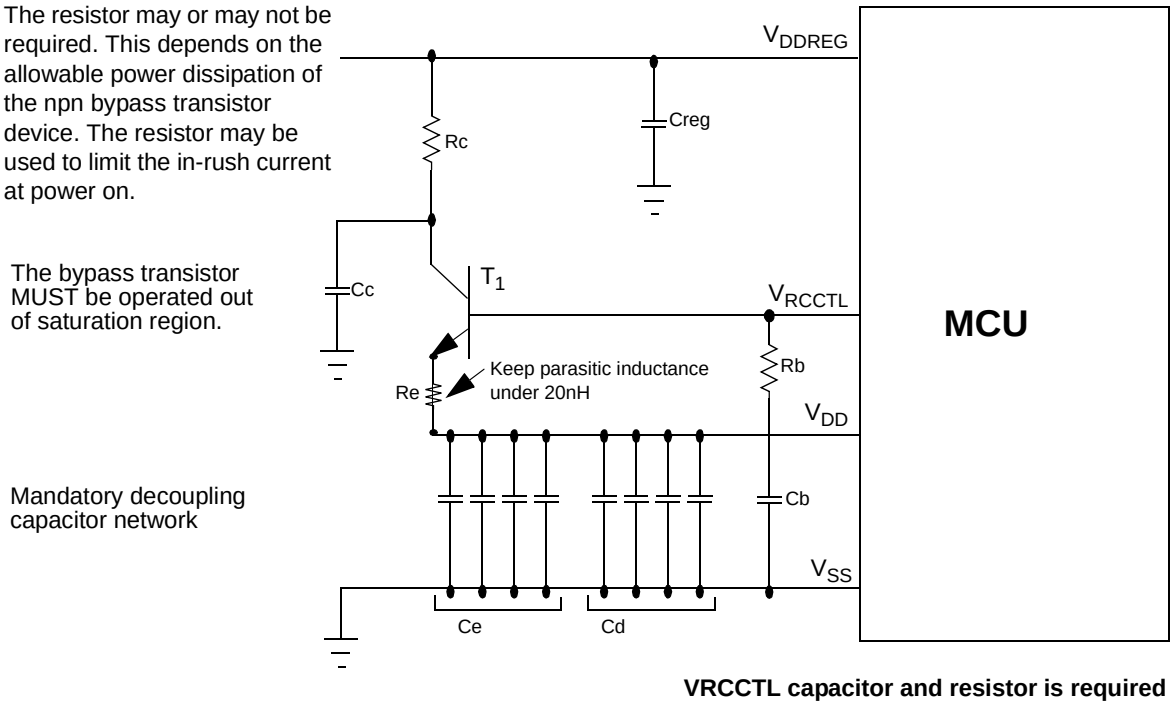



**Figure 8. Core voltage regulator controller external components preferred configuration**

**Table 17. SPC564A70 External network specification**

| External Network Parameter | Min | Typ | Max | Comment |
|---|---|---|---|---|
| T1 | — | — | — | NJD2873 or BCP68 only |
| Cb | 1.1 µF | 2.2µF | 2.97µF | X7R,-50%/+35% |
| Ce | 3*2.35µF+5µF | 3*4.7µF+10µF | 3*6.35µF+13.5µF | X7R, -50%/+35% |
| Equivalent ESR of Ce capacitors | 5mΩ | — | 50mΩ | — |
| Cd | 4*50nF | 4*100nF | 4*135nF | X7R, -50%/+35% |
| Rb | 9Ω | 10Ω | 11Ω | +/-10% |
| Re | 0.252Ω | 0.280Ω | 0.308Ω | +/-10% |
| Creg | — | 10µF | — | It depends on external Vreg. |
| Cc | 5µF | 10µF | 13.5µF | X7R, -50%/+35% |
| Rc | 1.1Ω | — | 5.6Ω | May or may not be required. It depends on the allowable power dissipation of T1. |

## 3.14 Platform flash controller electrical characteristics

**Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1)**

| Max. Flash Operating Frequency (MHz)(2) | APC(3) | RWSC(3) | WWSC |
|---|---|---|---|
| 20 MHz | 0b000 | 0b000 | 0b01 |
| 61 MHz | 0b001 | 0b001 | 0b01 |
| 90 MHz | 0b010 | 0b010 | 0b01 |
| 123 MHz | 0b011 | 0b011 | 0b01 |
| 153 MHz | 0b100 | 0b100 | 0b01 |

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. Max frequencies including 2% PLL FM.
3. APC must be equal to RWSC.

## 3.15 Flash memory electrical characteristics

**Table 33. Flash program and erase specifications(1)**

| # | Symbol | | C | Parameter | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Initial max(2) | Max(3) | |
| 1 | $T_{dwprogram}$ | CC | C | Double Word (64 bits) Program Time | — | 30 | — | 500 | µs |
| 2 | $T_{pprogram}$ | CC | C | Page Program Time(4) | — | 40 | 160 | 500 | µs |
| 3 | $T_{16kpperase}$ | CC | C | 16 KB Block Pre-program and Erase Time | — | — | 1000 | 5000 | ms |
| 5 | $T_{64kpperase}$ | CC | C | 64 KB Block Pre-program and Erase Time | — | — | 1800 | 5000 | ms |
| 6 | $T_{128kpperase}$ | CC | C | 128 KB Block Pre-program and Erase Time | — | — | 2600 | 7500 | ms |
| 7 | $T_{256kpperase}$ | CC | C | 256 KB Block Pre-program and Erase Time | — | — | 5200 | 15000 | ms |
| 8 | $T_{psrt}$ | SR | — | Program suspend request rate(5) | 100 | — | — | — | µs |
| 9 | $T_{esrt}$ | SR | — | Erase suspend request rate (6) | 10 | | | | ms |

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

**Table 36. Pad AC specifications ($V_{DDE}$ = 3.0 V)(1) (continued)**

| Pad type | | C | Output delay (ns)(2)(3) Low-to-High / High-to-Low | | Rise/Fall edge (ns)(3)(4) | | Drive load (pF) | SRC/DSC |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | MSB,LSB |
| Fast | CC | D | — | 2.5/2.5 | — | 1.2/1.2 | 10 | 00 |
| | CC | D | — | 2.5/2.5 | — | 1.2/1.2 | 20 | 01 |
| | CC | D | — | 2.5/2.5 | — | 1.2/1.2 | 30 | 10 |
| | CC | D | — | 2.5/2.5 | — | 1.2/1.2 | 50 | 11(8) |
| Standalone input buffer(12) | CC | D | 0.5/0.5 | 3/3 | 0.4/0.4 | ±1.5/1.5 | 0.5 | — |

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at $V_{DD}$ = 1.14 V to 1.32 V, $V_{DDE}$ = 3 V to 3.6 V, $V_{DDEH}$ = 3 V to 3.6 V, $T_A = T_L$ to $T_H$.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad $V_{OL}$ and $V_{OH}$ values are the same as those of the slew controlled output pads.
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
7. Output delay is shown in *Figure 9* and *Figure 10*. Add a maximum of one system clock to the output delay for delay with respect to system clock.
8. Can be used on the tester.
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pull-up/pull-down.
11. Selectable high/low swing I/O pad with selectable slew in high swing mode only.
12. Also has weak pull-up/pull-down.

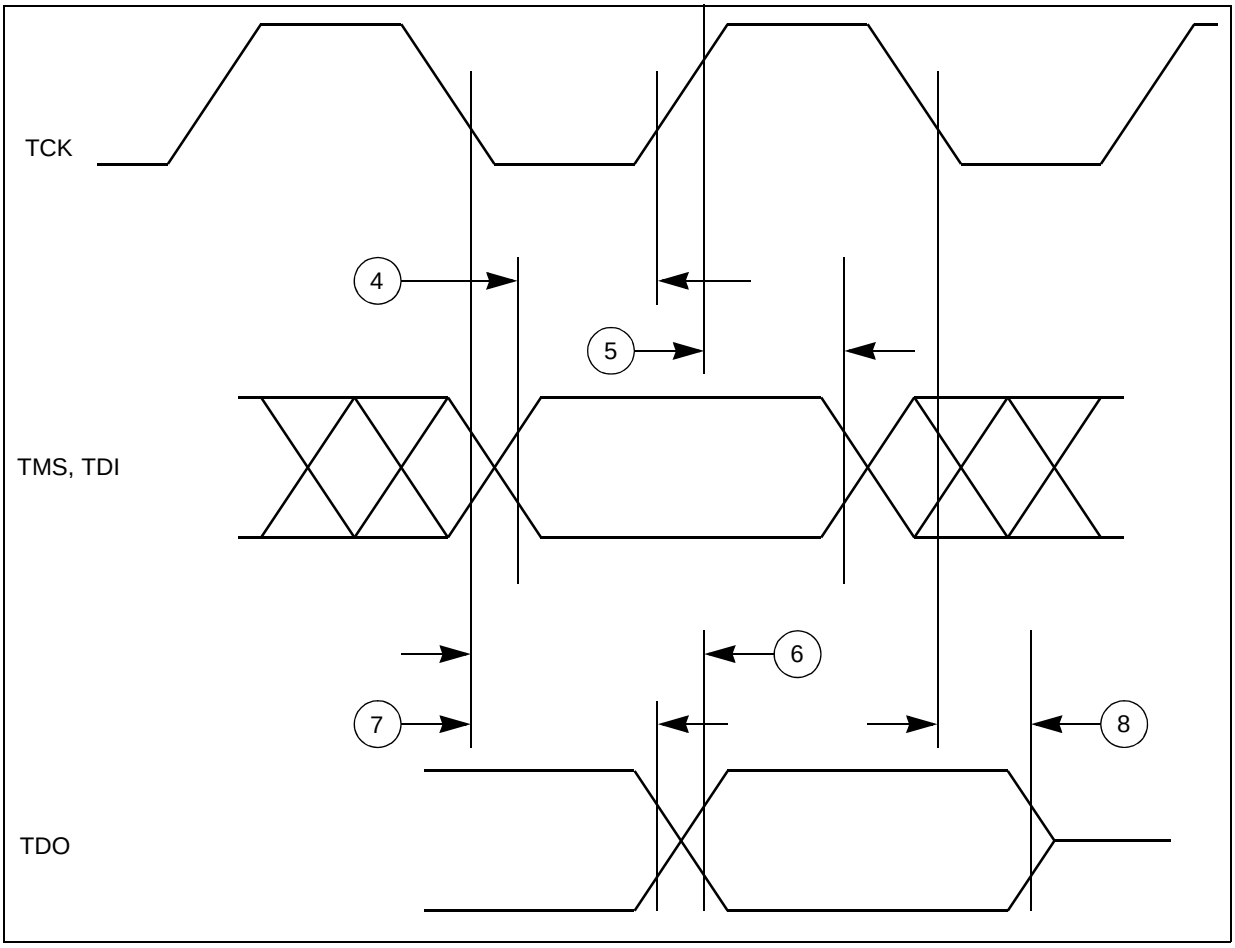



**Figure 13. JTAG test access port timing**

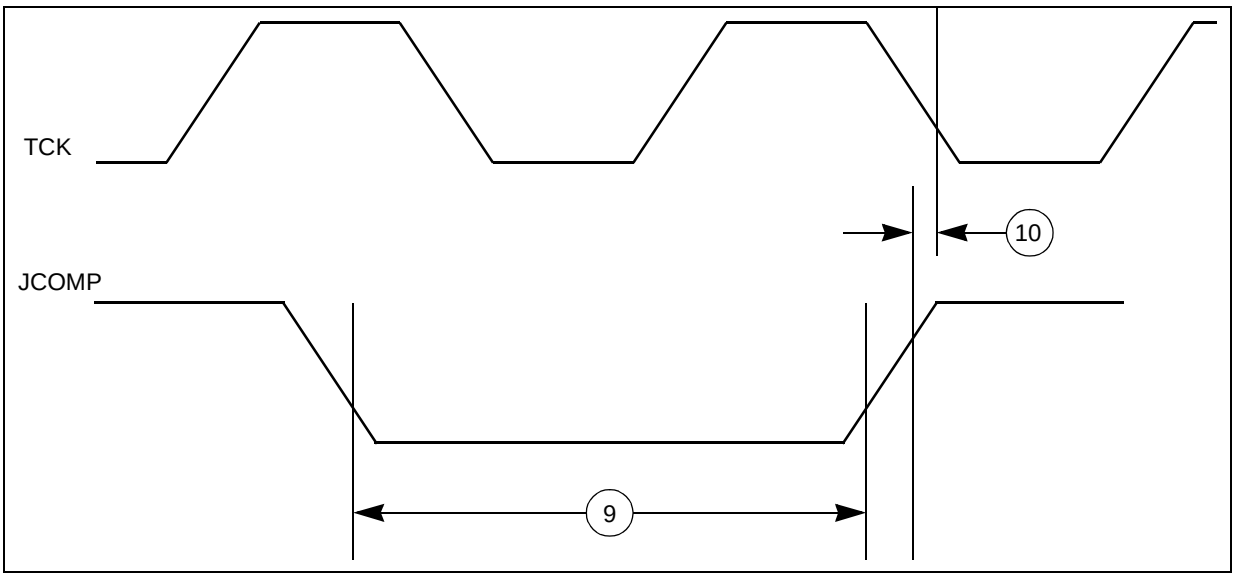
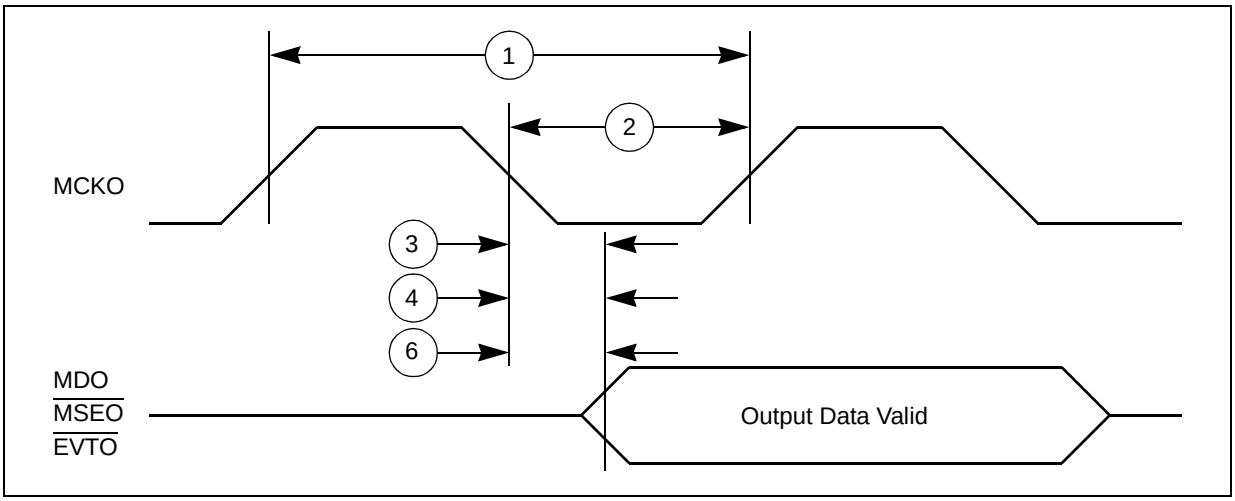



**Figure 14. JTAG JCOMP timing**

**Table 39. Nexus debug port timing[1] (continued)**

| # | Symbol | | C | Characteristic | Value | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| 8 | $t_{EVTOPW}$ | CC | D | $\overline{EVTO}$ Pulse Width | 1 | — | $t_{MCYC}$ |
| 9 | $t_{TCYC}$ | CC | D | TCK Cycle Time | 4[6],[7] | — | $t_{CYC}$ |
| 9a | $t_{TCYC}$ | CC | D | Absolute Minimum TCK Cycle Time | 100[8] | — | ns |
| 10 | $t_{TDC}$ | CC | D | TCK Duty Cycle | 40 | 60 | % |
| 11 | $t_{NTDIS}$ | CC | D | TDI Data Setup Time | 10 | — | ns |
| 12 | $t_{NTDIH}$ | CC | D | TDI Data Hold Time | 25 | — | ns |
| 13 | $t_{NTMSS}$ | CC | D | TMS Data Setup Time | 10 | — | ns |
| 14 | $t_{NTMSH}$ | CC | D | TMS Data Hold Time | 25 | — | ns |
| 15 | — | CC | D | TDO propagation delay from falling edge of TCK | — | 19.5 | ns |
| 16 | — | CC | D | TDO hold time wrt TCK falling edge (minimum TDO propagation delay) | 5.25 | — | ns |

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at $V_{DD}$ = 1.14 V to 1.32 V, $V_{DDEH}$ = 4.75 V to 5.25 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to $T_H$, and $C_L$ = 30 pF with DSC = 0b10.
2. Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.
3. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.
4. This may require setting the MCO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.
5. MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
6. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
8. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.



### 3.17.7 eMIOS timing

**Table 45. eMIOS timing(1)**

| # | Symbol | | C | Characteristic | Value | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| 1 | $t_{MIPW}$ | CC | D | eMIOS Input Pulse Width | 4 | — | $t_{CYC}$ |
| 2 | $t_{MOPW}$ | CC | D | eMIOS Output Pulse Width | 1 | — | $t_{CYC}$ |

1. eMIOS timing specified at $V_{DD}$ = 1.14 V to 1.32 V, $V_{DDEH}$ = 4.75 V to 5.25 V, $T_A = T_L$ to $T_H$, and $C_L$ = 50 pF with SRC = 0b00.

### 3.17.8 DSPI timing

DSPI channel frequency support for the SPC564A70 MCU is shown in *Table 46*. Timing specifications are in *Table 47*.

**Table 46. DSPI channel frequency support**

| System clock (MHz) | DSPI Use Mode | Maximum usable frequency (MHz) | Notes |
|---|---|---|---|
| 150 | LVDS | 37.5 | Use sysclock /4 divide ratio |
| | Non-LVDS | 18.75 | Use sysclock /8 divide ratio |
| 120 | LVDS | 40 | Use sysclock /3 divide ratio. Gives 33/66 duty cycle. Use DSPI configuration DBR = 0b1 (double baud rate), BR = 0b0000 (scaler value 2) and PBR = 0b01 (prescaler value 3). |
| | Non-LVDS | 20 | Use sysclock /6 divide ratio |
| 80 | LVDS | 40 | Use sysclock /2 divide ratio |
| | Non-LVDS | 20 | Use sysclock /4 divide ratio |

**Table 47. DSPI timing(1)(2)**

| # | Symbol | | C | Characteristic | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{SCK}$ | CC | D | SCK Cycle Time(3)(4)(5) | | 24.4 ns | 2.9 ms | — |
| 2 | $t_{CSC}$ | CC | D | PCS to SCK Delay(6) | | 22(7) | — | ns |
| 3 | $t_{ASC}$ | CC | D | After SCK Delay(8) | | 21(9) | — | ns |
| 4 | $t_{SDC}$ | CC | D | SCK Duty Cycle | | $(½t_{SC}) - 2$ | $(½t_{SC}) + 2$ | ns |
| 5 | $t_A$ | CC | D | Slave Access Time ($\overline{SS}$ active to SOUT driven) | | — | 25 | ns |
| 6 | $t_{DIS}$ | CC | D | Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid) | | — | 25 | ns |
| 7 | $t_{PCSC}$ | CC | D | PCSx to $\overline{PCSS}$ time | | 4(10) | — | ns |
| 8 | $t_{PASC}$ | CC | D | $\overline{PCSS}$ to PCSx time | | 5(11) | — | ns |

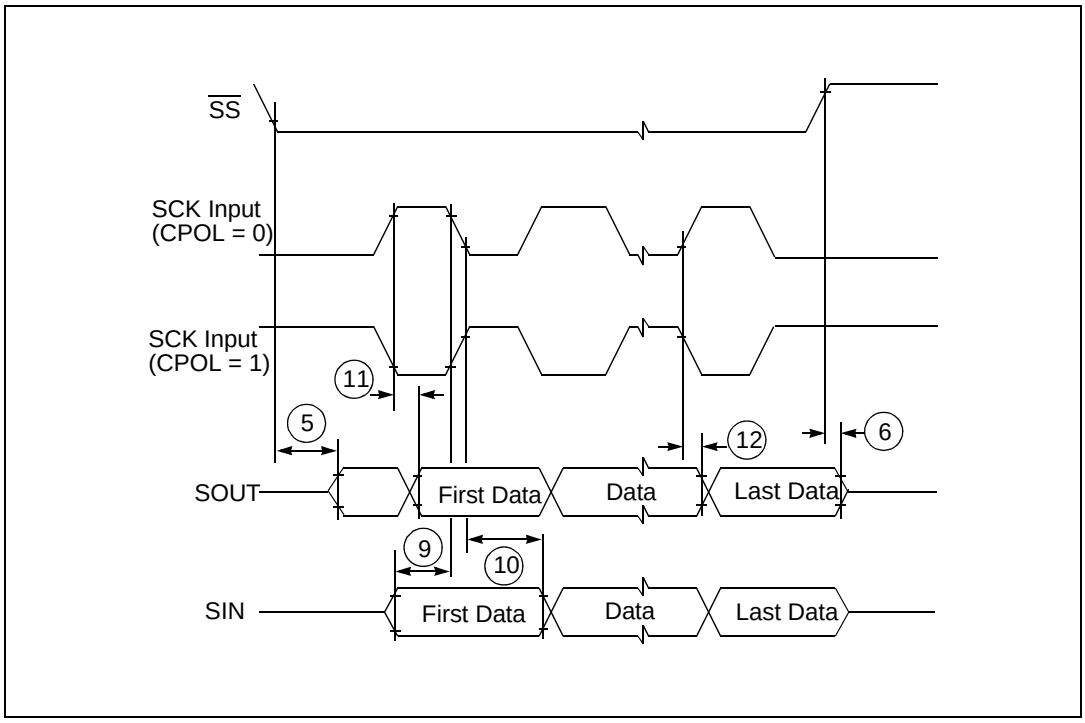



**Figure 27. DSPI classic SPI timing (slave, CPHA = 1)**

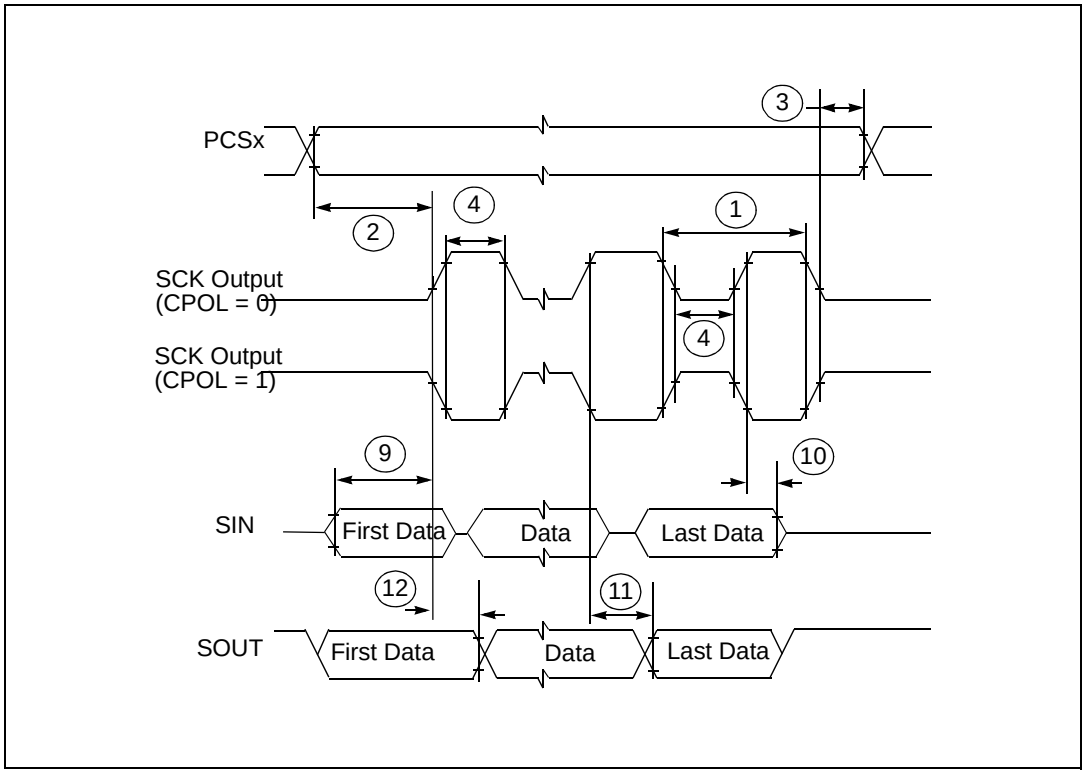



**Figure 28. DSPI modified transfer format timing (master, CPHA = 0)**

**Table 54. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 11-Apr-2012 | 2 (continued) | Added *Table 40 (Nexus debug port operating frequency)*<br>*Table 40 (Nexus debug port operating frequency)*, added a footnote near the value of $t_{AAI}$<br>*Table 45 (eMIOS timing)*:<br>changed minumum value of $t_{MOPW}$ to 1<br>removed the footnote of $t_{MOPW}$<br><br>Merged "DSPI timing ($V_{DDEH}$ = 3.0 to 3.6 V)" and "DSPI timing ($V_{DDEH}$ = 4.5 to 5.5V)" tables into *Table 47 (DSPI timing)* and changed all parameter classification to D<br>*Table 48 (eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V))* changed all parameter classification to D<br>*Table 52 (LBGA208 mechanical data)* deleted Notes column and moved all footnote next to relative references<br>*Table 53 (PBGA324 package mechanical data)* deleted Notes column and moved all footnote next to relative references<br>[[ST_Specific]]<br>*Table 12 (Thermal characteristics for 324-pin PBGA)*, updated values<br>In *Section 3.6, Power management control (PMC) and power on reset (POR) electrical specifications*, deleted the "Voltage regulator controller ($V_{RC}$) electrical specifications"<br>Updated *Section 4.2.1, LQFP176* |
| 06-Jun-2012 | 3 | Minor editorial changes and improvements throughout.<br>In *Section 2.4, Signal summary*, *Table 4 (SPC564A70 signal properties)*, updated the following properties for the Nexus pins:<br>– Added a footnote to the "Nexus" title for this pin group.<br>– Added a footnote to the "Name" entry for $\overline{\text{EVTO}}$.<br>– Updated the "Status During reset" entry for $\overline{\text{EVTO}}$.<br>In *Section 3.2, Maximum ratings*, *Table 9 (Absolute maximum ratings)*, removed the "TBD - To be defined" footnote.<br>In *Section 3.8, DC electrical specifications*, *Table 21 (DC electrical specifications)*, removed the "TBD - To be defined" footnote.<br>In *Section 3.9, I/O pad current specifications*, *Table 22 (I/O pad average IDDE specifications)*:<br>– Updated values and replaced TBDs with numerical data.<br>– Removed the "TBD - To be defined" footnote.<br>In *Section 3.9.1, I/O pad VRC33 current specifications*, *Table 23 (I/O pad VRC33 average IDDE specifications)*:<br>– Updated values and replaced TBDs with numerical data.<br>– Removed the "TBD - To be defined" footnote.<br>In *Section 3.14, Platform flash controller electrical characteristics*, *Table 32 (APC, RWSC, WWSC settings vs. frequency of operation)*, removed the "TBD - To be defined" footnote.<br>In *Table 54 (Document revision history)*, removed extraneous text from the Revision 2 entry. |
| 18-Sep-2013 | 4 | Updated Disclaimer. |