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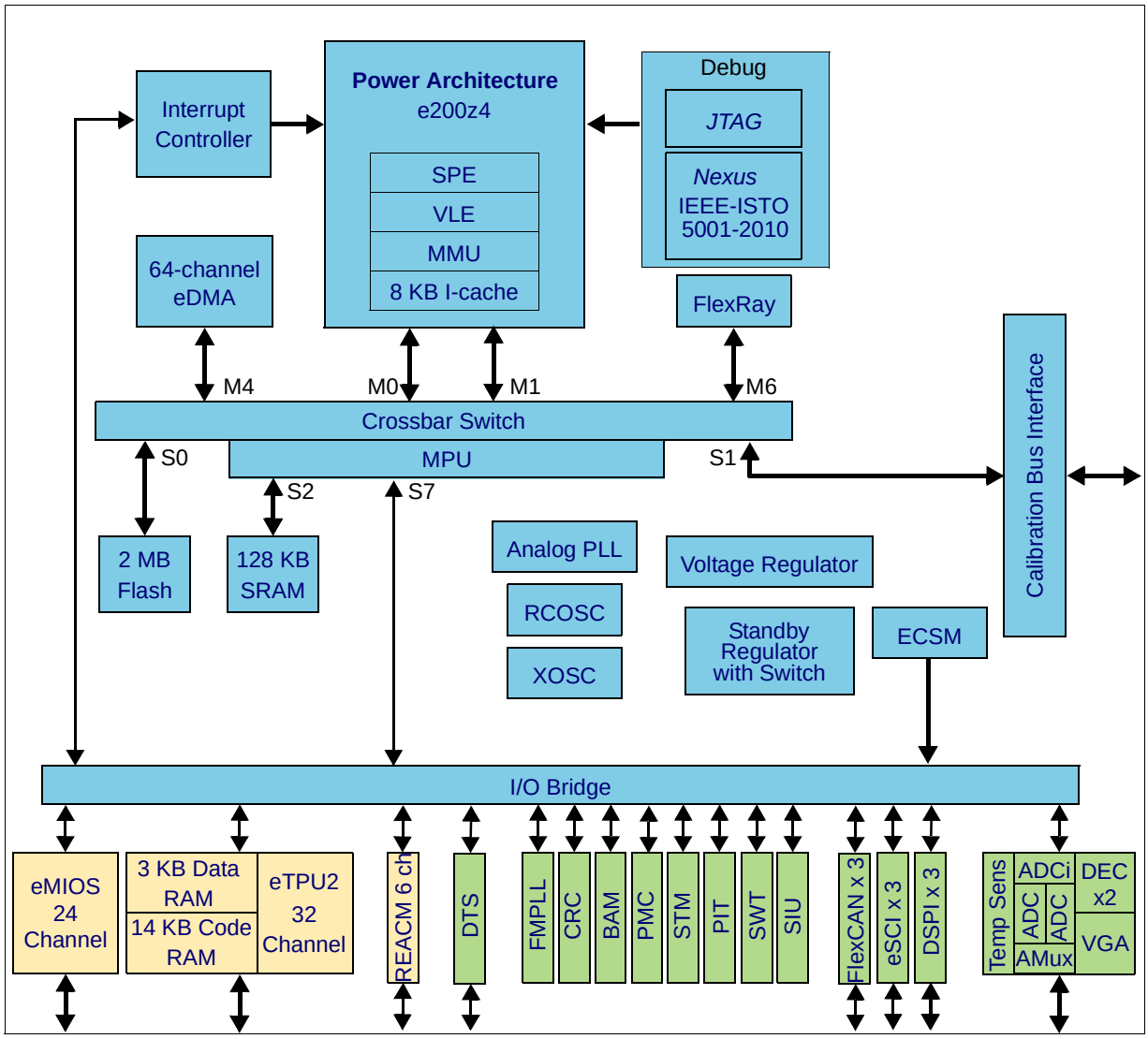
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	150
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a70l7cocy

List of tables

List of figures



LEGEND

ADC	– Analog to Digital Converter	**JTAG**	– IEEE 1149.1 Test Controller
ADCi	– ADC interface	**MMU**	– Memory Management Unit
AMux	– Analog Multiplexer	**MPU**	– Memory Protection Unit
BAM	– Boot Assist Module	**PMC**	– Power Management Controller
CRC	– Cyclic Redundancy Check unit	**PIT**	– Periodic Interrupt Timer
DEC	– Decimation Filter	**RCOSC**	– Low-speed RC Oscillator
DTS	– Development Trigger Semaphore	**REACM**	– Reaction Module
DSPI	– Deserial/Serial Peripheral Interface	**SIU**	– System Integration Unit
ECSM	– Error Correction Status Module	**SPE**	– Signal Processing Extension
eDMA	– Enhanced Direct Memory Access	**SRAM**	– Static RAM
eMIOS	– Enhanced Modular Input Output System	**STM**	– System Timer Module
eSCI	– Enhanced Serial Communications Interface	**SWT**	– Software Watchdog Timer
eTPU2	– Second gen. Enhanced Time Processing Unit	**VGA**	– Variable Gain Amplifier
FlexCAN	– Controller Area Network	**VLE**	– Variable Length (instruction) Encoding
FMPLL	– Frequency-Modulated Phase-Locked Loop	**XOSC**	– XTAL Oscillator

Figure 1. SPC564A70 series block diagram

out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
    12-bit conversion time – 938 ns (1 M sample/s)
    10-bit conversion time – 813 ns (1.2 M sample/s)
    8-bit conversion time – 688 ns (1.4M sample/s)
  - Up to 10-bit accuracy at 500K sample/s and 8-bit accuracy at 1M sample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Allows time stamp information relative to eTPU clock sources, such as an angle clock
  - Parallel interface to eQADC command FIFOs (CFIFOs) and result FIFOs (RFIFOs)
  - Supports both right-justified unsigned and signed formats for conversion results
- 40 single-ended input channels, expandable to 56 channels with external multiplexers (supports 4 external 8-to-1 muxes)
- 8 channels can be used as 4 pairs of differential analog input channels
- Differential channels include variable gain amplifier for improved dynamic range (×1, ×2, ×4)
- Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ, 100 kΩ, 5 kΩ)
- Additional internal channels for monitoring voltages (such as core voltage, I/O voltage, LVI voltages, etc.) inside the device
- An internal bandgap reference to allow absolute voltage measurements
- Silicon die temperature sensor
  - Provides temperature of silicon as an analog value
  - Read using an internal ADC analog channel
  - May be read with either ADC
- 2 decimation filters
  - Programmable decimation factor (1 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two’s Complement; Truncated)

  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of 0 to 8 bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full-featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wakeup on bus activity

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC564A70.

The sources of the ECC errors are:

- Flash memory
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 parameter RAM)

1.5.23 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.24 Calibration bus interface

The calibration bus interface controls data transfer across the crossbar switch to/from memories or peripherals attached to the calibration tool connector in the calibration address space. The calibration bus interface is only available in the calibration tool.

Features include:

- 3.3 V ± 10% I/O (3.0 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.5.25 Power management controller (PMC)

The PMC contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1), and the 5 V supply of the regulators (VDDREG).

2.2 LBGA208 ballmap[b]

Figure 3. 208-pin LBGA package ballmap (viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_SOUT	DSPI_B_PCS[3]	DSPI_B_SIN	DSPI_B_PCS[0]	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO[99]	DSPI_B_PCS[4]	DSPI_B_PCS[2]	DSPI_B_PCS[1]	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_PCS[5]	SCI_A_TX	GPIO[98]	DSPI_B_SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ETPUA19_O	VRC33	VSS	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO[207]	NC	EMIOS6	EMIOS8	MDO11_ETPUA29_O	MDO4_ETPUA2_O	MDO8_ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P

b. LBGA208 is available upon specific request. Please contact your ST sales office for details.

M	NC	TCRCLKA	NC	NC					NC	NC	VSS
N	NC	NC	NC	NC					VSS	VSS	NC
P	GPIO[12]	GPIO[13]	NC	VRC33					VSS	VSS	NC
R	GPIO[14]	GPIO[15]	VDDE-EH	NC							
T	GPIO[16]	GPIO[17]	NC	NC							
U	NC	NC	NC	NC							
V	NC	NC	NC	NC							
W	NC	VDDE-EH	NC	VSS	VDD	NC	VRC33	NC	NC	NC	NC
Y	NC	NC	VSS	VDD	NC	NC	NC	NC	GPIO[207]	NC	NC
AA	NC	VSS	VDD	NC	NC	NC	GPIO[206]	NC	NC	NC	EMIOS3
AB	VSS	VDD	NC	NC	NC	NC	NC	NC	NC	EMIOS0	EMIOS1
	1	2	3	4	5	6	7	8	9	10	11

Figure 5. 324-pin PBGA package ballmap (southwest, viewed from above)

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
AN20	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[20] / —	—	—	C7
AN21	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[21] / —	173	B4	C8
AN22	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[22] / —	161	B8	C11
AN23	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[23] / —	160	C9	B11
AN24	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[24] / —	159	D8	D12
AN25	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[25] / —	158	B9	C12
AN26	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[26] / —	—	—	B12
AN27	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[27] / —	157	A10	A12
AN28	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[28] / —	156	B10	A13
AN29	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[29] / —	—	—	D13
AN30	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[30] / —	155	D9	C13
AN31	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[31] / —	154	D10	B13
AN32	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[32] / —	153	C10	B14
AN33	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[33] / —	152	C11	C14
AN34	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[34] / —	151	C5	D14
AN35	Single-ended Analog Input	P	—	—	I	VDDA / Analog	I / —	AN[35] / —	150	D11	A14

Table 4. SPC564A70 signal properties (continued)

Name[1]	Function[2]	P / A / G[3]	PCR PA field[4]	PCR[5]	I/O type	Voltage[6] / Pad type[7]	Status[8]		Package pin No.		
							During reset	After reset	176	208[9]	324
VDDEH1AB[19]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH1AB[19]	—	K4	H4
VDDEH4[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4[20]	—	—	—
VDDEH4A[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4A[20]	55	—	—
VDDEH4B[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4B[20]	74	—	—
VDDEH4AB[20]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH4AB[20]	—	N9	W14
VDDEH6[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6[21]	—	—	—
VDDEH6A[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6A[21]	95	—	—
VDDEH6B[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6B[21]	110	—	—
VDDEH6AB[21]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH6AB[21]	—	F13	H19, U19
VDDEH7[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7	—	D12	D15
VDDEH7A[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7A	125	—	—
VDDEH7B[22]	I/O supply input	—		—	I	3.3 V – 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D19, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M11, M12, M13, M14, N9, N10, N12, N13, N14, P9, P10, P12, P13, P14, T21, T22, W4, W19, Y3, Y20, AA2, AA21, AB1, AB22

1. The suffix "_O" identifies an output-only eTPU channel
2. For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or GPIO is done in the SIU except where explicitly noted. See the Signal details table for a description of each signal.
3. The P/A/G column indicates the position a signal occupies in the muxing order for a pin—Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. S setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 - 0b0 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number these values.
4. The Pad Configuration Register (PCR) PA field is used by software to select pin function.
5. Values in the PCR column refer to registers in the System Integration Unit (SIU). The actual register name is "SIU_PCR" suffixed by the PCR num PCR[190] refers to the SIU register named SIU_PCR190.
6. The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V 10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/– 10%).
7. See *Table 5* for details on pad types.
8. The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. Terminology is (weak pull up enabled), Down (weak pull down enabled), Low (output driven low), High (output driven high). A dash for the function in this column input and output buffer are turned off. The signal name to the left or right of the slash indicates the pin is enabled.
9. LBGA208 is available upon specific request. Please contact your ST sales office for details.
10. When used as ETRIG, this pin must be configured as an input. For GPIO it can be configured either as an input or output.
11. Maximum frequency is 50 kHz
12. PCR219 controls two different pins: MCKO and GPIO[219]. Please refer to Pad Configuration Register 219 section in SIU chapter of device refere
13. On LQFP176 and LBGA208 packages, this pin is tied low internally.
14. These pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of this pin once enabled.
15. The BAM uses this pin to select if auto baud rate is on or off.
16. Output only
17. This signal name is used to support legacy naming.
18. Do not use VRC33 to drive external circuits.
19. VDDEH1A, VDDEH1B and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support they should be considered as the same signal in this document.
20. VDDEH4, VDDEH4A, VDDEH4B and VDDEH4AB are shorted together in all production packages. The separation of the signal names is present to however they should be considered as the same signal in this document.
21. VDDEH6, VDDEH6A, VDDEH6B and VDDEH6AB are shorted together in all production packages. The separation of the signal names is present to however they should be considered as the same signal in this document.
22. VDDEH7, VDDEH7A and VDDE7B are shorted together in all production packages. The separation of the signal names is present to support legac should be considered as the same signal in this document.

Table 6. Signal details (continued)

Signal	Module or function	Description
ETPU_A[0:31]	eTPU	eTPU I/O channel
RCH0_[A:C] RCH1_[A:C] RCH2_[A:C] RCH3_[A:C] RCH4_[A:C] RCH5_[A:C]	eTPU2 Reaction Module	eTPU2 reaction channels. Used to control external actuators, e.g., solenoid control for direct injection systems and valve control in automatic transmissions
TCRCLKA	eTPU2	Input clock for TCR time base
CAN_A_TX CAN_B_TX CAN_C_TX	FlexCAN_A – FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_B_RX CAN_C_RX	FlexCAN_A – FlexCAN_C	FlexCAN receive
FR_A_RX FR_B_RX	FlexRay	FlexRay receive (Channels A, B)
FR_A_TX_EN FR_B_TX_EN	FlexRay	FlexRay transmit enable (Channels A, B)
FR_A_TX FR_B_TX	FlexRay	FlexRay transmit (Channels A, B)
JCOMP	JTAG	Enables the JTAG TAP controller
TCK	JTAG	Clock input for the on-chip test logic
TDI	JTAG	Serial test instruction and data input for the on-chip test logic
TDO	JTAG	Serial test data output for the on-chip test logic
TMS	JTAG	Controls test mode operations for the on-chip test logic
$\overline{\text{EVTI}}$	Nexus	$\overline{\text{EVTI}}$ is an input that is read on the negation of $\overline{\text{RESET}}$ to enable or disable the Nexus Debug port. After reset, the $\overline{\text{EVTI}}$ pin is used to initiate program synchronization messages or generate a breakpoint.
$\overline{\text{EVTO}}$	Nexus	Output that provides timing to a development tool for a single watchpoint or breakpoint occurrence
MCKO	Nexus	MCKO is a free running clock output to the development tools which is used for timing of the MDO and $\overline{\text{MSEO}}$ signals.
MDO[0:11]	Nexus	Trace message output to development tools. This pin also indicates the status of the crystal oscillator clock following a power-on reset, when MDO[0] is driven high until the crystal oscillator clock achieves stability and is then negated.
$\overline{\text{MSEO}}$[0:1]	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the SPC564A70 series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using *Equation 4*:

Equation 4 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

- Semiconductor Equipment and Materials International
  3081 Zanker Road
  San Jose, CA 95134
  USA
  Phone (+1) 408-943-6900
- MIL-SPEC and EIA/JESD (JEDEC) specifications available from Global Engineering Documents (phone (+1) 800-854-7179 or (+1) 303-397-7956)
- JEDEC specifications available on the Web at www.jedec.org
- C.E. Triplett and B. Joiner, “*An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “*Thermal Modeling of a PBGA for Air-Cooled Applications*”, Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “*Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 25. DSPI LVDS pad specification

Symbol	C		Parameter	Condition	Value			Unit
					Min	Typ	Max	
Data rate								
$f_{LVDSCLK}$	CC	D	Data frequency	—	—	50	—	MHz
Driver specifications								
V_{OD}	CC	P	Differential output voltage	SRC = 0b00 or 0b11	150	—	400	mV
	CC	P		SRC = 0b01	90	—	320	
	CC	P		SRC = 0b10	160	—	480	
V_{OC}	CC	P	Common mode voltage (LVDS), VOS	—	1.06	1.2	1.39	V
T_R/T_F	CC	D	Rise/Fall time	—	—	2	—	ns
T_{PLH}	CC	D	Propagation delay (Low to High)	—	—	4	—	ns
T_{PHL}	CC	D	Propagation delay (High to Low)	—	—	4	—	ns
t_{PDSYNC}	CC	D	Delay (H/L), sync mode	—	—	4	—	ns
T_{DZ}	CC	D	Delay, Z to Normal (High/Low)	—	—	500	—	ns
T_{SKEW}	CC	D	Differential skew Itphla-tplhbI or Itplhb-tphlaI	—	—	—	0.5	ns
Termination								
	CC	D	Transmission line (differential Zo)	—	95	100	105	W
	CC	D	Temperature	—	–40	—	150	°C

3.10 Oscillator and PLLMRFM electrical characteristics

Table 26. PLLMRFM electrical specifications(1)

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol	C		Parameter	Conditions	Value		Unit
					Min	Max	
$f_{ref\_crystal}$	C	P	PLL reference frequency range(2)	Crystal reference	4	40	MHz
f_{ref_ext}	C	P		External reference	4	80	
f_{pll_in}	C	D	Phase detector input frequency range (after pre-divider)	—	4	16	MHz

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1)

Max. Flash Operating Frequency (MHz)(2)	APC(3)	RWSC(3)	WWSC
20 MHz	0b000	0b000	0b01
61 MHz	0b001	0b001	0b01
90 MHz	0b010	0b010	0b01
123 MHz	0b011	0b011	0b01
153 MHz	0b100	0b100	0b01

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. Max frequencies including 2% PLL FM.
3. APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications(1)

#	Symbol		C	Parameter	Value				Unit
					Min	Typ	Initial max(2)	Max(3)	
1	$T_{dwprogram}$	CC	C	Double Word (64 bits) Program Time	—	30	—	500	µs
2	$T_{pprogram}$	CC	C	Page Program Time(4)	—	40	160	500	µs
3	$T_{16kpperase}$	CC	C	16 KB Block Pre-program and Erase Time	—	—	1000	5000	ms
5	$T_{64kpperase}$	CC	C	64 KB Block Pre-program and Erase Time	—	—	1800	5000	ms
6	$T_{128kpperase}$	CC	C	128 KB Block Pre-program and Erase Time	—	—	2600	7500	ms
7	$T_{256kpperase}$	CC	C	256 KB Block Pre-program and Erase Time	—	—	5200	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

The tool/debugger must provide at least one TCK clock for the $\overline{EVTI}$ signal to be recognized by the MCU. When using the RDY signal to indicate the end of a Nexus read/write access, ensure that TCK continues to run for at least one TCK after leaving the Update-DR state. This can be just a TCK with TMS low while in the Run-Test/Idle state or by continuing with the next Nexus/JTAG command. Expect the effect of $\overline{EVTI}$ and RDY to be delayed by edges of TCK.

RDY is not available in all device packages.

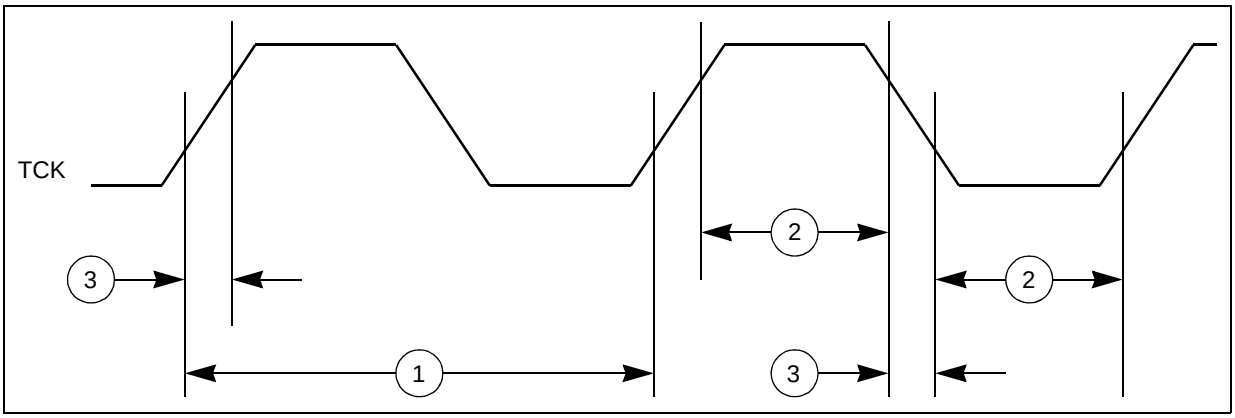


Figure 12. JTAG test clock input timing

Figure 16. Nexus output timing

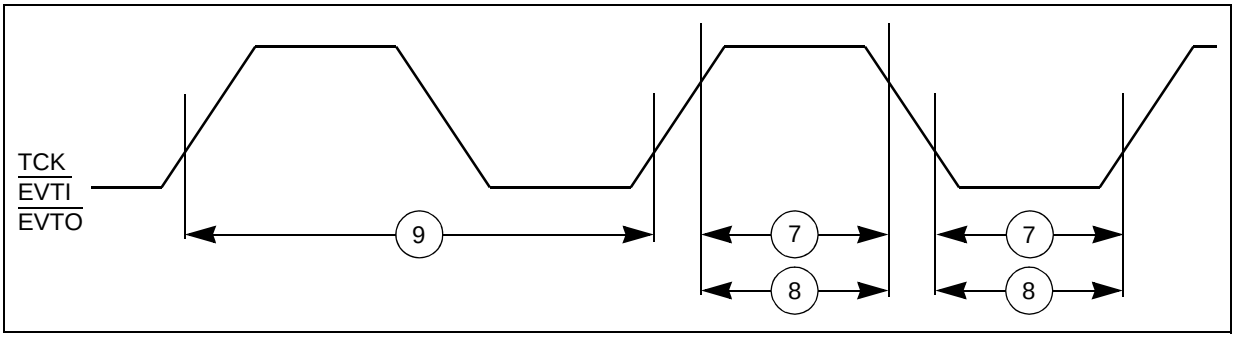


Figure 17. Nexus event trigger and test clock timings

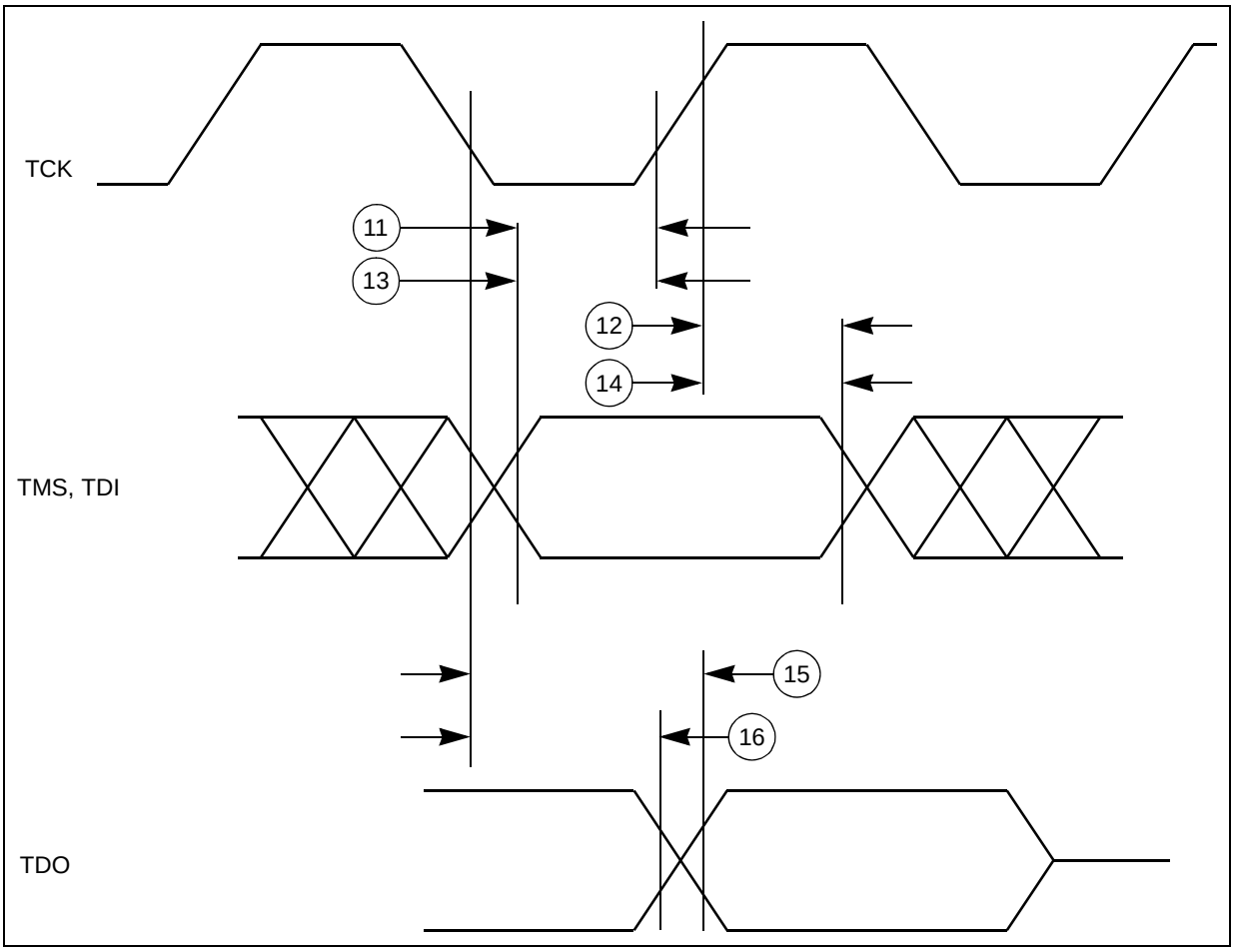


Figure 18. Nexus TDI, TMS, TDO timing

Table 42. Calibration bus operation timing(1) (continued)

#	Symbol		C	Characteristic	66 MHz(2)		Unit
					Min	Max	
8	t_{CIH}	CC	P	CLKOUT Posedge to Input Signal Invalid (Hold Time) DATA[0:31]	1.0	—	ns
9	t_{APW}	CC	P	ALE Pulse Width(5)	6.5	—	ns
10	t_{AAI}	CC	P	ALE Negated to Address Invalid(5)	1.5(6)	—	ns

1. Calibration bus timing specified at f_{SYS} = 150 MHz and 100 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. The calibration bus is limited to half the speed of the internal bus. The maximum calibration bus frequency is 66 MHz. The bus division factor should be set accordingly based on the internal frequency being used.
3. Signals are measured at 50% V_{DDE}
4. Refer to fast pad timing in *Table 35* and *Table 36* (different values for 1.8 V vs. 3.3 V).
5. Measured at 50% of ALE
6. When CAL_TS pad is used for CAL_ALE function the hold time is 1 ns instead of 1.5 ns.

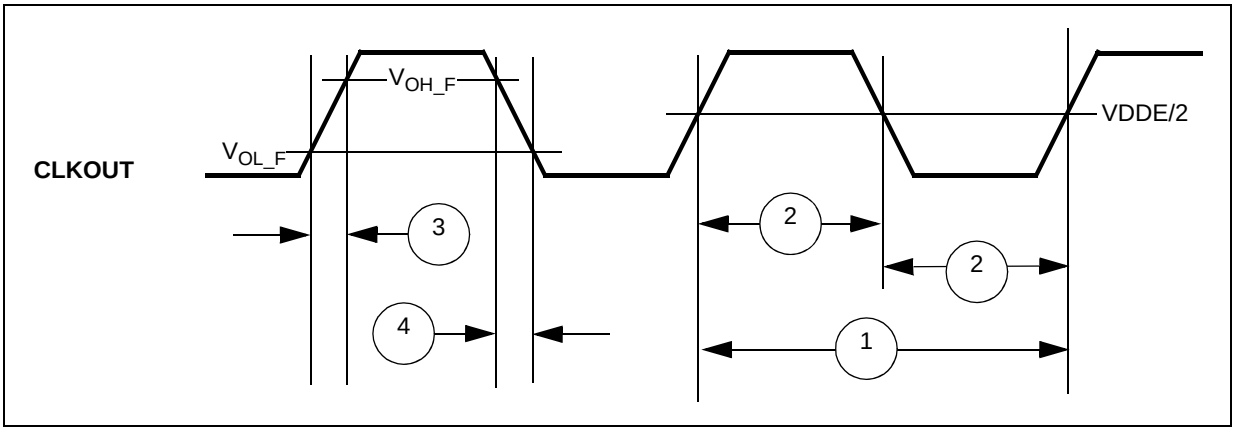


Figure 19. CLKOUT timing

Table 47. DSPI timing[1][2] (continued)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
9	t_{SUI}	CC	Data Setup Time for Inputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	20	—	ns
			D		V_{DDEH}=3–3.6 V	22	—	
			D	Slave		2	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		8	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	20	—	
			D		V_{DDEH}=3–3.6 V	22	—	
10	t_{HI}	CC	Data Hold Time for Inputs					
			D	Master (MTFE = 0)		–4	—	ns
			D	Slave		7	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		21	—	
			D	Master (MTFE = 1, CPHA = 1)		–4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	—	5	ns
			D		V_{DDEH}=3–3.6 V	—	6.3	
			D	Slave	V_{DDEH}=4.75–5.25 V	—	25	
			D		V_{DDEH}=3–3.6 V	—	25.7	
			D	Master (MTFE = 1, CPHA = 0)		—	21	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	—	5	
			D		V_{DDEH}=3–3.6 V	—	6.3	
12	t_{HO}	CC	Data Hold Time for Outputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.75–5.25 V	–5	—	ns
			D		V_{DDEH}=3–3.6 V	–6.3	—	
			D	Slave		5.5	—	
			D	Master (MTFE = 1, CPHA = 0)		3	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.75–5.25 V	–5	—	
			D		V_{DDEH}=3–3.6 V	–6.3	—	

1. All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type pad_msr. DSPI signals using pad type of pad_ssr have an additional delay based on the slew rate. DSPI timing is specified at V_{DDEH} = 3.0 to 3.6 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b11.
2. Data is verified at f_{SYS} = 102 MHz and 153 MHz (100 MHz and 150 MHz + 2% frequency modulation).
3. The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two SPC564A70 devices communicating over a DSPI link.
4. The actual minimum SCK cycle time is limited by pad performance.
5. For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.
6. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].
7. Timing met when PCSSCK = 3 (01), and CSSCK = 2 (0000)