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Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nexperia/p80c32ubaa-518

80C51 8-bit microcontroller family
128/256 byte RAM ROMless low voltage (2.7V–5.5V),
low power, high speed (33 MHz)

80C31/80C32

80C51/87C51 AND 80C31 ORDERING INFORMATION

ROMless	TEMPERATURE RANGE °C AND PACKAGE	VOLTAGE RANGE	FREQ. (MHz)	DRAWING NUMBER
P80C31SBPN	0 to +70, Plastic Dual In-line Package	2.7 V to 5.5 V	0 to 16	SOT129-1
P80C31SBAA	0 to +70, Plastic Leaded Chip Carrier	2.7 V to 5.5 V	0 to 16	SOT187-2
P80C31SBBB	0 to +70, Plastic Quad Flat Pack	2.7 V to 5.5 V	0 to 16	SOT307-2
P80C31SFPN	–40 to +85, Plastic Dual In-line Package	2.7 V to 5.5 V	0 to 16	SOT129-1
P80C31SFA A	–40 to +85, Plastic Leaded Chip Carrier	2.7 V to 5.5 V	0 to 16	SOT187-2
P80C31SFBB	–40 to +85, Plastic Quad Flat Pack	2.7 V to 5.5 V	0 to 16	SOT307-2

PART NUMBER DERIVATION

DEVICE NUMBER	OPERATING FREQUENCY, MAX (S)	TEMPERATURE RANGE (B)	PACKAGE (AA)
P80C31	S = 16 MHz	B = 0° to +70°C	AA = PLCC
P80C32	U = 33 MHz	F = –40°C to +85°C	BB = PQFP PN = PDIP

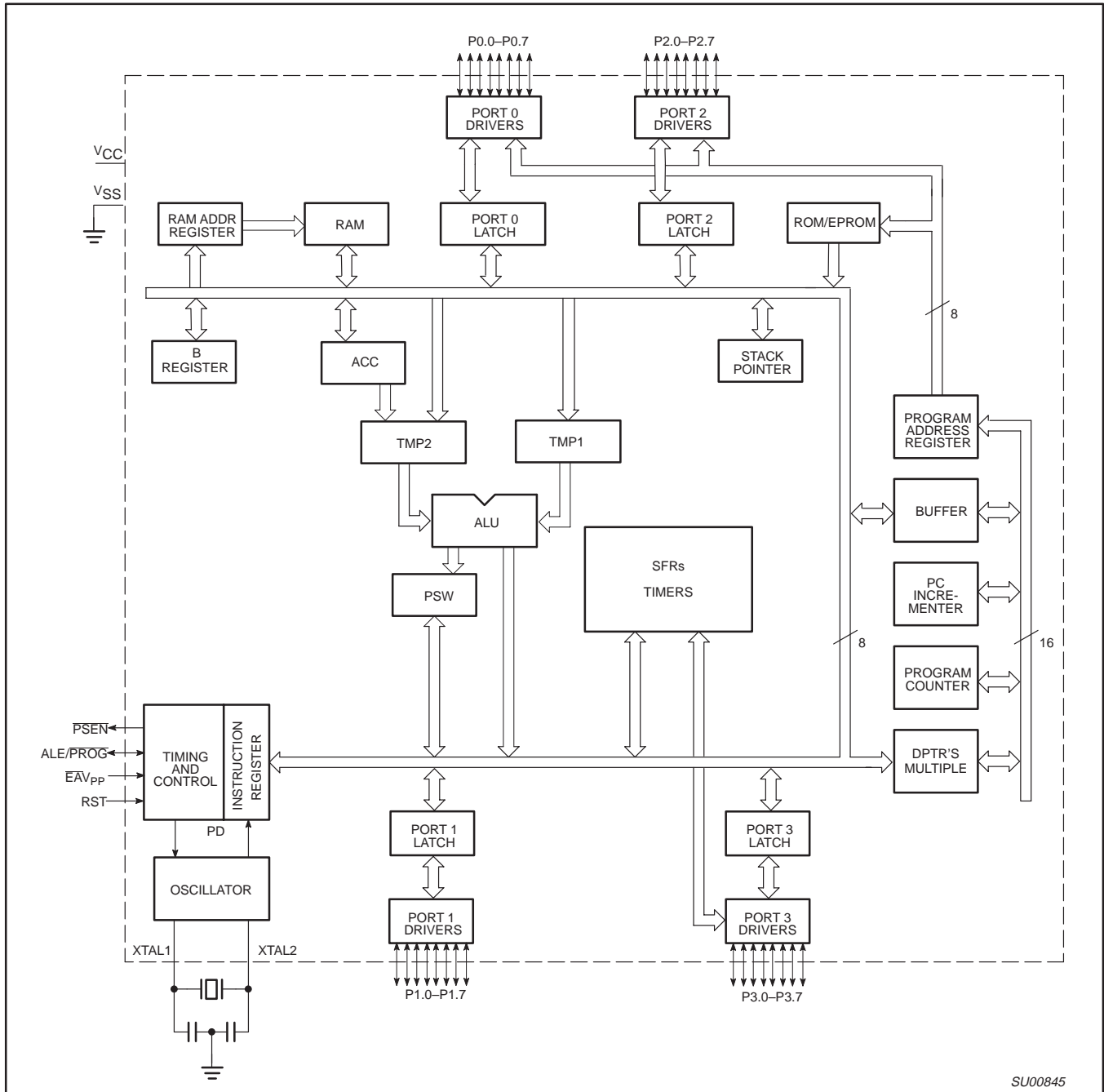
80C32 ORDERING INFORMATION

ROMless	TEMPERATURE RANGE °C AND PACKAGE	FREQ MHz	DRAWING NUMBER
P80C32SBP N	0 to +70, Plastic Dual In-line Package	16	SOT129-1
P80C32SBA A	0 to +70, Plastic Leaded Chip Carrier	16	SOT187-2
P80C32SBB B	0 to +70, Plastic Quad Flat Pack	16	SOT307-2
P80C32SFP N	–40 to +85, Plastic Dual In-line Package	16	SOT129-1
P80C32SFA A	–40 to +85, Plastic Leaded Chip Carrier	16	SOT187-2
P80C32SFB B	–40 to +85, Plastic Quad Flat Pack	16	SOT307-2
P80C32UBA A	0 to +70, Plastic Leaded Chip Carrier	33	SOT187-2
P80C32UBP N	0 to +70, Plastic Dual In-line Package	33	SOT129-1
P80C32UBB B	0 to +70, Plastic Quad Flat Pack	33	SOT307-2
P80C32UFA A	–40 to +85, Plastic Leaded Chip Carrier	33	SOT187-2
P80C32UFP N	–40 to +85, Plastic Dual In-line Package	33	SOT129-1
P80C32UFB B	–40 to +85, Plastic Quad Flat Pack	33	SOT307-2

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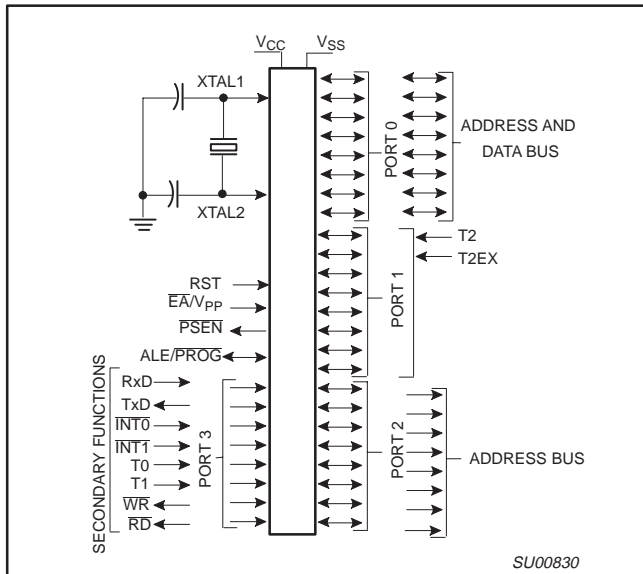
BLOCK DIAGRAM



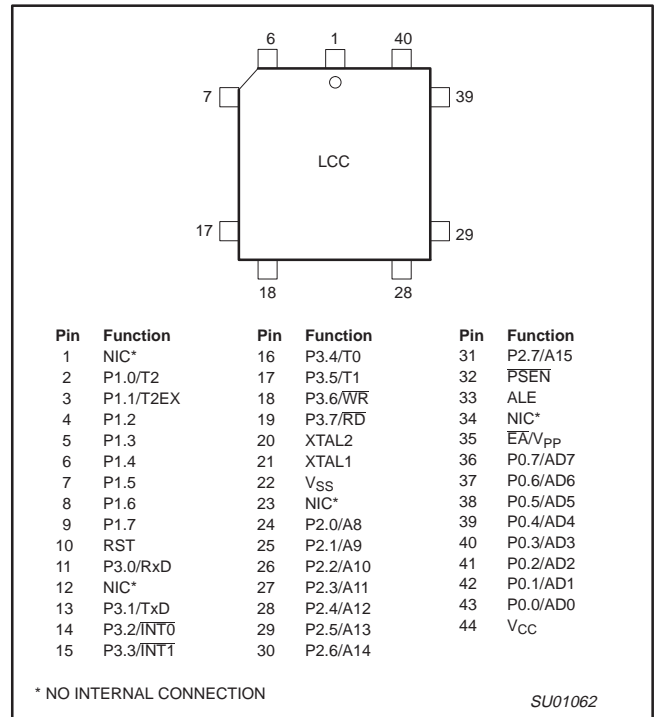
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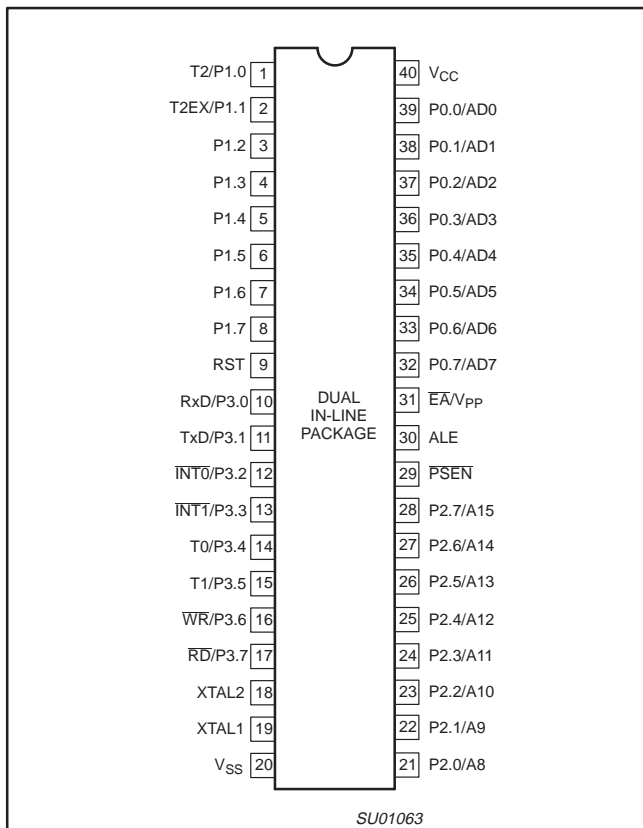
LOGIC SYMBOL



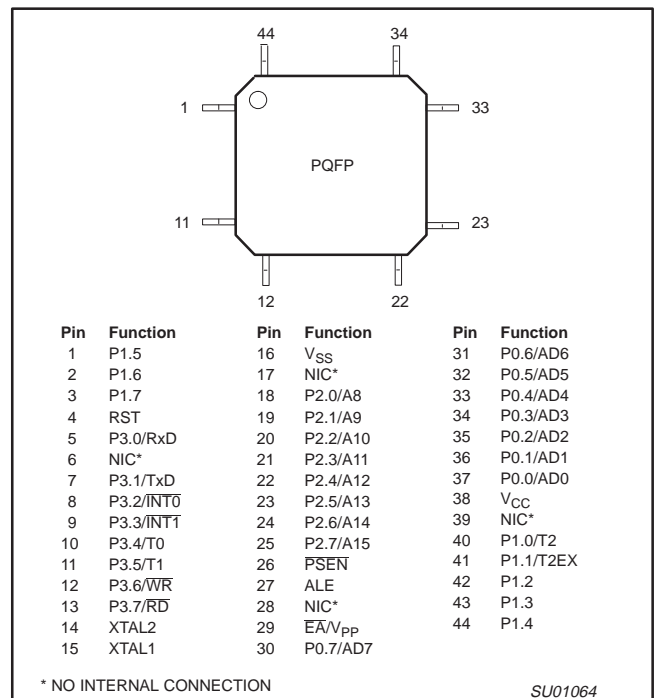
PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



PIN CONFIGURATIONS



PLASTIC QUAD FLAT PACK PIN FUNCTIONS



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Table 1. 8XC51/80C31 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	–	AO	xxxxxxx0B
AUXR1#	Auxiliary 1	A2H	–	–	–	–	WUPD ²	0	–	DPS	xxx000x0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	–	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
			B7	B6	B5	B4	B3	B2	B1	B0	
IPH#	Interrupt Priority High	B7H	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xx000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH
PCON# ¹	Power Control	87H	SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL	00xx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	000000x0B
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	T1	R1	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T ²	CP/RL2	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

NOTE:

Unused register bits that are not defined should not be set by the user's program. If violated, the device could function incorrectly.

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

– Reserved bits.

1. Reset value depends on reset source.

2. Not available on 80C31.

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OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

For the 80C31 or 80C32, either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values. WUPD (AUXR1.3–Wakeup from Power Down) enables or disables the wakeup from power down with external interrupt. Where:

- WUPD = 0 Disable
- WUPD = 1 Enable

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

For the 80C31, wakeup from power down is always enabled.

Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE (“On-Circuit Emulation”) Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and \overline{PSEN} is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and \overline{PSEN} are weakly pulled high. The oscillator circuit remains active. While the 80C31/32 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	\overline{PSEN}	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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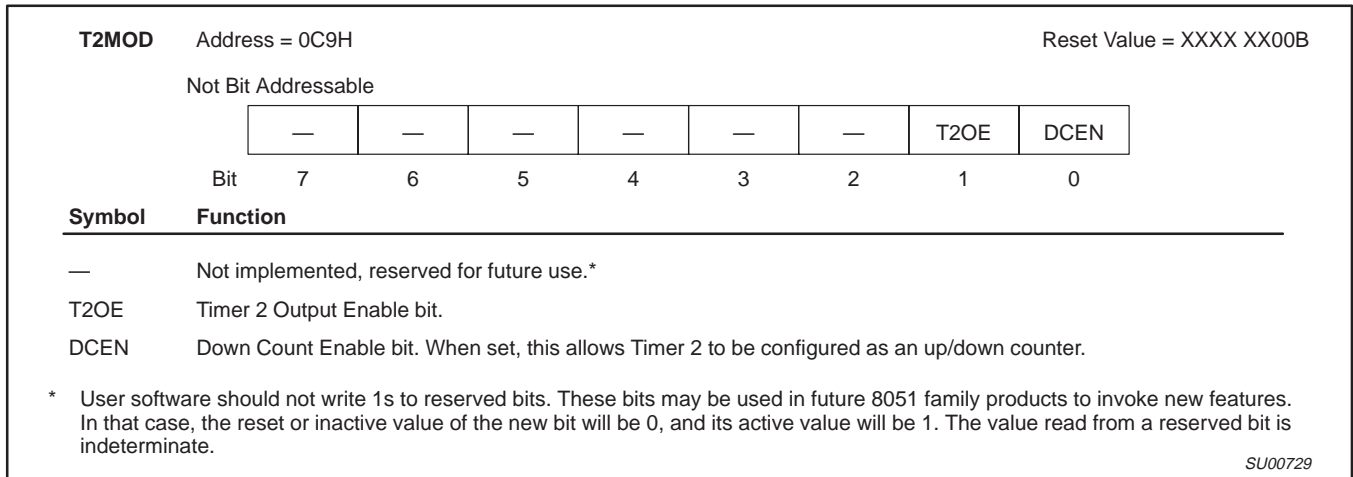


Figure 3. Timer 2 Mode (T2MOD) Control Register

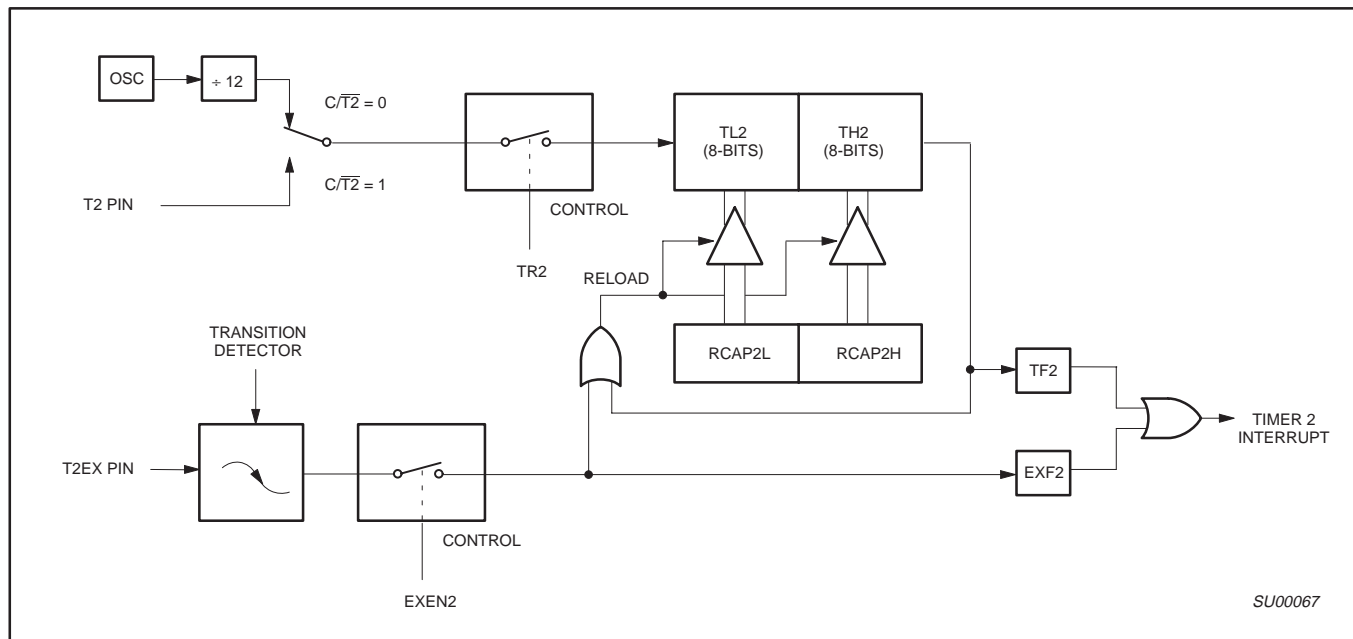


Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)

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Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 3) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 6 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation (C/T2=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/12 the oscillator frequency). As a baud rate generator, it increments every state time (i.e., 1/2 the oscillator frequency). Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where: (RCAP2H, RCAP2L)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 6, is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time (osc/2) or asynchronously from pin T2;

under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

Table 4. Timer 2 Generated Commonly Used Baud Rates

Baud Rate	Osc Freq	Timer 2	
		RCAP2H	RCAP2L
375 K	12 MHz	FF	FF
9.6 K	12 MHz	FF	D9
2.8 K	12 MHz	FF	B2
2.4 K	12 MHz	FF	64
1.2 K	12 MHz	FE	C8
300	12 MHz	FB	1E
110	12 MHz	F2	AF
300	6 MHz	FD	8F
110	6 MHz	F9	57

Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{\text{osc}}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where f_{osc}= Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H, RCAP2L} = 65536 - \left(\frac{f_{\text{osc}}}{32 \times \text{Baud Rate}} \right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

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Table 5. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 6. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 80C31/32 UART also fully supports multiprocessor communication.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 8.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 9.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the

SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

```
Slave 0   SADDR = 1100 0000
          SADEN = 1111 1101
          Given = 1100 00X0

Slave 1   SADDR = 1100 0000
          SADEN = 1111 1110
          Given = 1100 000X
```

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

```
Slave 0   SADDR = 1100 0000
          SADEN = 1111 1001
          Given = 1100 0XX0

Slave 1   SADDR = 1110 0000
          SADEN = 1111 1010
          Given = 1110 0X0X

Slave 2   SADDR = 1110 0000
          SADEN = 1111 1100
          Given = 1110 00XX
```

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0

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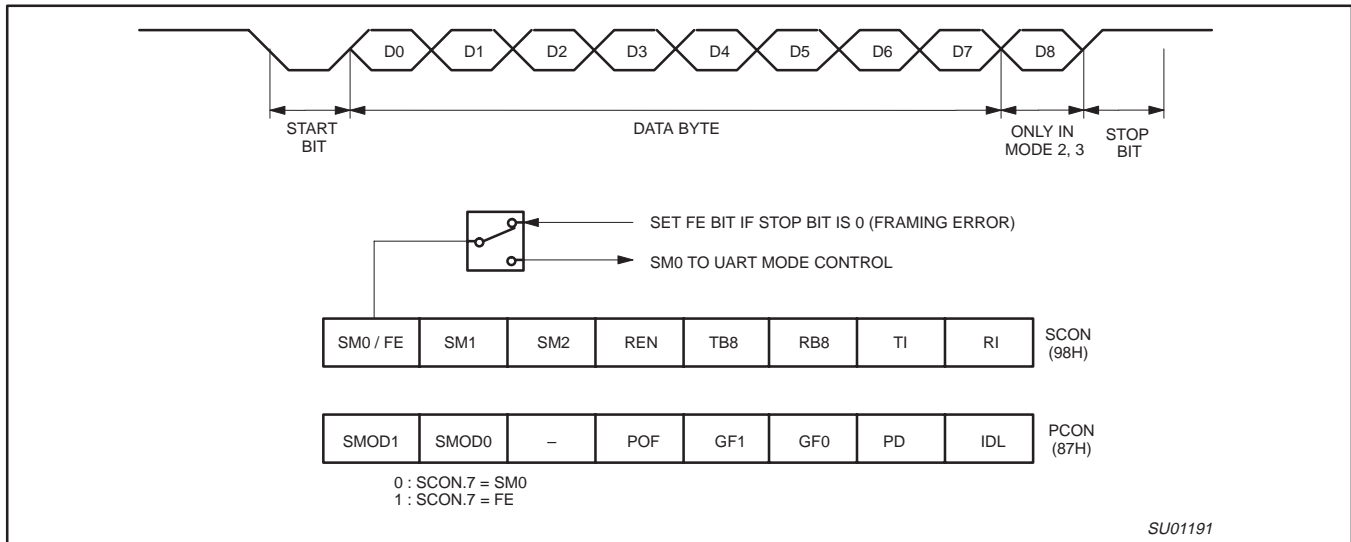


Figure 8. UART Framing Error Detection

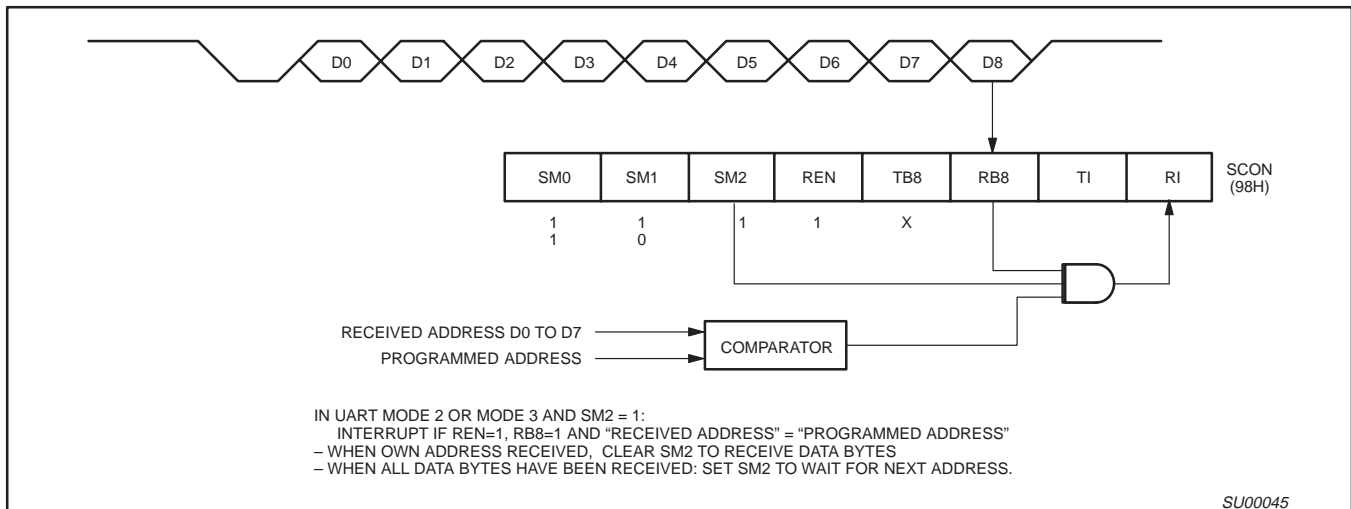


Figure 9. UART Multiprocessor Communication, Automatic Address Recognition

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Interrupt Priority Structure

The 80C31 and 80C32 have a 6-source four-level interrupt structure. They are the IE, IP and IPH. (See Figures 10, 11, and 12.) The IPH (Interrupt Priority High) register that makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 12.

An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 7. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L) ¹ Y (T) ²	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
SP	5	RI, TI	N	23H
T2	6	TF2, EXF2	N	2BH

NOTES:

- 1. L = Level activated
- 2. T = Transition activated

		7	6	5	4	3	2	1	0
IE (0A8H)		EA	—	ET2	ES	ET1	EX1	ET0	EX0
		Enable Bit = 1 enables the interrupt. Enable Bit = 0 disables it.							
BIT	SYMBOL	FUNCTION							
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.							
IE.6	—	Not implemented. Reserved for future use.							
IE.5	ET2	Timer 2 interrupt enable bit.							
IE.4	ES	Serial Port interrupt enable bit.							
IE.3	ET1	Timer 1 interrupt enable bit.							
IE.2	EX1	External interrupt 1 enable bit.							
IE.1	ET0	Timer 0 interrupt enable bit.							
IE.0	EX0	External interrupt 0 enable bit.							

SU00571

Figure 10. IE Registers

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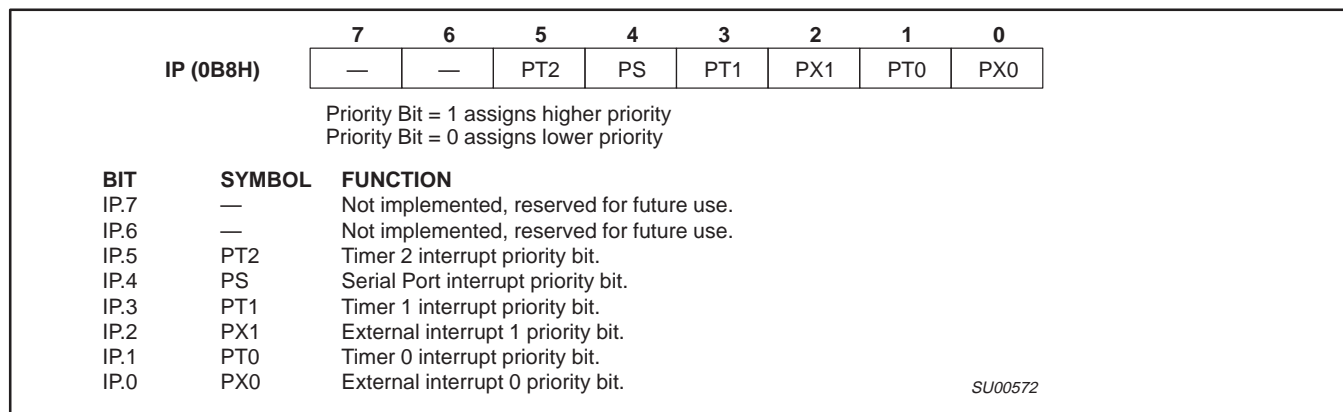


Figure 11. IP Registers

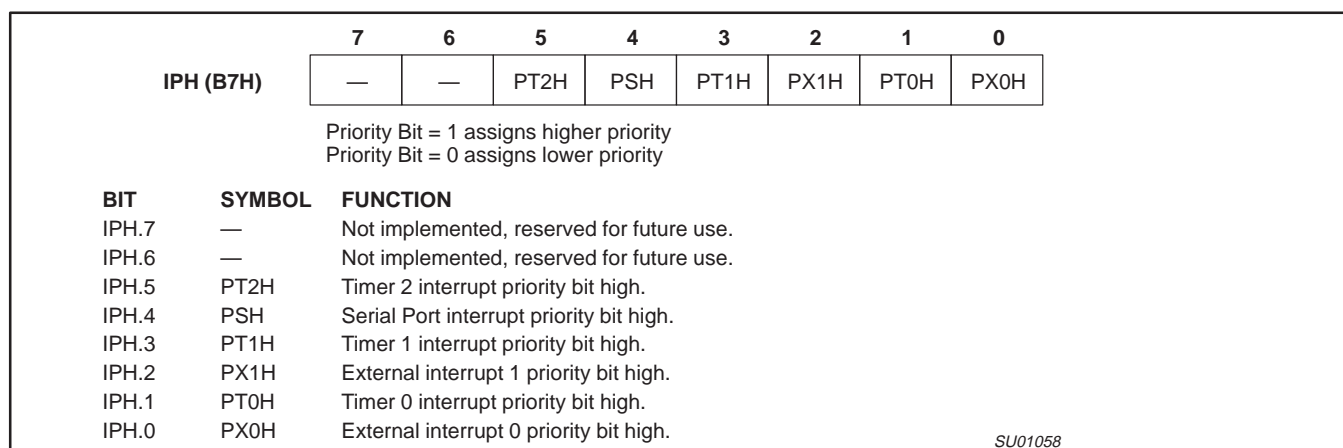


Figure 12. IPH Registers

80C51 8-bit microcontroller family
 128/256 byte RAM ROMless low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

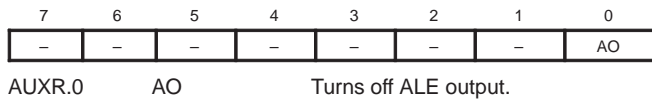
80C31/80C32

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

Reduced EMI Mode

AUXR (8EH)



Dual DPTR

The dual DPTR structure (see Figure 13) enables a way to specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxx000x0B

AUXR1 (A2H)



Where:

DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC DPTR instruction without affecting the WOPD or LPEP bits.

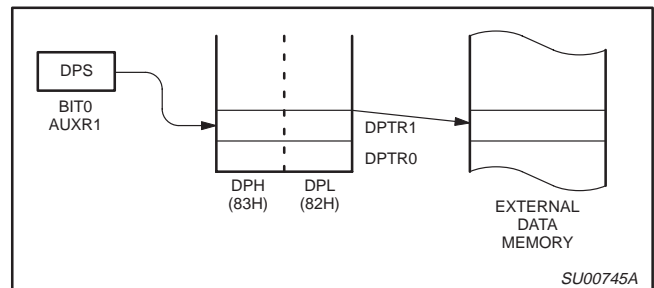


Figure 13.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR, A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

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DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$, 33 MHz devices; $5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage	$4.5\text{ V} < V_{CC} < 5.5\text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, E \bar{A})		$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7 V_{CC}$		$V_{CC} + 0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 1.6\text{ mA}^2$			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ^{7, 8}	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 3.2\text{ mA}^2$			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -30\mu\text{A}$	$V_{CC} - 0.7$			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , PSEN ³	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -3.2\text{ mA}$	$V_{CC} - 0.7$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4\text{ V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0\text{ V}$ See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current (see Figure 21): Active mode (see Note 5) Idle mode (see Note 5) Power-down mode or clock stopped (see Figure 25 for conditions)	See note 5 $T_{amb} = 0^{\circ}\text{C}$ to 70°C $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		3	50 75	μA μA
R_{RST}	Internal reset pull-down resistor		40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except E \bar{A})				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100\text{ pF}$), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
- See Figures 22 through 25 for I_{CC} test conditions.
Active mode: $I_{CC(MAX)} = 0.9 \times \text{FREQ.} + 1.1\text{ mA}$
Idle mode: $I_{CC(MAX)} = 0.18 \times \text{FREQ.} + 1.0\text{ mA}$; See Figure 21.
- This value applies to $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$. For $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $I_{TL} = -750\mu\text{A}$.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85°C specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except E \bar{A} is 25 pF).

80C51 8-bit microcontroller family
 128/256 byte RAM ROMless low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A – Address
- C – Clock
- D – Input data
- H – Logic level high
- I – Instruction (program memory contents)
- L – Logic level low, or ALE

- P – $\overline{\text{PSEN}}$
- Q – Output data
- R – $\overline{\text{RD}}$ signal
- t – Time
- V – Valid
- W – $\overline{\text{WR}}$ signal
- X – No longer a valid logic level
- Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

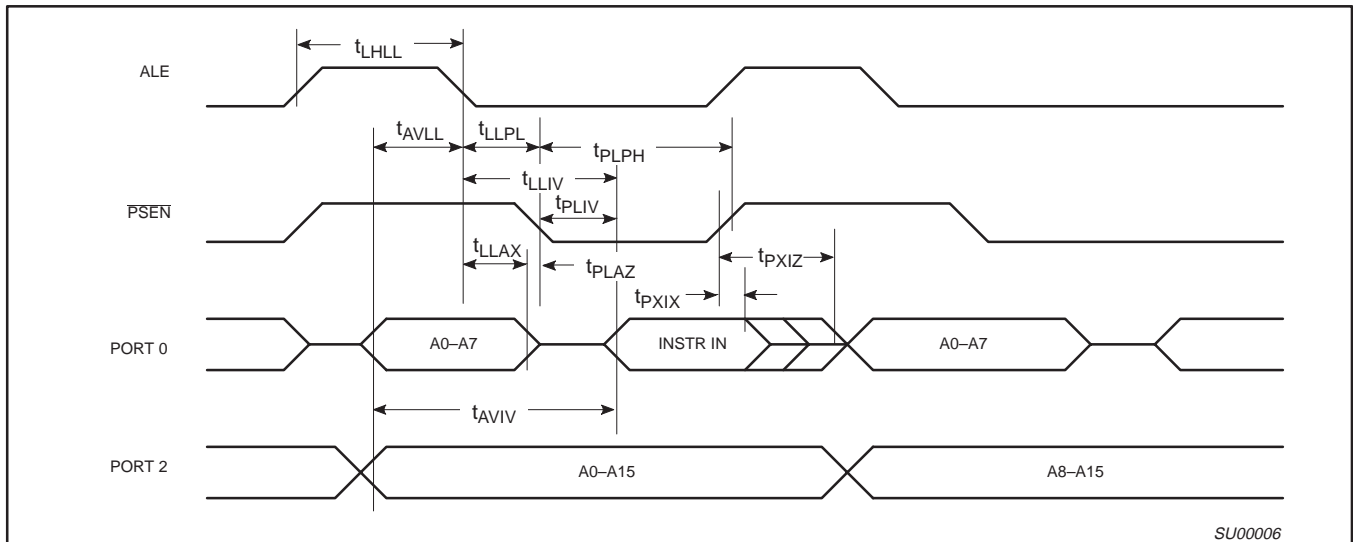


Figure 14. External Program Memory Read Cycle

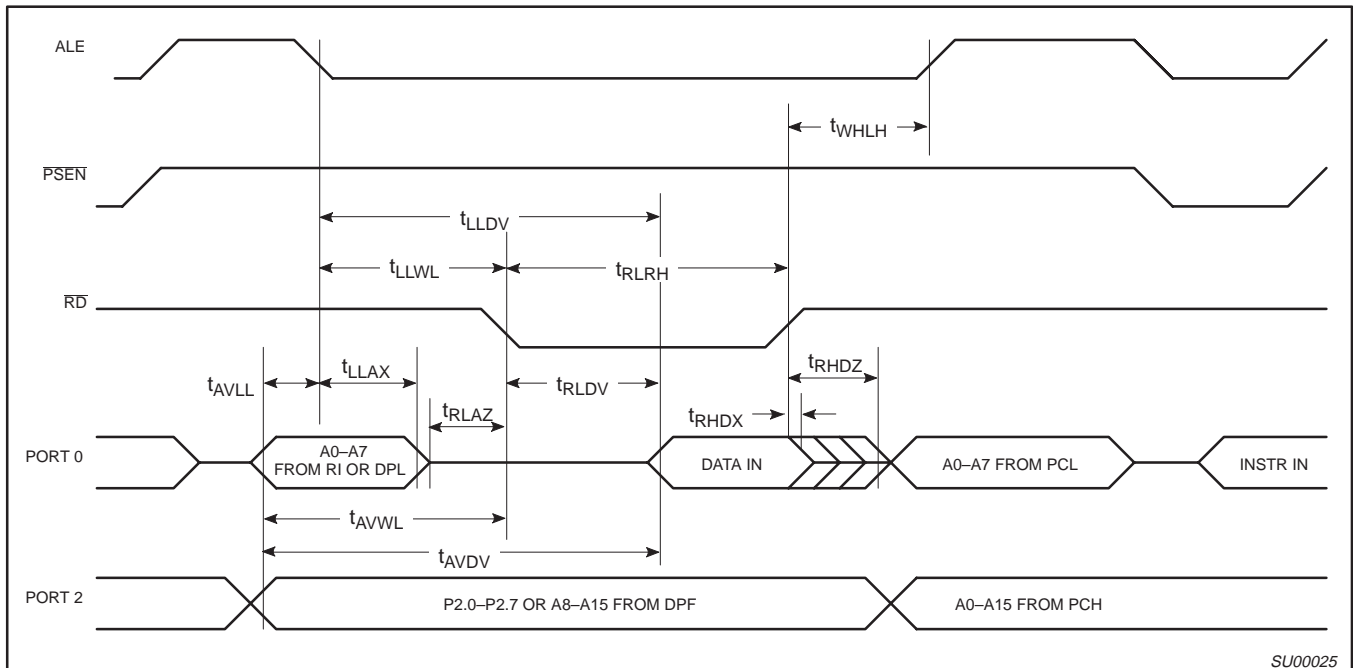


Figure 15. External Data Memory Read Cycle

80C51 8-bit microcontroller family
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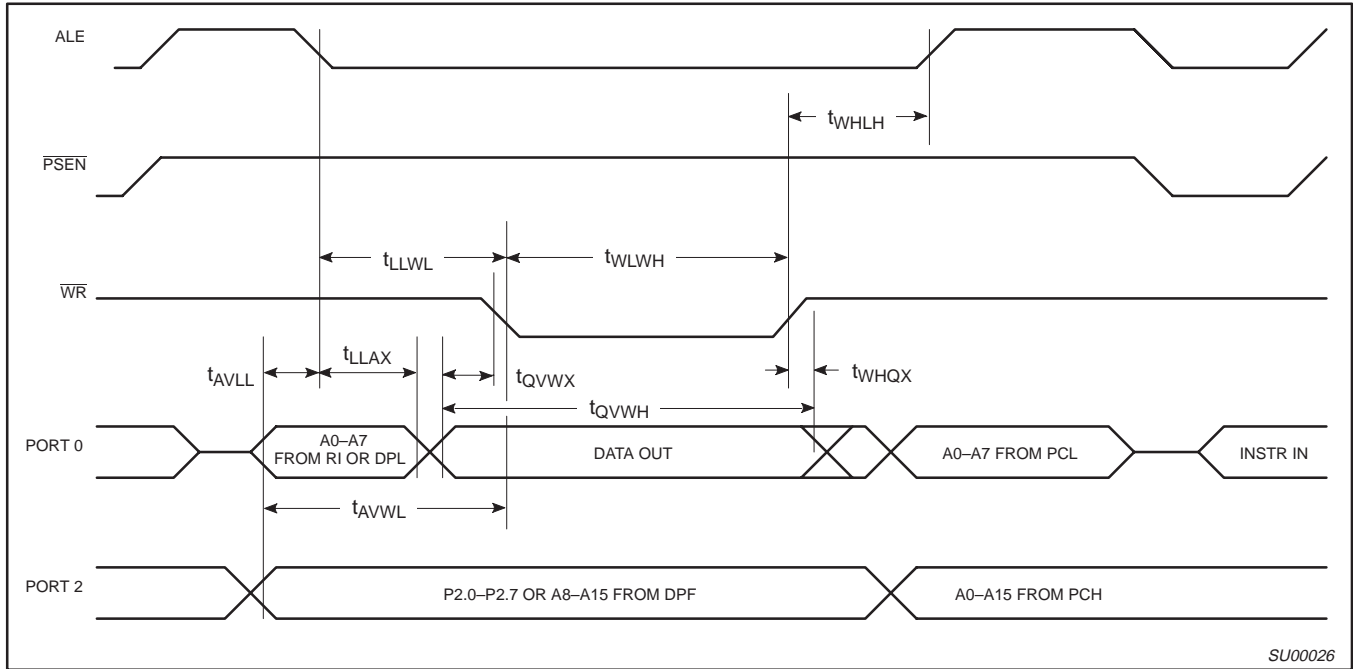


Figure 16. External Data Memory Write Cycle

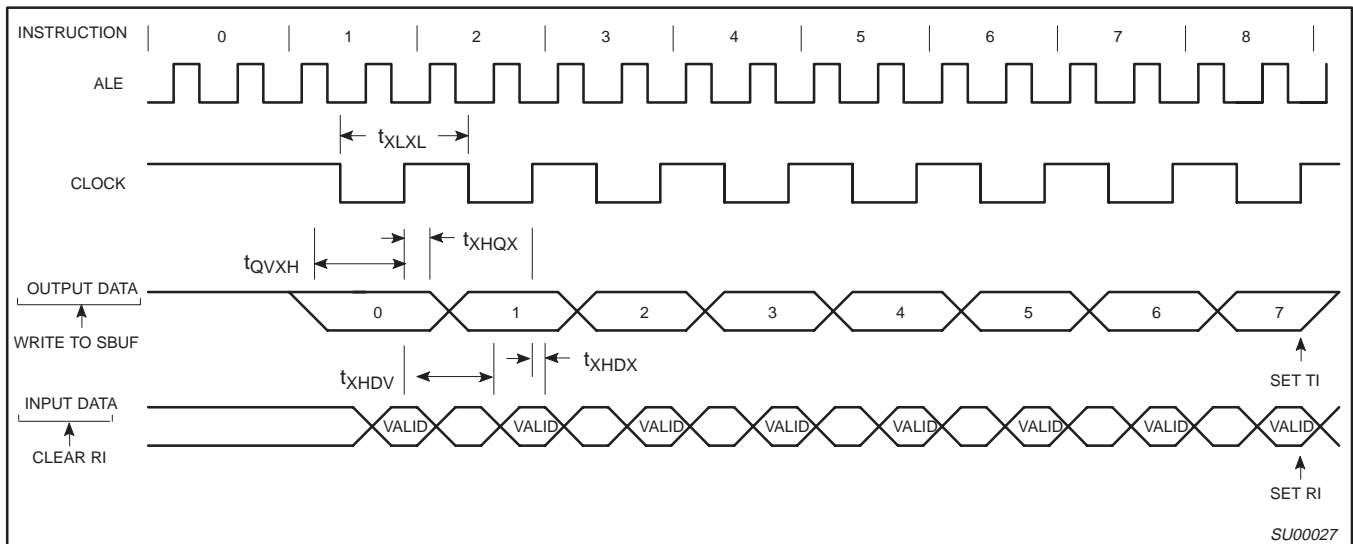


Figure 17. Shift Register Mode Timing

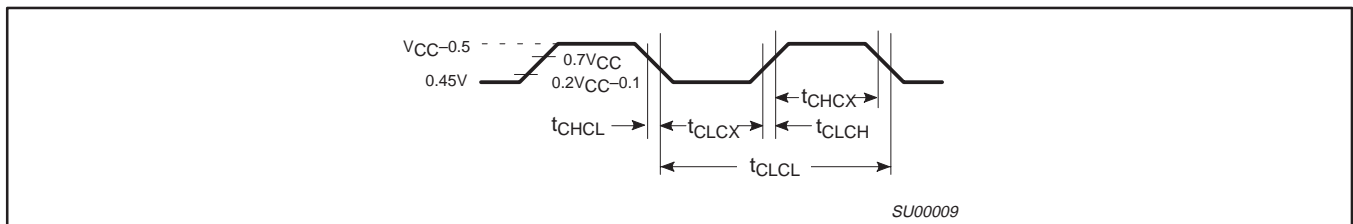


Figure 18. External Clock Drive

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 low power, high speed (33 MHz)

80C31/80C32

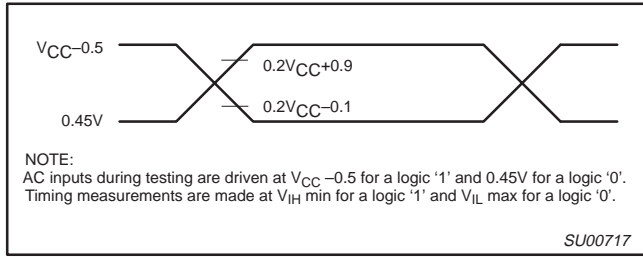


Figure 19. AC Testing Input/Output

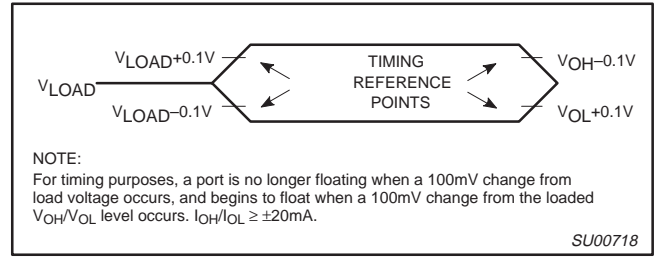


Figure 20. Float Waveform

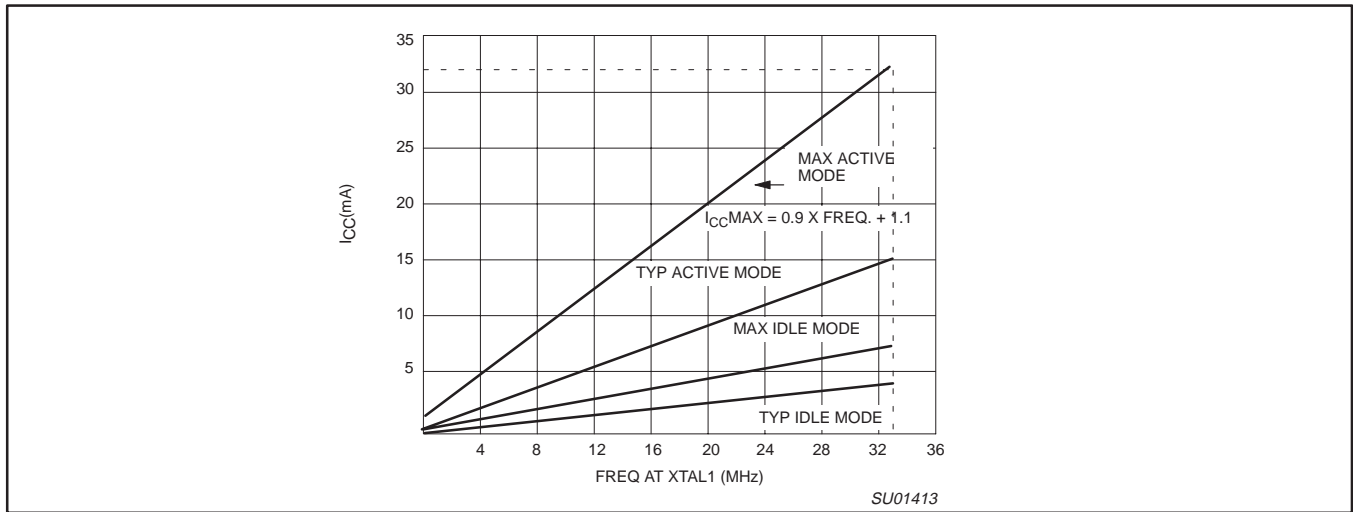


Figure 21. I_{CC} vs. FREQ
 Valid only within frequency specifications of the device under test

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 128/256 byte RAM ROMless low voltage (2.7V–5.5V),
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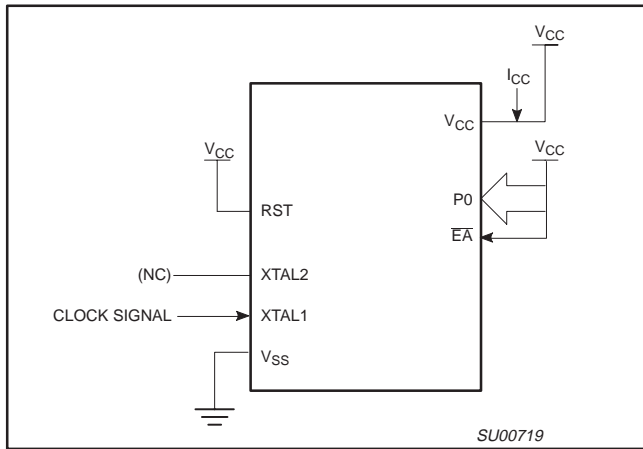


Figure 22. I_{CC} Test Condition, Active Mode
 All other pins are disconnected

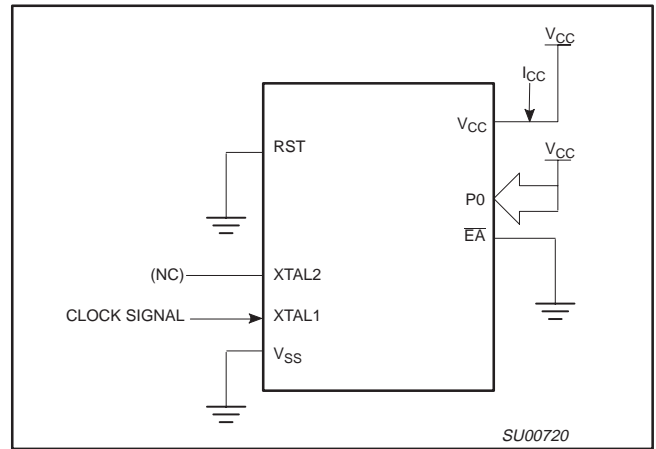


Figure 23. I_{CC} Test Condition, Idle Mode
 All other pins are disconnected

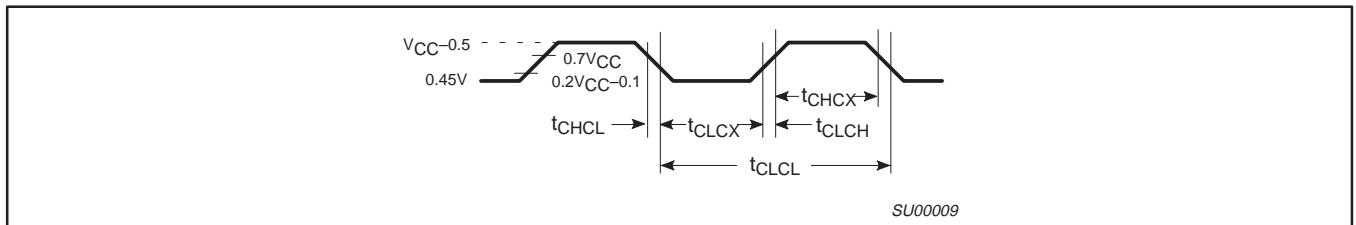


Figure 24. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$

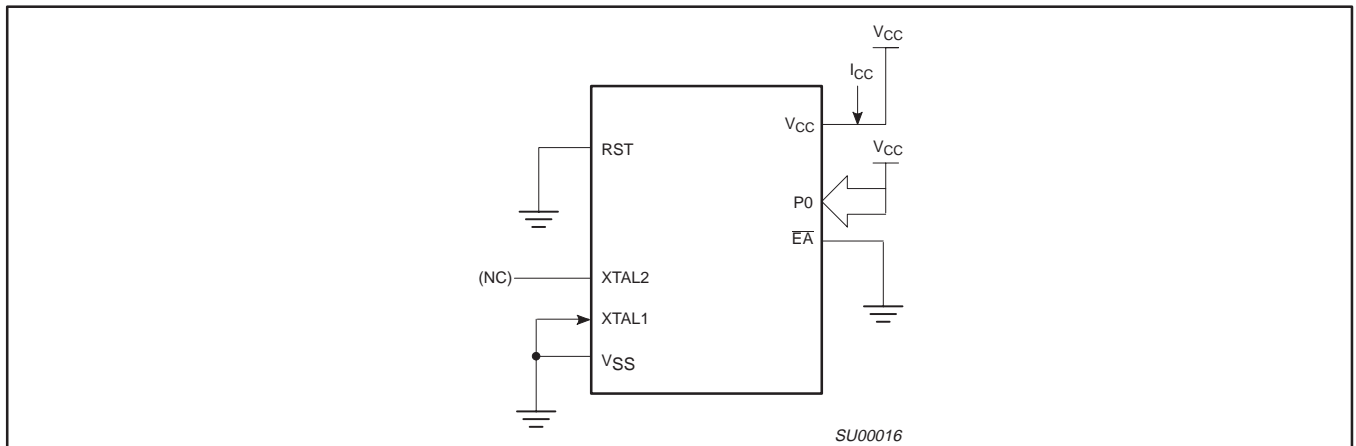


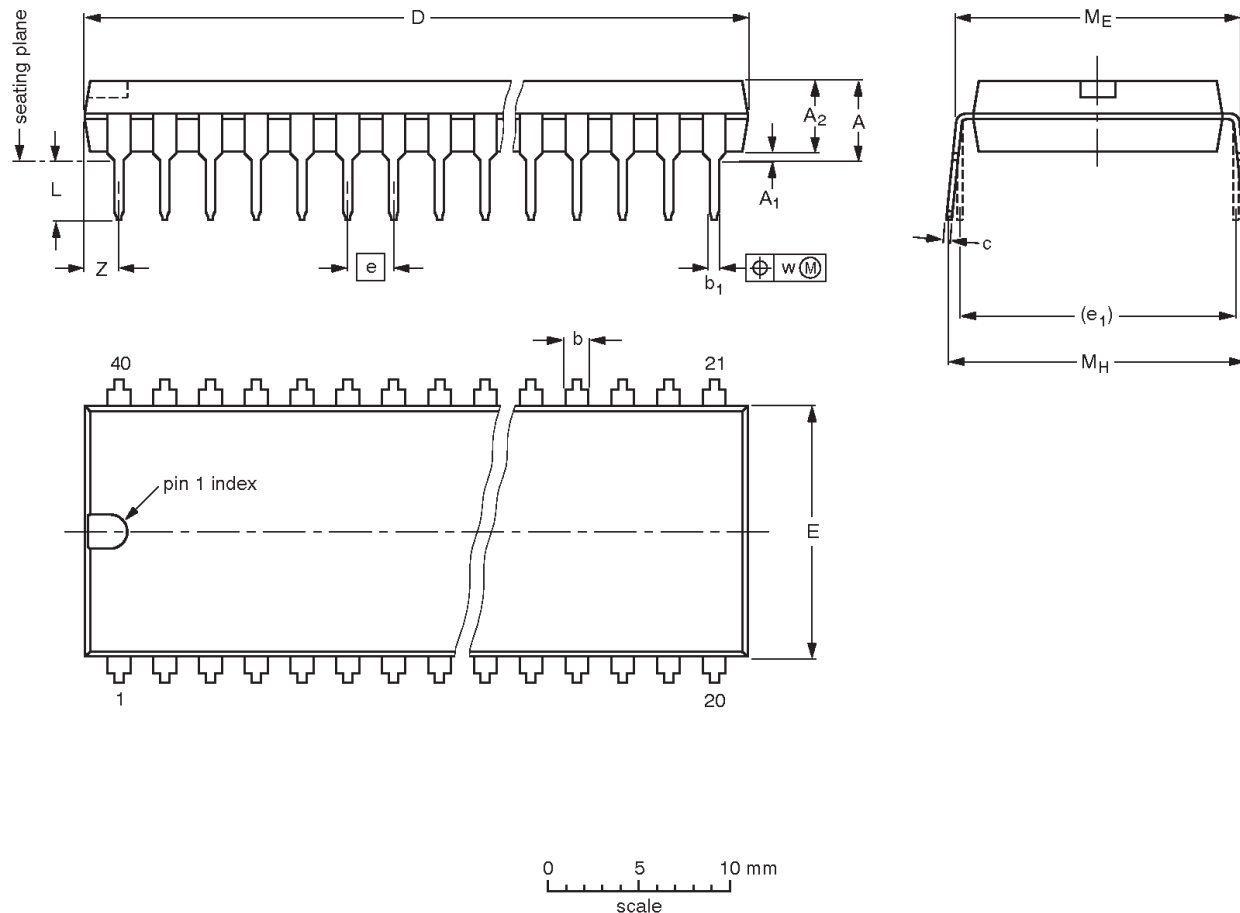
Figure 25. I_{CC} Test Condition, Power Down Mode
 All other pins are disconnected. $V_{CC} = 2\text{ V to }5.5\text{ V}$

80C51 8-bit microcontroller family
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 low power, high speed (33 MHz)

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DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

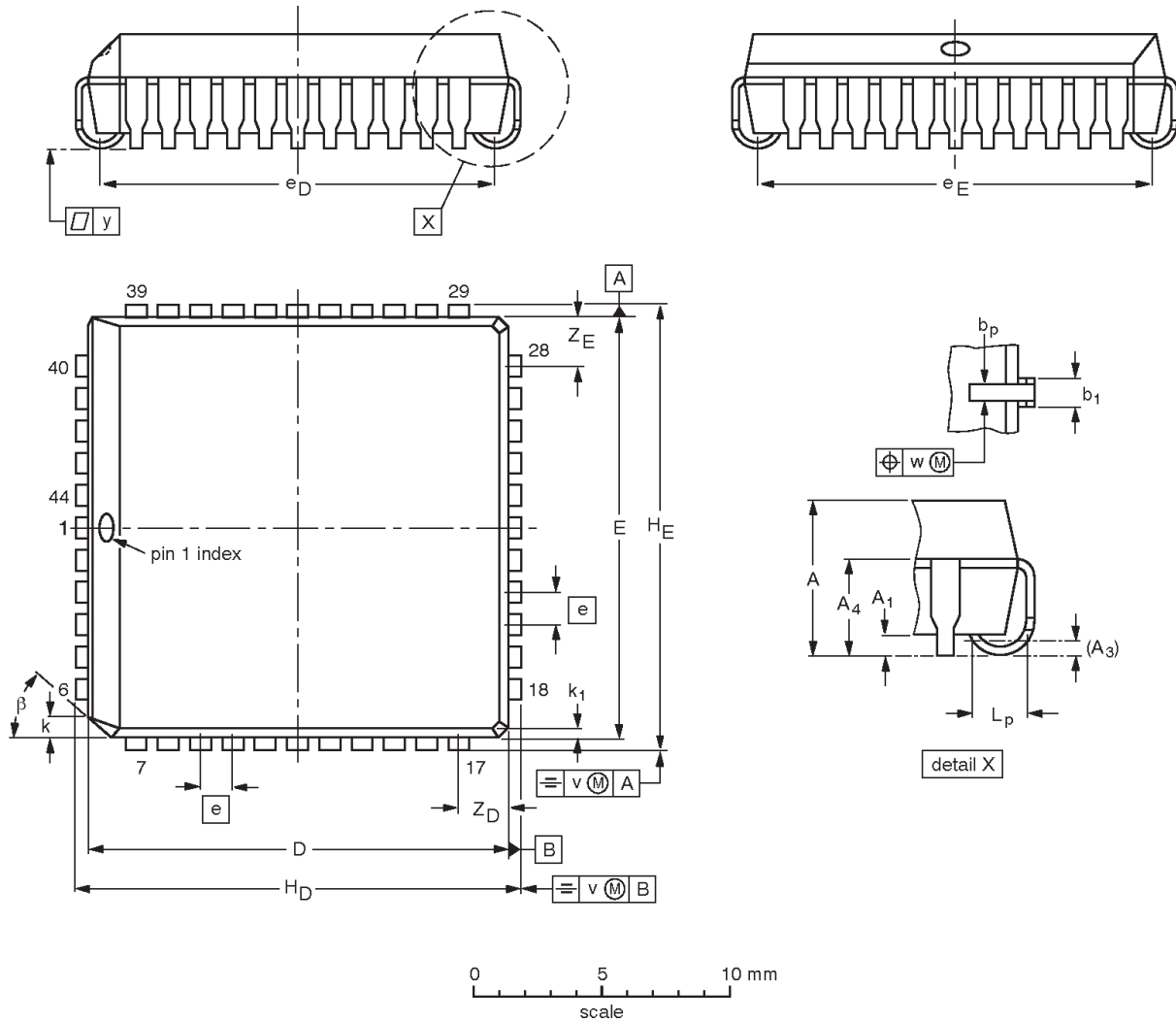
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015	SC-511-40			95-01-14 99-12-27

80C51 8-bit microcontroller family
 128/256 byte RAM ROMless low voltage (2.7V–5.5V),
 low power, high speed (33 MHz)

80C31/80C32

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	k ₁ max.	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT187-2	112E10	MO-047			97-12-16 99-12-27

80C51 8-bit microcontroller family
 128/256 byte RAM ROMless low voltage (2.7V–5.5V),
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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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