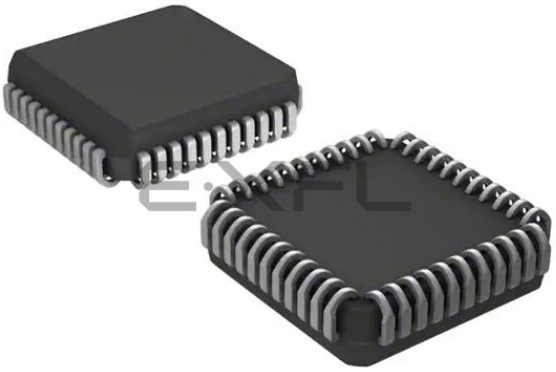
NXP USA Inc. - P80C32UFAA,512 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 33MHz |
| Connectivity | UART/USART |
| Peripherals | POR |
| Number of I/O | 32 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/p80c32ufaa-512 |

## DESCRIPTION

The Philips 80C31/32 is a high-performance static 80C51 design fabricated with Philips high-density CMOS technology with operation from 2.7 V to 5.5 V.

The 80C31/32 ROMless devices contain a 128 × 8 RAM/256 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device is a low power static design which offers a wide range of operating frequencies down to zero. Two software selectable modes of power reduction—idle mode and power-down mode are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data and then the execution resumed from the point the clock was stopped.

## SELECTION TABLE

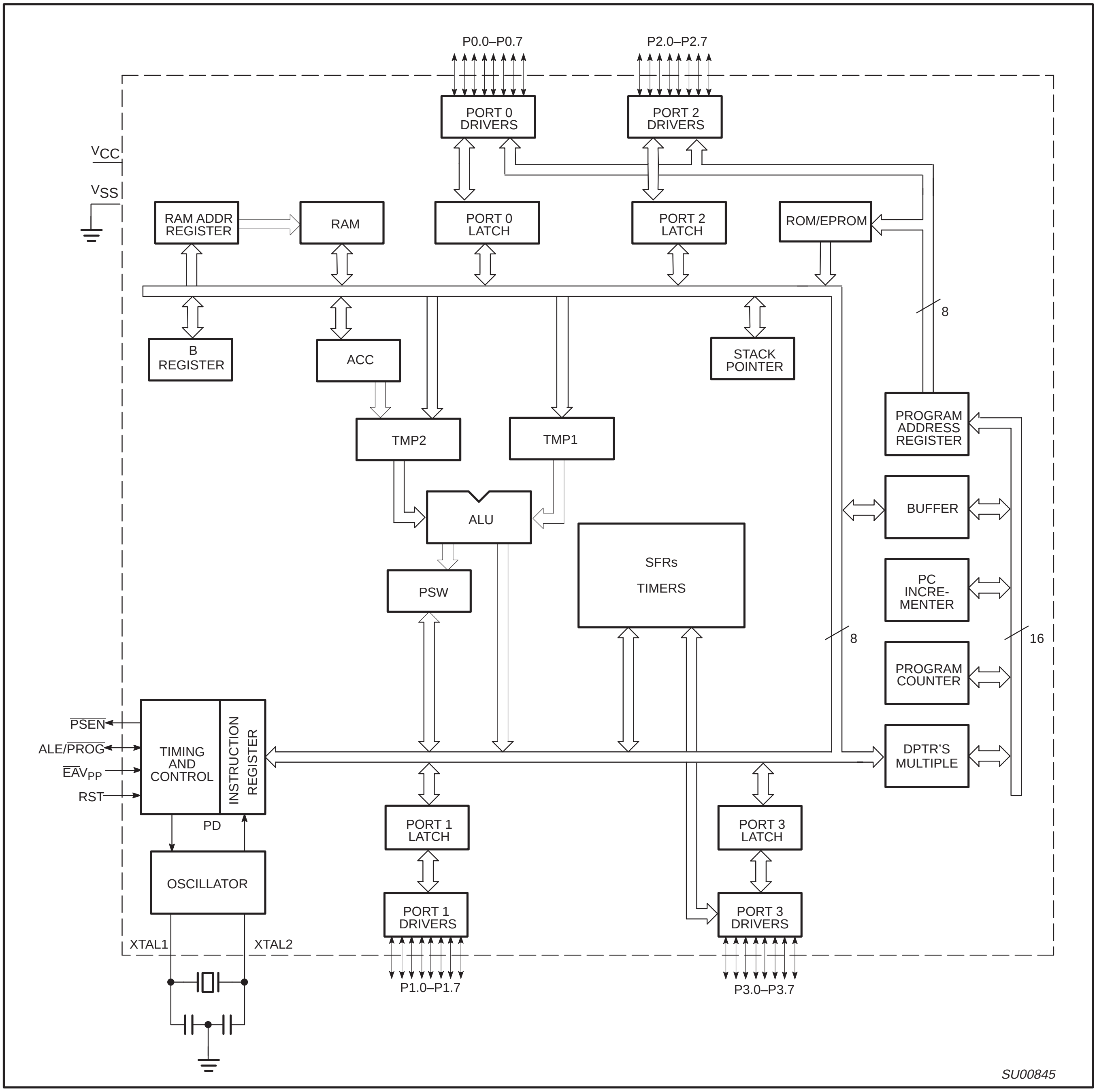
For applications requiring more ROM and RAM, see the 8XC54/58 and 8XC51RA+/RB+/RC+/80C51RA+ data sheet.

| ROM/EPROM Memory Size (X by 8) | RAM Size (X by 8) | Programmable Timer Counter (PCA) | Hardware Watch Dog Timer |
|---|---|---|---|
| **80C31/8XC51** | | | |
| 0K/4K | 128 | No | No |
| **80C32/8XC52/54/58** | | | |
| 0K/8K/16K/32K | 256 | No | No |
| **80C51RA+/8XC51RA+/RB+/RC+** | | | |
| 0K/8K/16K/32K | 512 | Yes | Yes |
| **8XC51RD+** | | | |
| 64K | 1024 | Yes | Yes |

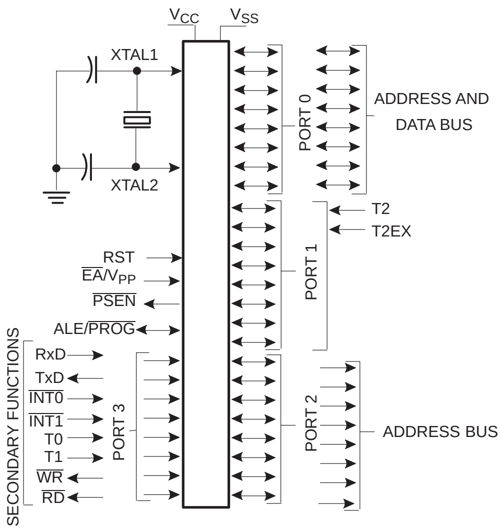
## FEATURES

- 8051 Central Processing Unit
  - 128 × 8 RAM (80C31)
  - 256 × 8 RAM (80C32)
  - Three 16-bit counter/timers
  - Boolean processor
  - Full static operation
  - Low voltage (2.7 V to 5.5 V@ 16 MHz) operation
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Clock can be stopped and resumed
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- TWO speed ranges at $V_{CC}$ = 5 V
  - 0 to 16 MHz
  - 0 to 33 MHz
- Three package styles
- Extended temperature ranges
- Dual Data Pointers
- 4 level priority interrupt
- 6 interrupt sources
- Four 8-bit I/O ports
- Full–duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Programmable clock out
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Wake-up from Power Down by an external interrupt

## BLOCK DIAGRAM



## LOGIC SYMBOL

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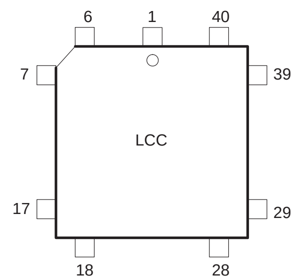
## PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

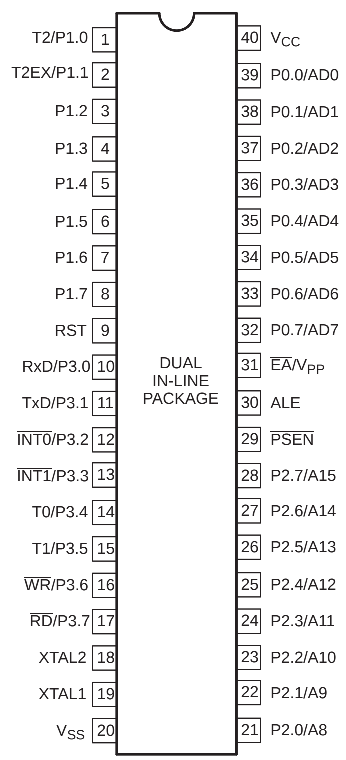



| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | NIC* | 16 | P3.4/T0 | 31 | P2.7/A15 |
| 2 | P1.0/T2 | 17 | P3.5/T1 | 32 | $\overline{PSEN}$ |
| 3 | P1.1/T2EX | 18 | P3.6/$\overline{WR}$ | 33 | ALE |
| 4 | P1.2 | 19 | P3.7/$\overline{RD}$ | 34 | NIC* |
| 5 | P1.3 | 20 | XTAL2 | 35 | $\overline{EA}/V_{PP}$ |
| 6 | P1.4 | 21 | XTAL1 | 36 | P0.7/AD7 |
| 7 | P1.5 | 22 | $V_{SS}$ | 37 | P0.6/AD6 |
| 8 | P1.6 | 23 | NIC* | 38 | P0.5/AD5 |
| 9 | P1.7 | 24 | P2.0/A8 | 39 | P0.4/AD4 |
| 10 | RST | 25 | P2.1/A9 | 40 | P0.3/AD3 |
| 11 | P3.0/RxD | 26 | P2.2/A10 | 41 | P0.2/AD2 |
| 12 | NIC* | 27 | P2.3/A11 | 42 | P0.1/AD1 |
| 13 | P3.1/TxD | 28 | P2.4/A12 | 43 | P0.0/AD0 |
| 14 | P3.2/$\overline{INT0}$ | 29 | P2.5/A13 | 44 | $V_{CC}$ |
| 15 | P3.3/$\overline{INT1}$ | 30 | P2.6/A14 | | |

* NO INTERNAL CONNECTION

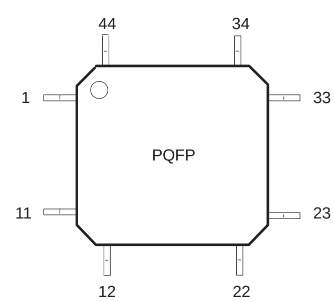
SU01062

## PIN CONFIGURATIONS




SU01063

## PLASTIC QUAD FLAT PACK PIN FUNCTIONS




| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | P1.5 | 16 | $V_{SS}$ | 31 | P0.6/AD6 |
| 2 | P1.6 | 17 | NIC* | 32 | P0.5/AD5 |
| 3 | P1.7 | 18 | P2.0/A8 | 33 | P0.4/AD4 |
| 4 | RST | 19 | P2.1/A9 | 34 | P0.3/AD3 |
| 5 | P3.0/RxD | 20 | P2.2/A10 | 35 | P0.2/AD2 |
| 6 | NIC* | 21 | P2.3/A11 | 36 | P0.1/AD1 |
| 7 | P3.1/TxD | 22 | P2.4/A12 | 37 | P0.0/AD0 |
| 8 | P3.2/$\overline{INT0}$ | 23 | P2.5/A13 | 38 | $V_{CC}$ |
| 9 | P3.3/$\overline{INT1}$ | 24 | P2.6/A14 | 39 | NIC* |
| 10 | P3.4/T0 | 25 | P2.7/A15 | 40 | P1.0/T2 |
| 11 | P3.5/T1 | 26 | $\overline{PSEN}$ | 41 | P1.1/T2EX |
| 12 | P3.6/$\overline{WR}$ | 27 | ALE | 42 | P1.2 |
| 13 | P3.7/$\overline{RD}$ | 28 | NIC* | 43 | P1.3 |
| 14 | XTAL2 | 29 | $\overline{EA}/V_{PP}$ | 44 | P1.4 |
| 15 | XTAL1 | 30 | P0.7/AD7 | | |

* NO INTERNAL CONNECTION

SU01064

**Table 1. 8XC51/80C31 Special Function Registers**

| SYMBOL | DESCRIPTION | DIRECT ADDRESS | BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB | | | | | | | LSB | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ACC* | Accumulator | E0H | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 | 00H |
| AUXR# | Auxiliary | 8EH | – | – | – | – | – | – | – | AO | xxxxxxx0B |
| AUXR1# | Auxiliary 1 | A2H | – | – | – | – | WUPD[2] | 0 | – | DPS | xxx000x0B |
| B* | B register | F0H | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | 00H |
| DPTR: | Data Pointer (2 bytes) | | | | | | | | | | |
| DPH | Data Pointer High | 83H | | | | | | | | | 00H |
| DPL | Data Pointer Low | 82H | | | | | | | | | 00H |
| | | | AF | AE | AD | AC | AB | AA | A9 | A8 | |
| IE* | Interrupt Enable | A8H | EA | – | ET2 | ES | ET1 | EX1 | ET0 | EX0 | 0x000000B |
| | | | BF | BE | BD | BC | BB | BA | B9 | B8 | |
| IP* | Interrupt Priority | B8H | – | – | PT2 | PS | PT1 | PX1 | PT0 | PX0 | xx000000B |
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| IPH# | Interrupt Priority High | B7H | – | – | PT2H | PSH | PT1H | PX1H | PT0H | PX0H | xx000000B |
| | | | 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 | |
| P0* | Port 0 | 80H | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FFH |
| | | | 97 | 96 | 95 | 94 | 93 | 92 | 91 | 90 | |
| P1* | Port 1 | 90H | – | – | – | – | – | – | T2EX | T2 | FFH |
| | | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| P2* | Port 2 | A0H | AD15 | AD14 | AD13 | AD12 | AD11 | AD10 | AD9 | AD8 | FFH |
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| P3* | Port 3 | B0H | $\overline{RD}$ | $\overline{WR}$ | T1 | T0 | $\overline{INT1}$ | $\overline{INT0}$ | TxD | RxD | FFH |
| PCON#[1] | Power Control | 87H | SMOD1 | SMOD0 | – | POF | GF1 | GF0 | PD | IDL | 00xx0000B |
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PSW* | Program Status Word | D0H | CY | AC | F0 | RS1 | RS0 | OV | – | P | 000000x0B |
| RACAP2H# | Timer 2 Capture High | CBH | | | | | | | | | 00H |
| RACAP2L# | Timer 2 Capture Low | CAH | | | | | | | | | 00H |
| SADDR# | Slave Address | A9H | | | | | | | | | 00H |
| SADEN# | Slave Address Mask | B9H | | | | | | | | | 00H |
| SBUF | Serial Data Buffer | 99H | | | | | | | | | xxxxxxxxB |
| | | | 9F | 9E | 9D | 9C | 9B | 9A | 99 | 98 | |
| SCON* | Serial Control | 98H | SM0/FE | SM1 | SM2 | REN | TB8 | RB8 | TI | RI | 00H |
| SP | Stack Pointer | 81H | | | | | | | | | 07H |
| | | | 8F | 8E | 8D | 8C | 8B | 8A | 89 | 88 | |
| TCON* | Timer Control | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00H |
| | | | CF | CE | CD | CC | CB | CA | C9 | C8 | |
| T2CON* | Timer 2 Control | C8H | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/$\overline{T2}$ | CP/$\overline{RL2}$ | 00H |
| T2MOD# | Timer 2 Mode Control | C9H | – | – | – | – | – | – | T2OE | DCEN | xxxxxx00B |
| TH0 | Timer High 0 | 8CH | | | | | | | | | 00H |
| TH1 | Timer High 1 | 8DH | | | | | | | | | 00H |
| TH2# | Timer High 2 | CDH | | | | | | | | | 00H |
| TL0 | Timer Low 0 | 8AH | | | | | | | | | 00H |
| TL1 | Timer Low 1 | 8BH | | | | | | | | | 00H |
| TL2# | Timer Low 2 | CCH | | | | | | | | | 00H |
| TMOD | Timer Mode | 89H | GATE | C/$\overline{T}$ | M1 | M0 | GATE | C/$\overline{T}$ | M1 | M0 | 00H |

**NOTE:**
Unused register bits that are not defined should not be set by the user's program. If violated, the device could function incorrectly.
* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.
1. Reset value depends on reset source.
2. Not available on 80C31.

## Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

Where:

(RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

## TIMER 2 OPERATION

### Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/$\overline{\text{T}}$2* in the special function register T2CON (see Figure 1). Timer 2 has three operating modes:Capture, Auto-reload (up or down counting) ,and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

### Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/T2* in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt. The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/12 pulses.).

### Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter (C/T2* in T2CON)) then programmed to count up or down. The counting direction is determined by bit DCEN (Down Counter Enable) which is located in the T2MOD register (see Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16–bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

**Table 3. Timer 2 Operating Modes**

| RCLK + TCLK | CP/$\overline{\text{RL2}}$ | TR2 | MODE |
|---|---|---|---|
| 0 | 0 | 1 | 16-bit Auto-reload |
| 0 | 1 | 1 | 16-bit Capture |
| 1 | X | 1 | Baud rate generator |
| X | X | 0 | (off) |

**T2MOD** Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | T2OE | DCEN |

| Symbol | Function |
|---|---|
| — | Not implemented, reserved for future use.* |
| T2OE | Timer 2 Output Enable bit. |
| DCEN | Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter. |

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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**Figure 3. Timer 2 Mode (T2MOD) Control Register**

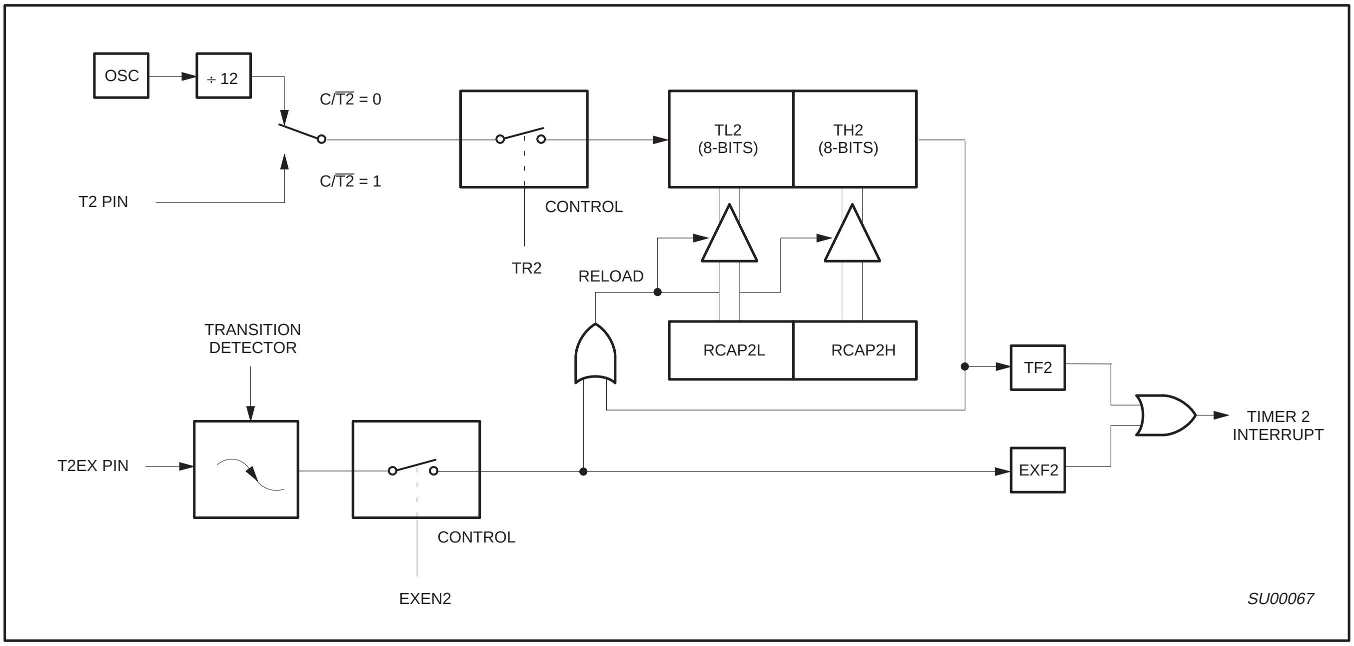


**Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)**

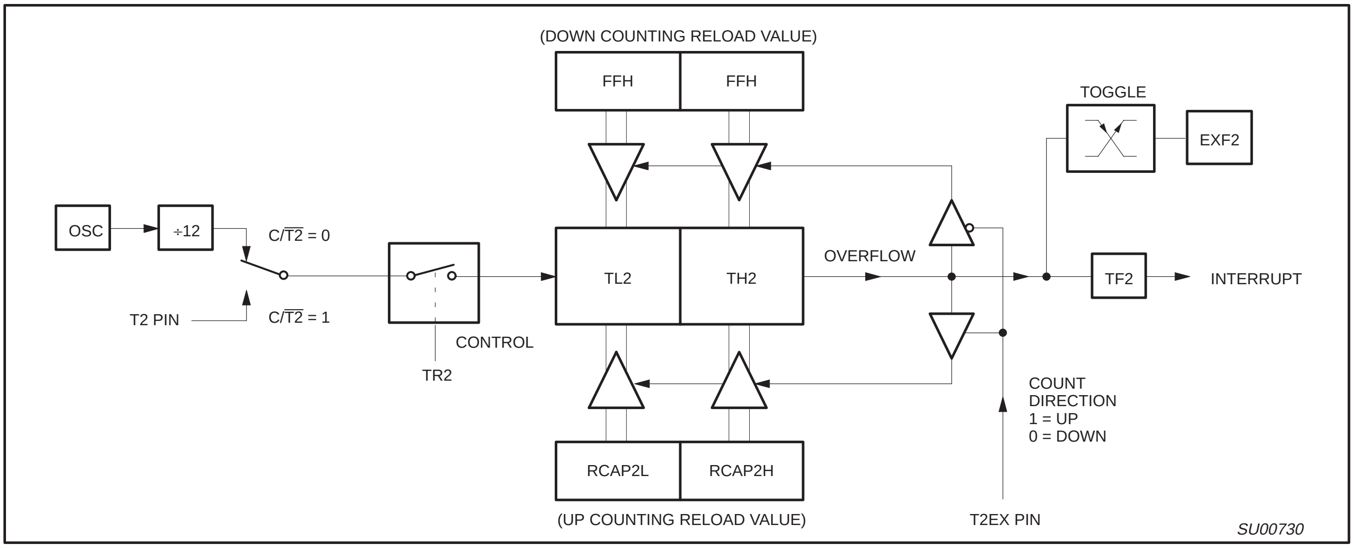


**Figure 5. Timer 2 Auto Reload Mode (DCEN = 1)**

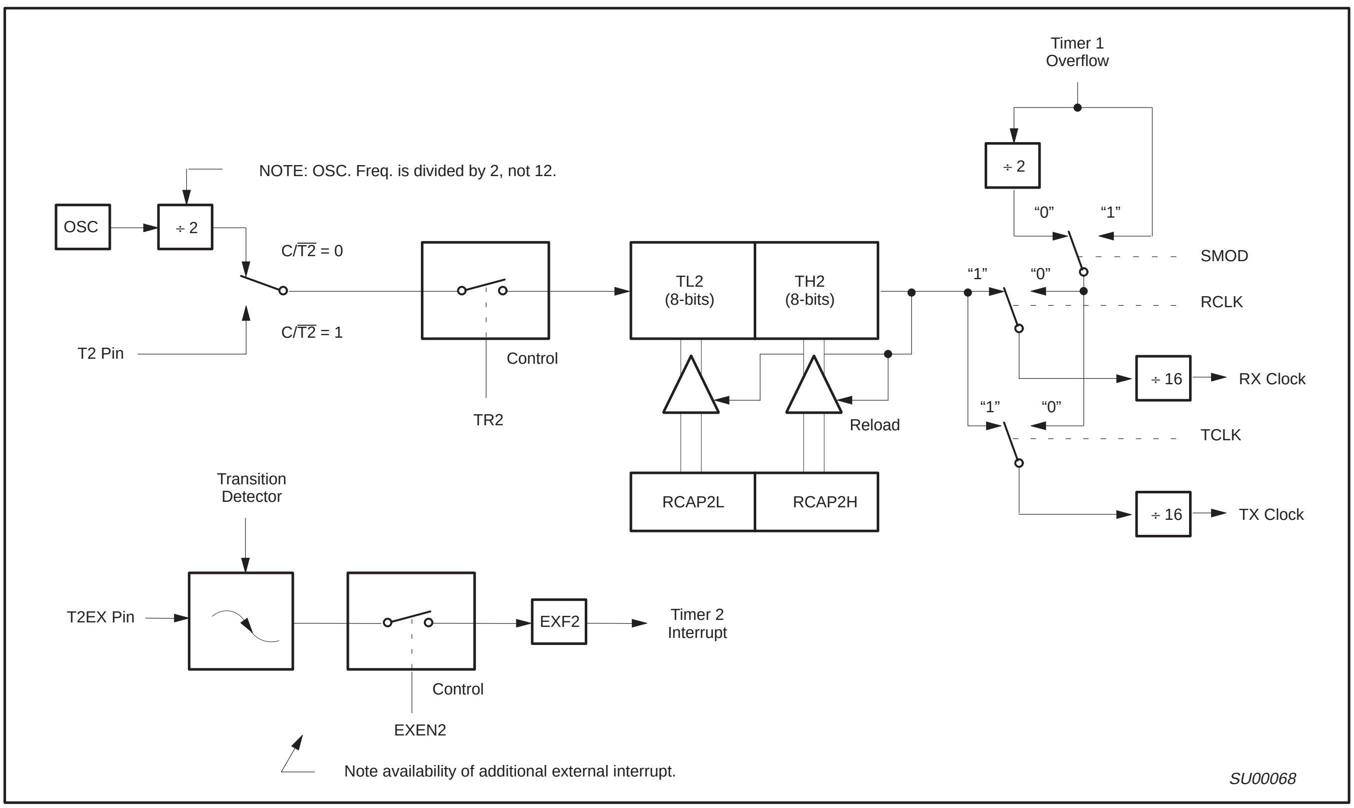


**Figure 6. Timer 2 in Baud Rate Generator Mode**

## Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 3) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 6 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation ($C/\overline{T}2$*=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/12 the oscillator frequency). As a baud rate generator, it increments every state time (i.e., 1/2 the oscillator frequency). Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where: (RCAP2H, RCAP2L)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 6, is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2,TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time (osc/2) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

**Table 4. Timer 2 Generated Commonly Used Baud Rates**

| Baud Rate | Osc Freq | Timer 2 | |
|---|---|---|---|
| | | RCAP2H | RCAP2L |
| 375 K | 12 MHz | FF | FF |
| 9.6 K | 12 MHz | FF | D9 |
| 2.8 K | 12 MHz | FF | B2 |
| 2.4 K | 12 MHz | FF | 64 |
| 1.2 K | 12 MHz | FE | C8 |
| 300 | 12 MHz | FB | 1E |
| 110 | 12 MHz | F2 | AF |
| 300 | 6 MHz | FD | 8F |
| 110 | 6 MHz | F9 | 57 |

## Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{OSC}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where $f_{OSC}$= Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H}, \text{RCAP2L} = 65536 - \left(\frac{f_{OSC}}{32 \times \text{Baud Rate}}\right)$$

## Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

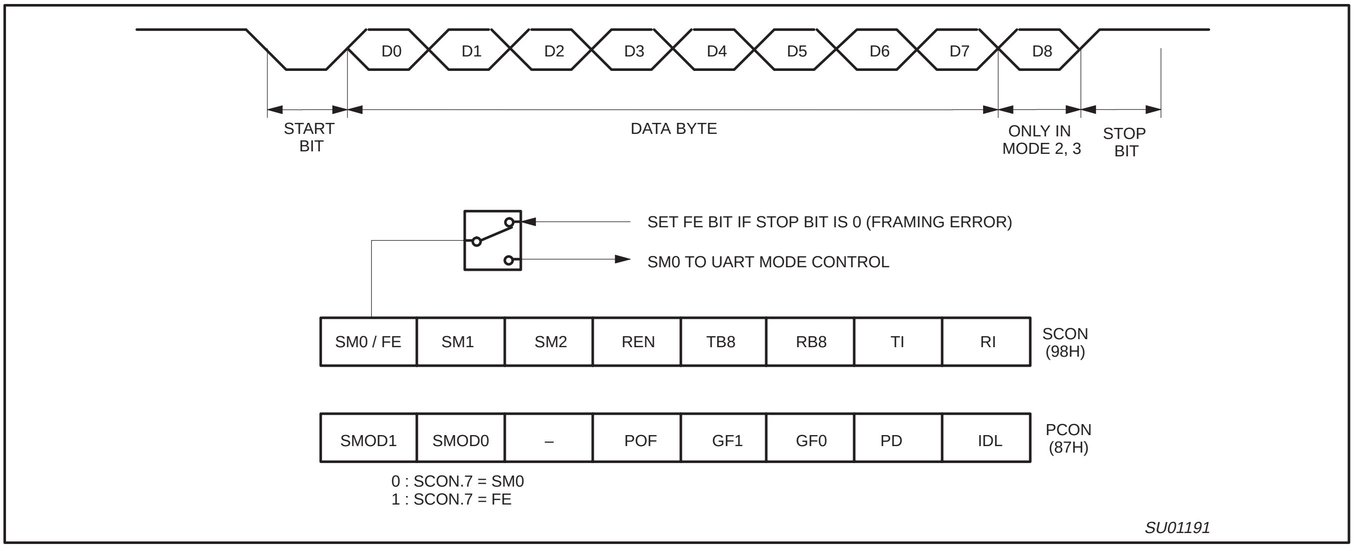


**Figure 8. UART Framing Error Detection**

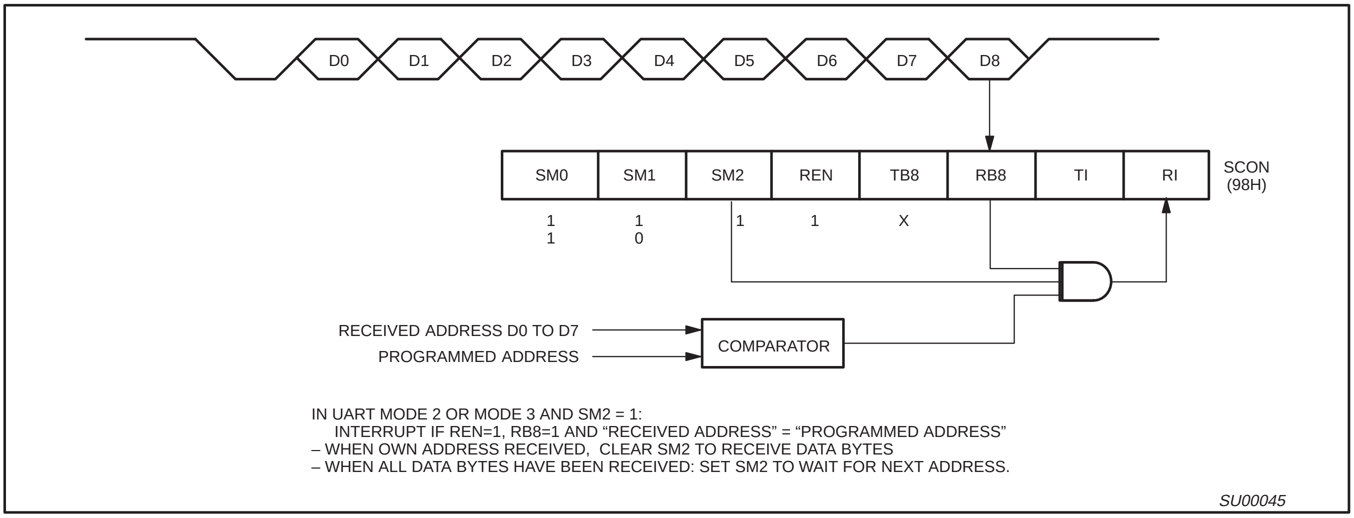


**Figure 9. UART Multiprocessor Communication, Automatic Address Recognition**

## Interrupt Priority Structure

The 80C31 and 80C32 have a 6-source four-level interrupt structure. They are the IE, IP and IPH. (See Figures 10, 11, and 12.) The IPH (Interrupt Priority High) register that makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 12.

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

| PRIORITY BITS | | INTERRUPT PRIORITY LEVEL |
|---|---|---|
| IPH.x | IP.x | |
| 0 | 0 | Level 0 (lowest priority) |
| 0 | 1 | Level 1 |
| 1 | 0 | Level 2 |
| 1 | 1 | Level 3 (highest priority) |

An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

### Table 7. Interrupt Table

| SOURCE | POLLING PRIORITY | REQUEST BITS | HARDWARE CLEAR? | VECTOR ADDRESS |
|---|---|---|---|---|
| X0 | 1 | IE0 | N (L)[1] Y (T)[2] | 03H |
| T0 | 2 | TP0 | Y | 0BH |
| X1 | 3 | IE1 | N (L) Y (T) | 13H |
| T1 | 4 | TF1 | Y | 1BH |
| SP | 5 | RI, TI | N | 23H |
| T2 | 6 | TF2, EXF2 | N | 2BH |

**NOTES:**
1. L = Level activated
2. T = Transition activated

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **IE (0A8H)** | EA | — | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| IE.7 | EA | Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit. |
| IE.6 | — | Not implemented. Reserved for future use. |
| IE.5 | ET2 | Timer 2 interrupt enable bit. |
| IE.4 | ES | Serial Port interrupt enable bit. |
| IE.3 | ET1 | Timer 1 interrupt enable bit. |
| IE.2 | EX1 | External interrupt 1 enable bit. |
| IE.1 | ET0 | Timer 0 interrupt enable bit. |
| IE.0 | EX0 | External interrupt 0 enable bit. |

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**Figure 10. IE Registers**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **IP (0B8H)** | — | — | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

Priority Bit = 1 assigns higher priority
Priority Bit = 0 assigns lower priority

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| IP.7 | — | Not implemented, reserved for future use. |
| IP.6 | — | Not implemented, reserved for future use. |
| IP.5 | PT2 | Timer 2 interrupt priority bit. |
| IP.4 | PS | Serial Port interrupt priority bit. |
| IP.3 | PT1 | Timer 1 interrupt priority bit. |
| IP.2 | PX1 | External interrupt 1 priority bit. |
| IP.1 | PT0 | Timer 0 interrupt priority bit. |
| IP.0 | PX0 | External interrupt 0 priority bit. |

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**Figure 11. IP Registers**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **IPH (B7H)** | — | — | PT2H | PSH | PT1H | PX1H | PT0H | PX0H |

Priority Bit = 1 assigns higher priority
Priority Bit = 0 assigns lower priority

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| IPH.7 | — | Not implemented, reserved for future use. |
| IPH.6 | — | Not implemented, reserved for future use. |
| IPH.5 | PT2H | Timer 2 interrupt priority bit high. |
| IPH.4 | PSH | Serial Port interrupt priority bit high. |
| IPH.3 | PT1H | Timer 1 interrupt priority bit high. |
| IPH.2 | PX1H | External interrupt 1 priority bit high. |
| IPH.1 | PT0H | Timer 0 interrupt priority bit high. |
| IPH.0 | PX0H | External interrupt 0 priority bit high. |

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**Figure 12. IPH Registers**

## ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

| PARAMETER | RATING | UNIT |
|---|---|---|
| Operating temperature under bias | 0 to +70 or –40 to +85 | °C |
| Storage temperature range | –65 to +150 | °C |
| Voltage on $\overline{EA}$ pin to $V_{SS}$ | 0 to +13.0 | V |
| Voltage on any other pin to $V_{SS}$ | –0.5 to +6.5 | V |
| Maximum $I_{OL}$ per I/O pin | 15 | mA |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1.5 | W |

**NOTES:**
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

## AC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0°C to +70°C or –40°C to +85°C

| SYMBOL | FIGURE | PARAMETER | CLOCK FREQUENCY RANGE –f | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $1/t_{CLCL}$ | 29 | Oscillator frequency<br>Speed versions : S (16 MHz)<br>U (33 MHz) | <br>0<br>0 | <br>16<br>33 | <br>MHz<br>MHz |

## DC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0°C to +70°C or –40°C to +85°C, $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V (16 MHz devices)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | |
| $V_{IL}$ | Input low voltage | 4.0 V < $V_{CC}$ < 5.5 V | –0.5 | | 0.2 $V_{CC}$–0.1 | V |
| | | 2.7 V<$V_{CC}$< 4.0 V | –0.5 | | 0.7 | V |
| $V_{IH}$ | Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$) | | 0.2 $V_{CC}$+0.9 | | $V_{CC}$+0.5 | V |
| $V_{IH1}$ | Input high voltage, XTAL1, RST | | 0.7 $V_{CC}$ | | $V_{CC}$+0.5 | V |
| $V_{OL}$ | Output low voltage, ports 1, 2, [8] | $V_{CC}$ = 2.7 V<br>$I_{OL}$ = 1.6 mA[2] | | | 0.4 | V |
| $V_{OL1}$ | Output low voltage, port 0, ALE, $\overline{PSEN}$[8, 7] | $V_{CC}$ = 2.7 V<br>$I_{OL}$ = 3.2 mA[2] | | | 0.4 | V |
| $V_{OH}$ | Output high voltage, ports 1, 2, 3 [3] | $V_{CC}$ = 2.7 V<br>$I_{OH}$ = –20 µA | $V_{CC}$ – 0.7 | | | V |
| | | $V_{CC}$ = 4.5 V<br>$I_{OH}$ = –30 µA | $V_{CC}$ – 0.7 | | | V |
| $V_{OH1}$ | Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3] | $V_{CC}$ = 2.7 V<br>$I_{OH}$ = –3.2 mA | $V_{CC}$ – 0.7 | | | V |
| $I_{IL}$ | Logical 0 input current, ports 1, 2, 3 | $V_{IN}$ = 0.4 V | –1 | | –50 | µA |
| $I_{TL}$ | Logical 1-to-0 transition current, ports 1, 2, 3[6] | $V_{IN}$ = 2.0 V<br>See note 4 | | | –650 | µA |
| $I_{LI}$ | Input leakage current, port 0 | 0.45 < $V_{IN}$ < $V_{CC}$ – 0.3 | | | ±10 | µA |
| $I_{CC}$ | Power supply current (see Figure 21): | See note 5 | | | | |
| | Active mode @ 16 MHz | | | | | µA |
| | Idle mode @ 16 MHz | | | | | µA |
| | Power-down mode or clock stopped (see Figure 25 for conditions) | $T_{amb}$ = 0°C to 70°C | | 3 | 50 | µA |
| | | $T_{amb}$ = –40°C to +85°C | | | 75 | µA |
| $R_{RST}$ | Internal reset pull-down resistor | | 40 | | 225 | kΩ |
| $C_{IO}$ | Pin capacitance[10] (except $\overline{EA}$) | | | | 15 | pF |

**NOTES:**

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the $V_{OL}$s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. $I_{OL}$ can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall below the $V_{CC}$–0.7 specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when $V_{IN}$ is approximately 2 V.
5. See Figures 22 through 25 for $I_{CC}$ test conditions.
   Active mode: $I_{CC}$ = 0.9 × FREQ. + 1.1 mA
   Idle mode: $I_{CC}$ = 0.18 × FREQ. +1.01 mA; See Figure 21.
6. This value applies to $T_{amb}$ = 0°C to +70°C. For $T_{amb}$ = –40°C to +85°C, $I_{TL}$ = –750 µA.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
8. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 15 mA (*NOTE: This is 85°C specification.)
   Maximum $I_{OL}$ per 8-bit port: 26 mA
   Maximum total $I_{OL}$ for all outputs: 71 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to $V_{OH1}$, except when ALE is off then $V_{OH}$ is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF.

## AC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0°C to +70°C or –40°C to +85°C, $V_{CC}$ = 5 V ±10%, $V_{SS}$ = 0 V[1, 2, 3]

| SYMBOL | FIGURE | PARAMETER | VARIABLE CLOCK[4] 16 MHz to $f_{max}$ | | 33 MHz CLOCK | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{LHLL}$ | 14 | ALE pulse width | $2t_{CLCL}$–40 | | 21 | | ns |
| $t_{AVLL}$ | 14 | Address valid to ALE low | $t_{CLCL}$–25 | | 5 | | ns |
| $t_{LLAX}$ | 14 | Address hold after ALE low | $t_{CLCL}$–25 | | | | ns |
| $t_{LLIV}$ | 14 | ALE low to valid instruction in | | $4t_{CLCL}$–65 | | 55 | ns |
| $t_{LLPL}$ | 14 | ALE low to $\overline{PSEN}$ low | $t_{CLCL}$–25 | | 5 | | ns |
| $t_{PLPH}$ | 14 | $\overline{PSEN}$ pulse width | $3t_{CLCL}$–45 | | 45 | | ns |
| $t_{PLIV}$ | 14 | $\overline{PSEN}$ low to valid instruction in | | $3t_{CLCL}$–60 | | 30 | ns |
| $t_{PXIX}$ | 14 | Input instruction hold after $\overline{PSEN}$ | 0 | | 0 | | ns |
| $t_{PXIZ}$ | 14 | Input instruction float after $\overline{PSEN}$ | | $t_{CLCL}$–25 | | 5 | ns |
| $t_{AVIV}$ | 14 | Address to valid instruction in | | $5t_{CLCL}$–80 | | 70 | ns |
| $t_{PLAZ}$ | 14 | $\overline{PSEN}$ low to address float | | 10 | | 10 | ns |
| **Data Memory** | | | | | | | |
| $t_{RLRH}$ | 15, 16 | $\overline{RD}$ pulse width | $6t_{CLCL}$–100 | | 82 | | ns |
| $t_{WLWH}$ | 15, 16 | $\overline{WR}$ pulse width | $6t_{CLCL}$–100 | | 82 | | ns |
| $t_{RLDV}$ | 15, 16 | $\overline{RD}$ low to valid data in | | $5t_{CLCL}$–90 | | 60 | ns |
| $t_{RHDX}$ | 15, 16 | Data hold after $\overline{RD}$ | 0 | | 0 | | ns |
| $t_{RHDZ}$ | 15, 16 | Data float after $\overline{RD}$ | | $2t_{CLCL}$–28 | | 32 | ns |
| $t_{LLDV}$ | 15, 16 | ALE low to valid data in | | $8t_{CLCL}$–150 | | 90 | ns |
| $t_{AVDV}$ | 15, 16 | Address to valid data in | | $9t_{CLCL}$–165 | | 105 | ns |
| $t_{LLWL}$ | 15, 16 | ALE low to $\overline{RD}$ or $\overline{WR}$ low | $3t_{CLCL}$–50 | $3t_{CLCL}$+50 | 40 | 140 | ns |
| $t_{AVWL}$ | 15, 16 | Address valid to $\overline{WR}$ low or $\overline{RD}$ low | $4t_{CLCL}$–75 | | 45 | | ns |
| $t_{QVWX}$ | 15, 16 | Data valid to $\overline{WR}$ transition | $t_{CLCL}$–30 | | 0 | | ns |
| $t_{WHQX}$ | 15, 16 | Data hold after $\overline{WR}$ | $t_{CLCL}$–25 | | 5 | | ns |
| $t_{QVWH}$ | 16 | Data valid to $\overline{WR}$ high | $7t_{CLCL}$–130 | | 80 | | ns |
| $t_{RLAZ}$ | 15, 16 | $\overline{RD}$ low to address float | | 0 | | 0 | ns |
| $t_{WHLH}$ | 15, 16 | $\overline{RD}$ or $\overline{WR}$ high to ALE high | $t_{CLCL}$–25 | $t_{CLCL}$+25 | 5 | 55 | ns |
| **External Clock** | | | | | | | |
| $t_{CHCX}$ | 18 | High time | $0.38t_{CLCL}$ | $t_{CLCL}$–$t_{CLCX}$ | | | ns |
| $t_{CLCX}$ | 18 | Low time | $0.38t_{CLCL}$ | $t_{CLCL}$–$t_{CHCX}$ | | | ns |
| $t_{CLCH}$ | 18 | Rise time | | 5 | | | ns |
| $t_{CHCL}$ | 18 | Fall time | | 5 | | | ns |
| **Shift Register** | | | | | | | |
| $t_{XLXL}$ | 17 | Serial port clock cycle time | $12t_{CLCL}$ | | 360 | | ns |
| $t_{QVXH}$ | 17 | Output data setup to clock rising edge | $10t_{CLCL}$–133 | | 167 | | ns |
| $t_{XHQX}$ | 17 | Output data hold after clock rising edge | $2t_{CLCL}$–80 | | | | ns |
| $t_{XHDX}$ | 17 | Input data hold after clock rising edge | 0 | | 0 | | ns |
| $t_{XHDV}$ | 17 | Clock rising edge to input data valid | | $10t_{CLCL}$–133 | | 167 | ns |

**NOTES:**
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
3. Interfacing the 80C31 and 80C32 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Variable clock is specified for oscillator frequencies greater than 16 MHz to 33 MHz. For frequencies equal or less than 16 MHz, see 16 MHz “AC Electrical Characteristics”, page 23.
5. Parts are guaranteed to operate down to 0 Hz. When an external clock source is used, the RST pin should be held high for a minimum of 20 µs for power-on or wakeup from power down.

## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

**Examples:** $t_{AVLL}$ = Time for address valid to ALE low.
$t_{LLPL}$ =Time for ALE low to $\overline{PSEN}$ low.

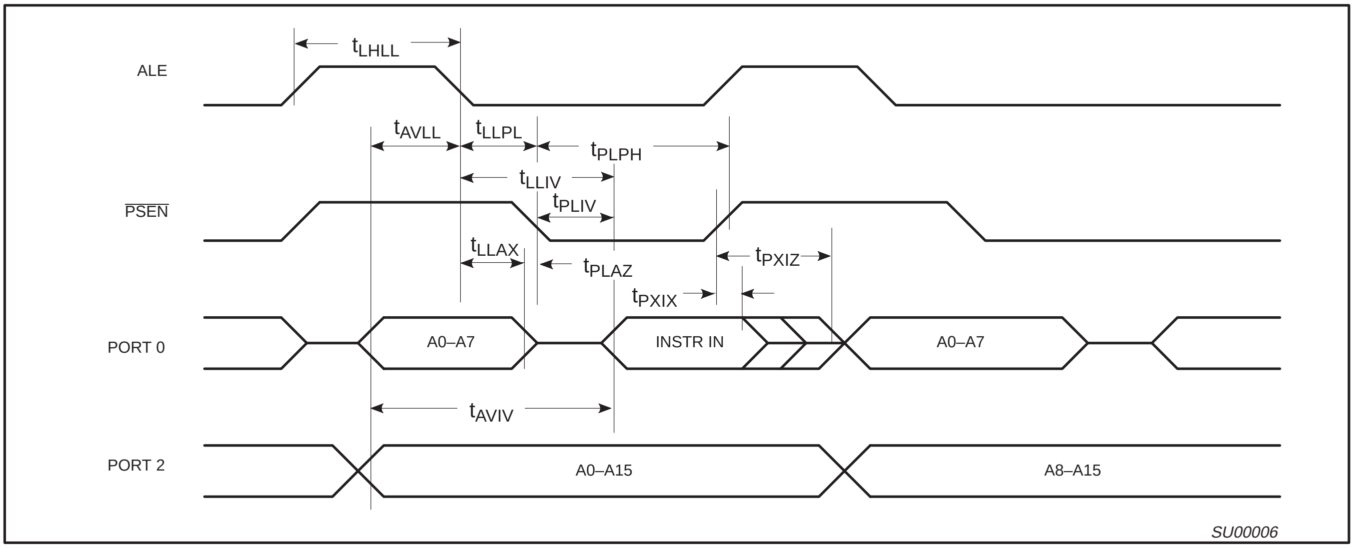



**Figure 14. External Program Memory Read Cycle**

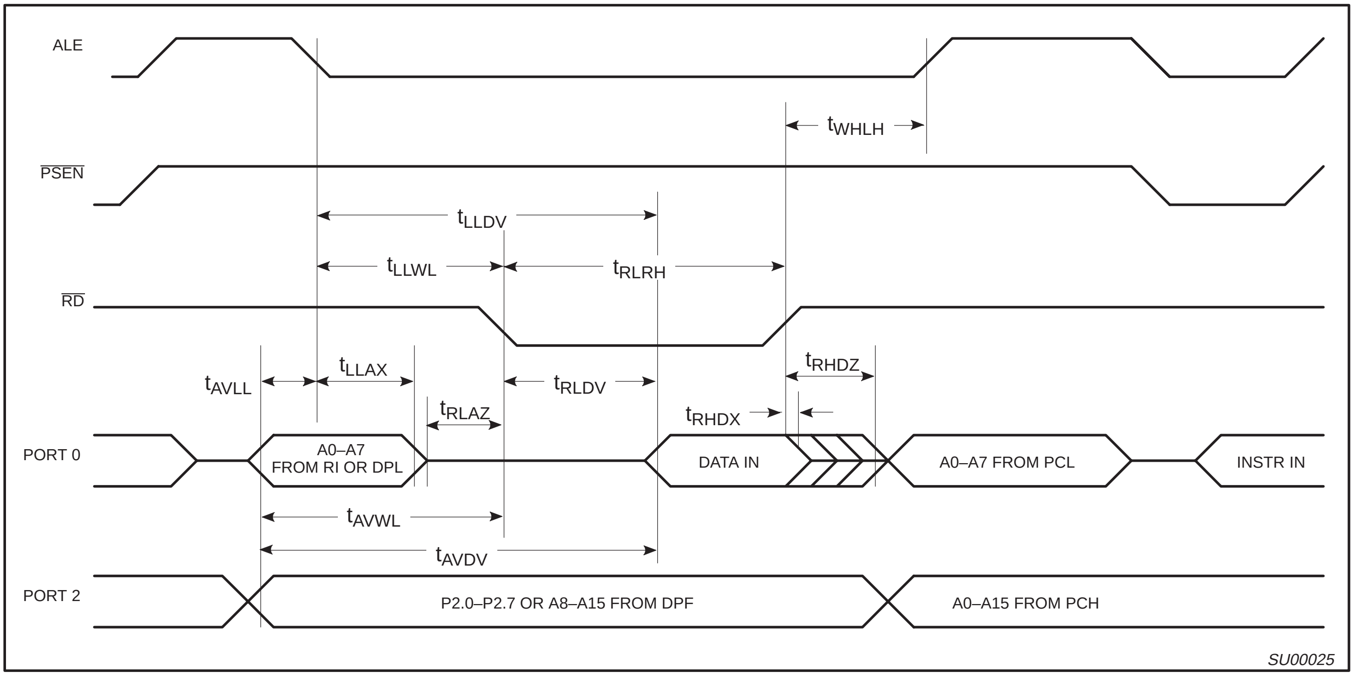



**Figure 15. External Data Memory Read Cycle**

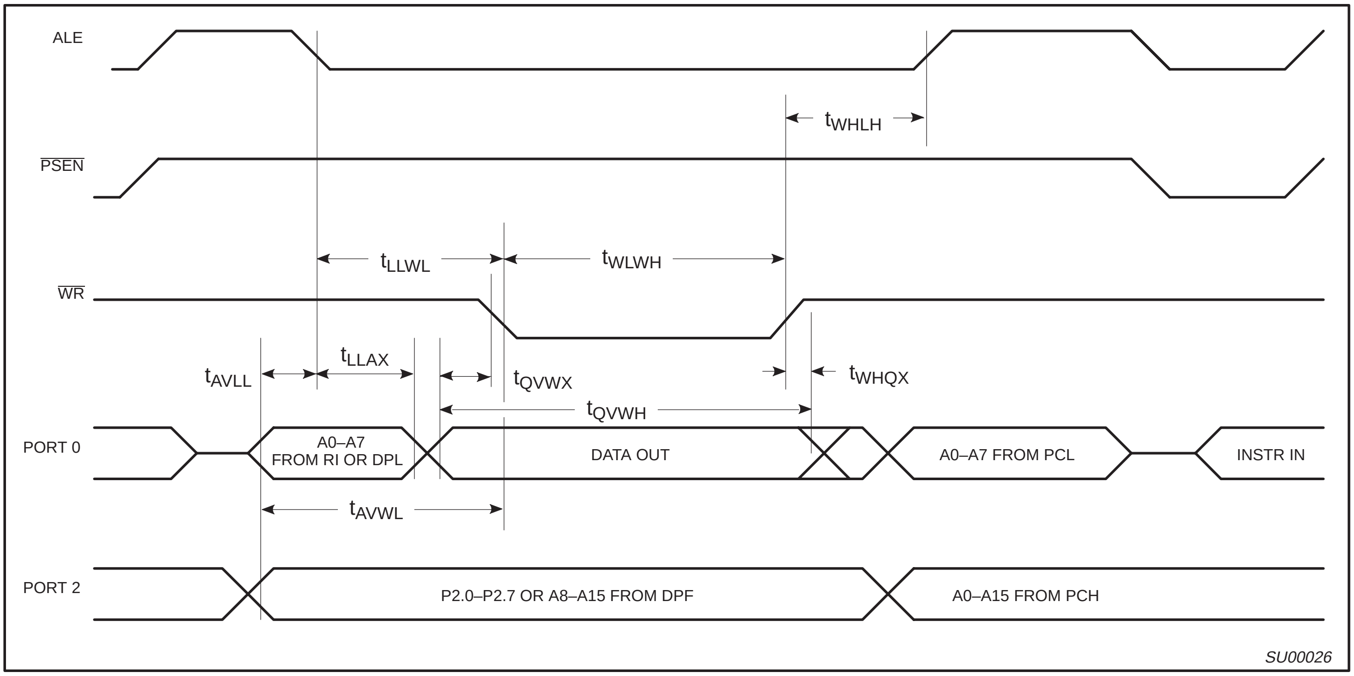



**Figure 16. External Data Memory Write Cycle**

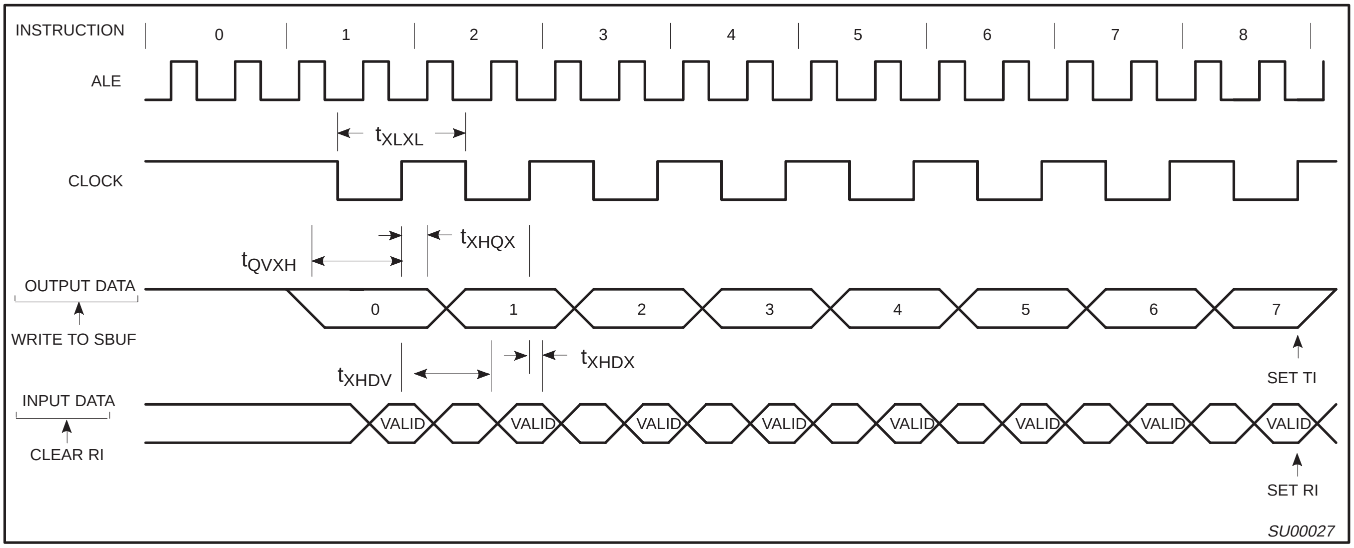



**Figure 17. Shift Register Mode Timing**

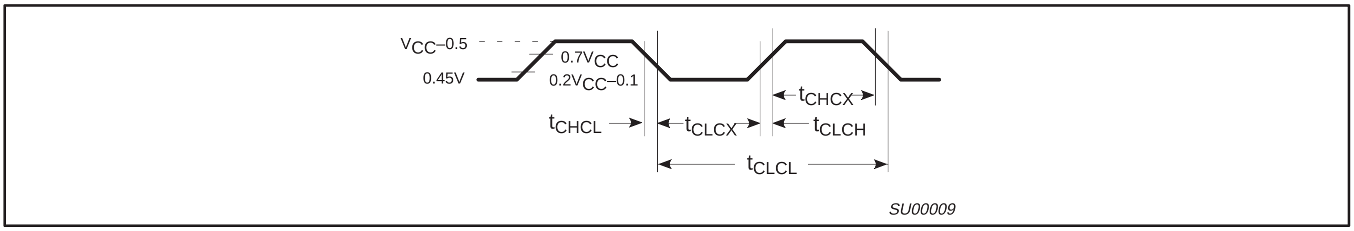



**Figure 18. External Clock Drive**

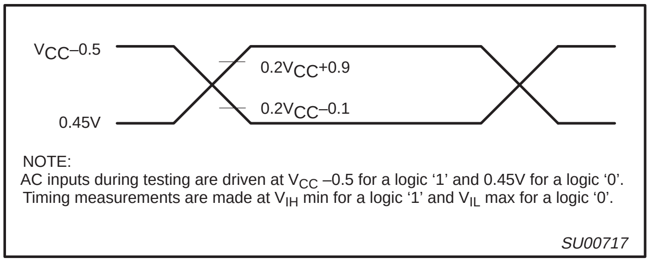



**Figure 19. AC Testing Input/Output**

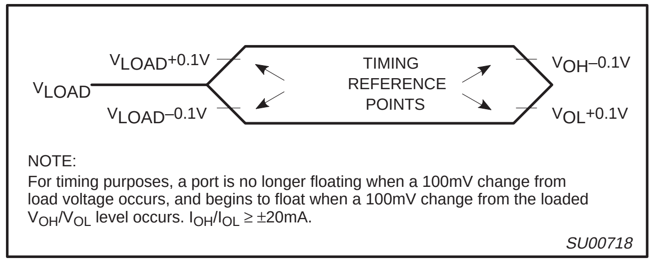



**Figure 20. Float Waveform**

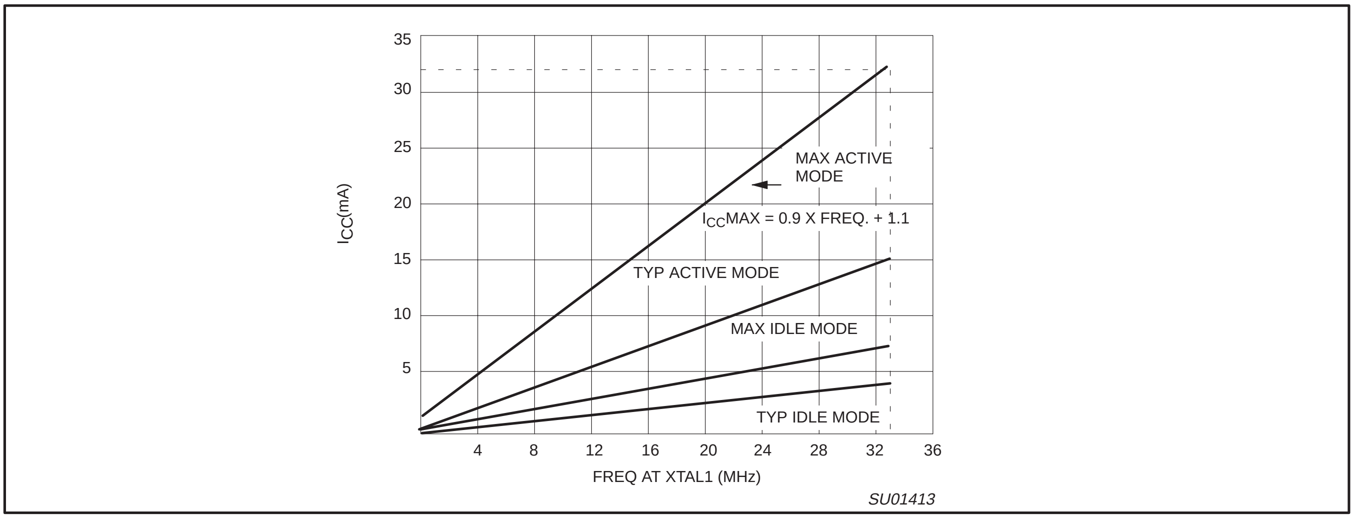



**Figure 21. $I_{CC}$ vs. FREQ**
**Valid only within frequency specifications of the device under test**

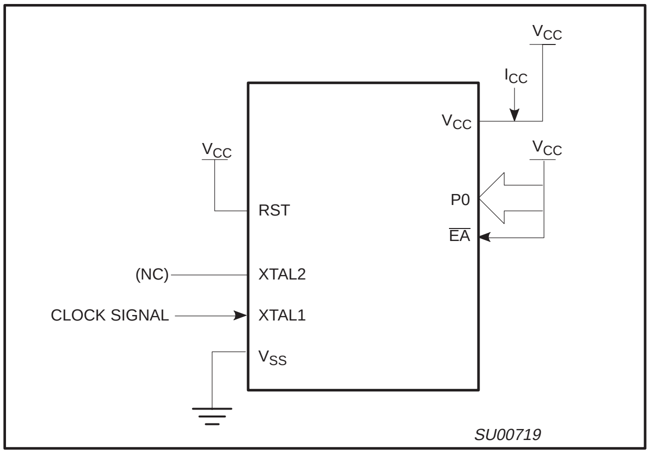



**Figure 22. $I_{CC}$ Test Condition, Active Mode**
**All other pins are disconnected**

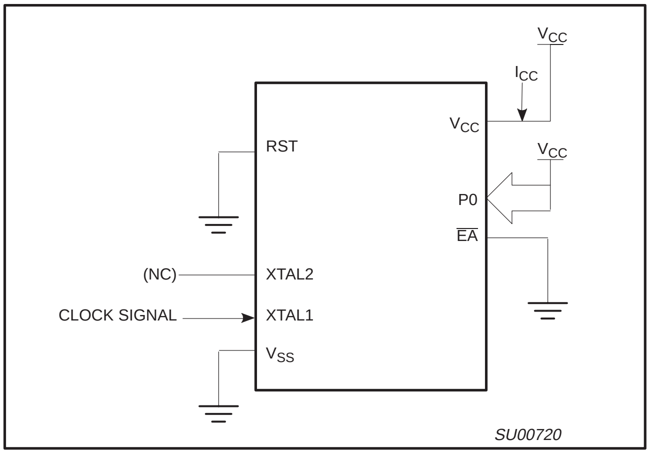



**Figure 23. $I_{CC}$ Test Condition, Idle Mode**
**All other pins are disconnected**

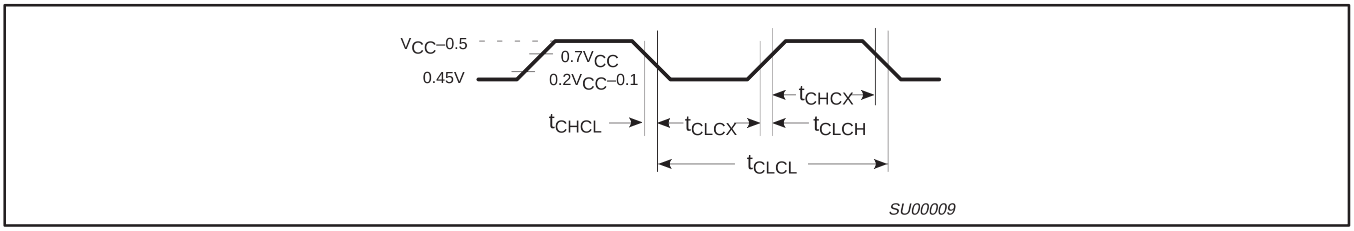



**Figure 24. Clock Signal Waveform for $I_{CC}$ Tests in Active and Idle Modes**
**$t_{CLCH} = t_{CHCL}$ = 5ns**

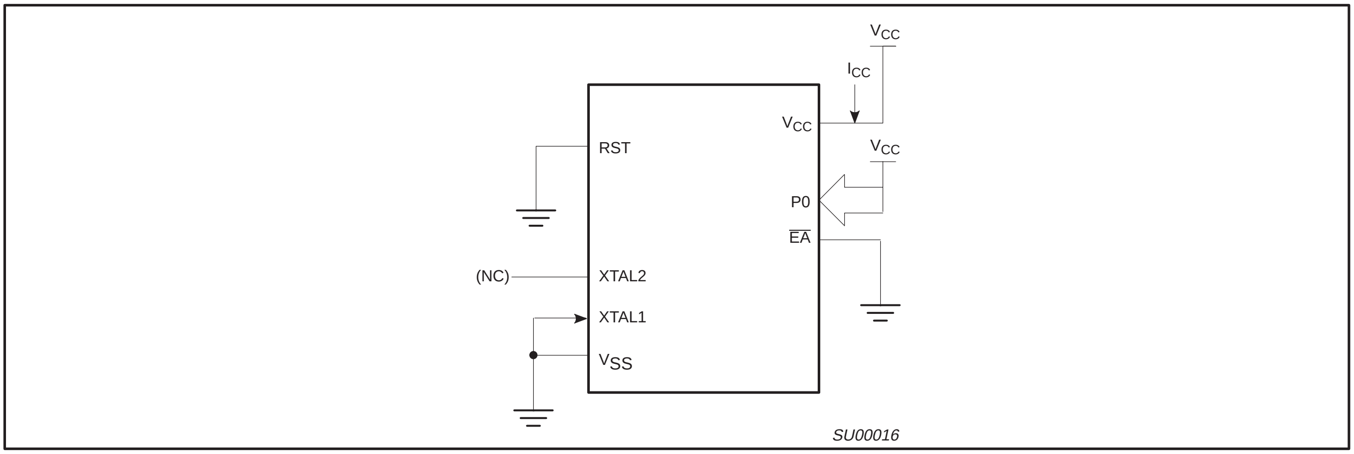
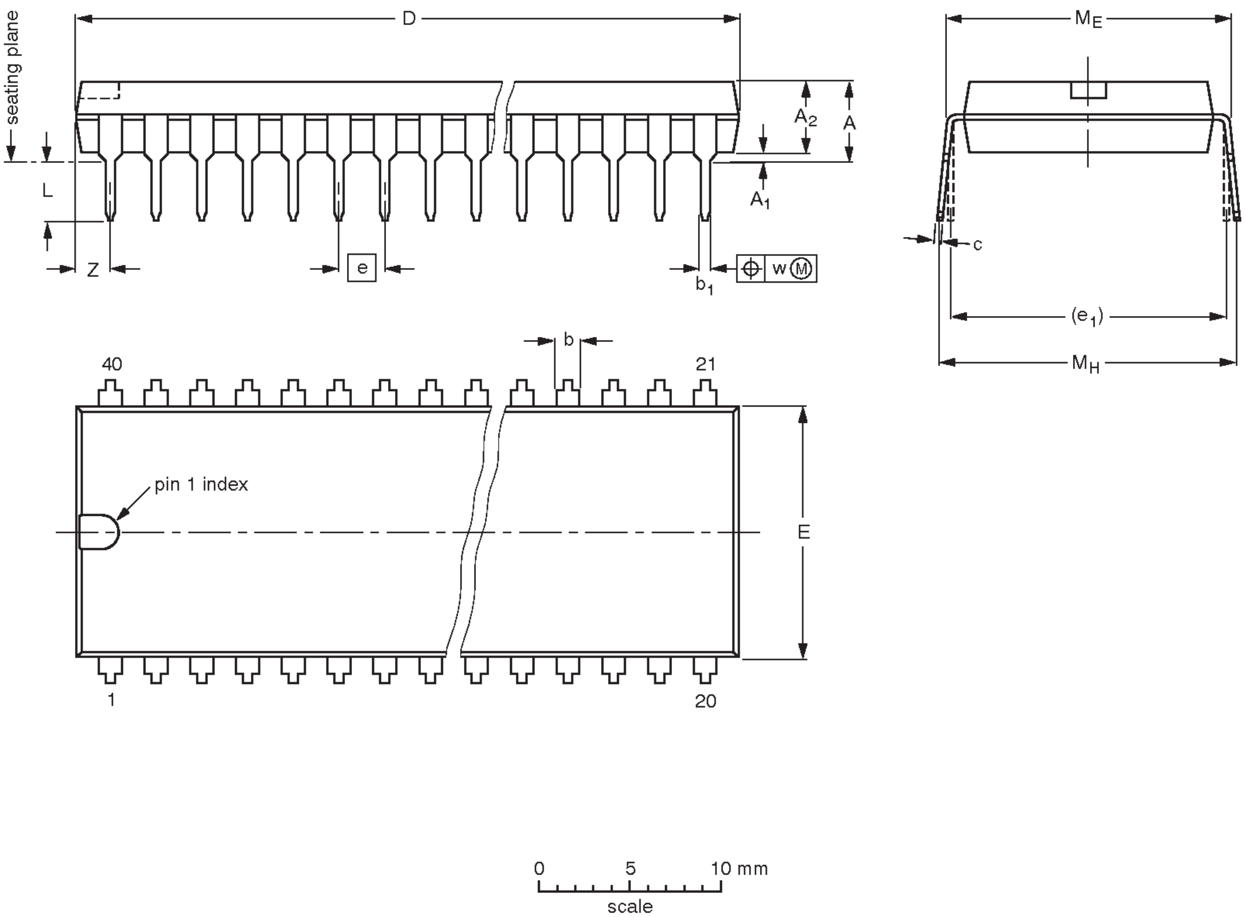



**Figure 25. $I_{CC}$ Test Condition, Power Down Mode**
**All other pins are disconnected. $V_{CC}$ = 2 V to 5.5 V**

**DIP40: plastic dual in-line package; 40 leads (600 mil)** **SOT129-1**

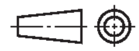



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

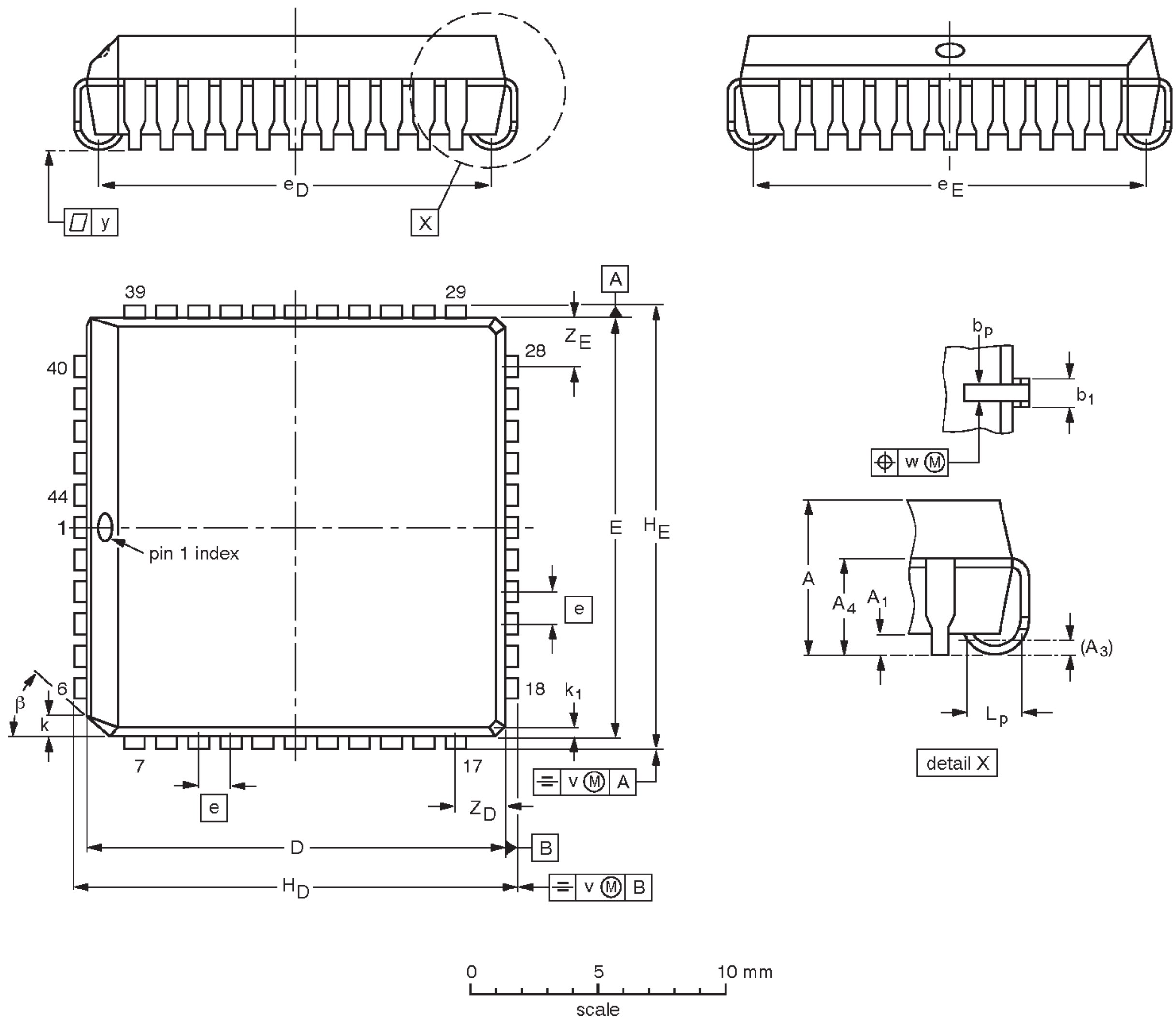
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7 | 0.51 | 4.0 | 1.70<br>1.14 | 0.53<br>0.38 | 0.36<br>0.23 | 52.50<br>51.50 | 14.1<br>13.7 | 2.54 | 15.24 | 3.60<br>3.05 | 15.80<br>15.24 | 17.42<br>15.90 | 0.254 | 2.25 |
| inches | 0.19 | 0.020 | 0.16 | 0.067<br>0.045 | 0.021<br>0.015 | 0.014<br>0.009 | 2.067<br>2.028 | 0.56<br>0.54 | 0.10 | 0.60 | 0.14<br>0.12 | 0.62<br>0.60 | 0.69<br>0.63 | 0.01 | 0.089 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT129-1 | 051G08 | MO-015 | SC-511-40 | |  | ~~95-01-14~~<br>99-12-27 |

## PLCC44: plastic leaded chip carrier; 44 leads — SOT187-2




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

| UNIT | A | $A_1$ min. | $A_3$ | $A_4$ max. | $b_p$ | $b_1$ | D(1) | E(1) | e | $e_D$ | $e_E$ | $H_D$ | $H_E$ | k | $k_1$ max. | $L_p$ | v | w | y | $Z_D$(1) max. | $Z_E$(1) max. | β |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.57<br>4.19 | 0.51 | 0.25 | 3.05 | 0.53<br>0.33 | 0.81<br>0.66 | 16.66<br>16.51 | 16.66<br>16.51 | 1.27 | 16.00<br>14.99 | 16.00<br>14.99 | 17.65<br>17.40 | 17.65<br>17.40 | 1.22<br>1.07 | 0.51 | 1.44<br>1.02 | 0.18 | 0.18 | 0.10 | 2.16 | 2.16 | 45° |
| inches | 0.180<br>0.165 | 0.020 | 0.01 | 0.12 | 0.021<br>0.013 | 0.032<br>0.026 | 0.656<br>0.650 | 0.656<br>0.650 | 0.05 | 0.630<br>0.590 | 0.630<br>0.590 | 0.695<br>0.685 | 0.695<br>0.685 | 0.048<br>0.042 | 0.020 | 0.057<br>0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT187-2 | 112E10 | MO-047 | | | | ~~97-12-16~~<br>99-12-27 |