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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x14b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb10f16e-a-qfp32

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3.7 Analog

14/12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 14-, 12-, and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 14-bit, 12-bit and 10-bit modes
- Supports an output update rate of up to 1 Msps in 12-bit mode
- · Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated factory-calibrated temperature sensor

12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- · Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- · Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- · Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- · Supports references from internal supply, on-chip precision reference, or external VREF pin

Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- · Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- · Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- · Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ±20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Temperature Sensor	I _{TSENSE}	SENSE		75	120	μA
Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3) ⁶	I _{DAC}			125	_	μA
Comparators (CMP0, CMP1)	I _{CMP}	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	_	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Comparator Reference	I _{CPREF}		_	TBD	_	μA
Voltage Supply Monitor (VMON0)	I _{VMON}		—	15	20	μA

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.

2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.

3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.

- 4. ADC0 power excludes internal reference supply current.
- 5. The internal reference is enabled as-needed when operating the ADC in low power mode. Total ADC + Reference current will depend on sampling rate.

6. DAC supply current for each enabled DA and not including external load on pin.

4.1.3 Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
VDD Supply Monitor Threshold	V _{VDDM}		1.85	1.95	2.1	V
Power-On Reset (POR) Threshold	V _{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	_	1.36	V
VDD Ramp Time	t _{RMP}	Time to V _{DD} > 2.2 V	10		_	μs
Reset Delay from POR	t _{POR}	Relative to V _{DD} > V _{POR}	3	10	31	ms
Reset Delay from non-POR source	t _{RST}	Time between release of reset source and code execution	_	50	_	μs
RST Low Time to Generate Reset	t _{RSTL}		15	_	_	μs
Missing Clock Detector Response Time (final rising edge to reset)	t _{MCD}	F _{SYSCLK} >1 MHz	_	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F _{MCD}		_	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t _{MON}		—	2	_	μs

Table 4.3. Reset and Supply Monitor

4.1.4 Flash Memory

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Write Time ^{1,2}	t _{WRITE}	One Byte,	19	20	21	μs
		F _{SYSCLK} = 24.5 MHz				
Erase Time ^{1 ,2}	t _{ERASE}	One Page,	5.2	5.35	5.5	ms
		F _{SYSCLK} = 24.5 MHz				
V _{DD} Voltage During Programming ³	V _{PROG}		2.2		3.6	V
Endurance (Write/Erase Cycles)	N _{WE}		20k	100k		Cycles

Table 4.4. Flash Memory

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.

2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.

3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).

4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Idle Mode Wake-up Time	t _{IDLEWK}		2	_	3	SYSCLKs
Suspend Mode Wake-up Time	t _{SUS-}	SYSCLK = HFOSC0	—	170	_	ns
	PENDWK	CLKDIV = 0x00				
Snooze Mode Wake-up Time	t _{SLEEPWK}	SYSCLK = HFOSC0	—	12	_	μs
		CLKDIV = 0x00				

4.1.10 Voltage Reference

Table 4.1	0. Volt	age Re	ference
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Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
Internal Fast Settling Reference								
Output Voltage	V _{REFFS}		1.62	1.65	1.68	V		
(Full Temperature and Supply Range)								
Temperature Coefficient	TC _{REFFS}			50	_	ppm/°C		
Turn-on Time	t _{REFFS}		_	_	1.5	μs		
Power Supply Rejection	PSRR _{REF} FS	RR _{REF}		400		ppm/V		
On-chip Precision Reference								
Valid Supply Range	V _{DD}	1.2 V Output	2.2		3.6	V		
		2.4 V Output	2.7	_	3.6	V		
Output Voltage	V _{REFP}	1.2 V Output, T = 25 °C	TBD	1.2	TBD	V		
		2.4 V Output, T = 25 °C	TBD	2.4	TBD	V		
Turn-on Time, settling to 0.5 LSB	t _{VREFP}	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	_	3	_	ms		
		0.1 µF ceramic bypass on VREF pin	_	100	_	μs		
Load Regulation	LR _{VREFP}	Load = 0 to 200 µA to GND	—	TBD	—	μV/μΑ		
Load Capacitor	C _{VREFP}	Load = 0 to 200 µA to GND	0.1	_	_	μF		
Short-circuit current	ISC _{VREFP}		—	_	8	mA		
Power Supply Rejection	PSRR _{VRE} FP	R _{VRE}		TBD	_	ppm/V		
External Reference			1	1	1			
Input Current	I _{EXTREF}	ADC Sample Rate = 1 Msps; VREF = 3.0 V	_	5	_	μA		

4.1.11 Temperature Sensor

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Uncalibrated Offset	V _{OFF}	T _A = 0 °C	_	TBD	_	mV
Uncalibrated Offset Error ¹	E _{OFF}	T _A = 0 °C	_	TBD	_	mV
Slope	М		—	2.83	—	mV/°C
Slope Error ¹	E _M		_	TBD	_	μV/°C
Linearity			_	TBD	_	°C
Turn-on Time			—	TBD	—	μs
Temp Sensor Error Using Typical		T = 0 °C to 70 °C	TBD		TBD	°C
set ^{2, 3}		T = -20 °C to 85 °C	-3	—	3	°C
		T = -40 °C to 105 °C	TBD		TBD	°C

Table 4.11. Temperature Sensor

Note:

1. Represents one standard deviation from the mean.

2. The factory-calibrated offset value is stored in the read-only area of flash in locations 0xFFD4 (low byte) and 0xFFD5 (high byte). The 14-bit result represents the output of the ADC when sampling the temp sensor using the 1.65 V internal voltage reference.

3. Temp sensor error is based upon characterization and is not tested across temperature in production. The values represent three standard deviations above and below the mean.

4.1.13 Comparators

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Response Time, CPMD = 00	t _{RESP0}	+100 mV Differential		100	_	ns
(Highest Speed)		-100 mV Differential	_	150	_	ns
Response Time, CPMD = 11 (Low-	t _{RESP3}	+100 mV Differential		1.5	_	μs
est Power)		-100 mV Differential		3.5		μs
Positive Hysteresis	HYS _{CP+}	CPHYP = 00		0.4	_	mV
Mode 0 (CPMD = 00)		CPHYP = 01		8		mV
		CPHYP = 10		16		mV
		CPHYP = 11		32	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00		-0.4		mV
Mode 0 (CPMD = 00)		CPHYN = 01		-8	_	mV
		CPHYN = 10		-16	_	mV
		CPHYN = 11		-32	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00		0.5	_	mV
Mode 1 (CPMD = 01)		CPHYP = 01		6	_	mV
		CPHYP = 10	_	12	_	mV
		CPHYP = 11	_	24	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	_	-0.5	_	mV
Mode 1 (CPMD = 01)		CPHYN = 01	_	-6	_	mV
		CPHYN = 10	_	-12	_	mV
		CPHYN = 11	_	-24	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	0.7	_	mV
Mode 2 (CPMD = 10)		CPHYP = 01	_	4.5	_	mV
		CPHYP = 10	_	9	_	mV
		CPHYP = 11	_	18	_	mV
Negative Hysteresis	HYS _{CP-}	CPHYN = 00	_	-0.6	_	mV
Mode 2 (CPMD = 10)		CPHYN = 01	_	-4.5	_	mV
		CPHYN = 10	_	-9	_	mV
		CPHYN = 11		-18	_	mV
Positive Hysteresis	HYS _{CP+}	CPHYP = 00	_	1.5	_	mV
Mode 3 (CPMD = 11)		CPHYP = 01	_	4	_	mV
		CPHYP = 10	_	8	_	mV
		CPHYP = 11		16	_	mV

Table 4.13. Comparators

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number					
1	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
2	VIO	I/O Supply Power Input			
3	VDD	Supply Power Input			
4	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
5	P3.7 /	Multifunction I/O /			
	C2D	C2 Debug Data			
6	P3.4	Multifunction I/O			
7	P3.3	Multifunction I/O			DAC3
8	P3.2	Multifunction I/O			DAC2
9	P3.1	Multifunction I/O			DAC1
10	P3.0	Multifunction I/O			DAC0
11	P2.6	Multifunction I/O			ADC0.19
					CMP1P.8
					CMP1N.8
12	P2.5	Multifunction I/O		CLU3OUT	ADC0.18
					CMP1P.7
					CMP1N.7
13	P2.4	Multifunction I/O			ADC0.17
					CMP1P.6
					CMP1N.6
14	P2.3	Multifunction I/O	Yes	P2MAT.3	ADC0.16
				CLU1B.15	CMP1P.5
				CLU2B.15	CMP1N.5
				CLU3A.15	

Table 6.1. Pin Definitions for EFM8LB1x-QFN32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
22	P1.3	Multifunction I/O	Yes	P1MAT 3	
				CLU0B 13	
				CLU1B.11	
				CLU2B 11	
				CLU3A.13	
23	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	CMP0P.8
				CLU1A.11	CMP0N.8
				CLU2B.10	
				CLU3A.12	
				CLU3B.13	
24	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	CMP0P.7
				CLU1B.10	CMP0N.7
				CLU2A.11	
				CLU3B.12	
25	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU1OUT	CMP0P.6
				CLU0A.12	CMP0N.6
				CLU1A.10	CMP1P.1
				CLU2A.10	CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU0B.11	CMP1P.0
				CLU1B.9	CMP1N.0
				CLU3A.11	
27	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	
				CLU0A.11	
				CLU1B.8	
				CLU3A.10	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.10
				CLU2OUT	CMP1P.4
				CLU0B.14	CMP1N.4
				CLU1A.13	
				CLU2B.13	
				CLU3B.11	
13	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.9
				I2C0_SCL	CMP1P.3
				CLU0A.14	CMP1N.3
				CLU1A.12	
				CLU2B.12	
				CLU3B.10	
14	P1.3	Multifunction I/O	Yes	P1MAT.3	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	
				CLU1A.11	
				CLU2B.10	
				CLU3A.12	
				CLU3B.13	
17	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	
				CLU1B.10	
				CLU2A.11	
				CLU3B.12	
18	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU0A.12	
				CLU1A.10	
				CLU2A.10	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU1OUT	CMP1P.1
				CLU0B.11	CMP1N.1
				CLU1B.9	
				CLU3A.11	
20	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	CMP1P.0
				CLU0A.11	CMP1N.0
				CLU1B.8	
				CLU3A.10	
21	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	
22	P0.4	Multifunction I/O	Yes	P0MAT.4	ADC0.2
				INT0.4	CMP0P.2
				INT1.4	CMP0N.2
				UART0_TX	
				CLU0A.10	
				CLU1A.8	
23	P0.3	Multifunction I/O	Yes	P0MAT.3	XTAL2
				EXTCLK	
				INT0.3	
				INT1.3	
				CLU0B.9	
				CLU2B.10	
				CLU3A.9	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.2	Multifunction I/O	Yes	P0MAT.2	XTAL1
				INT0.2	ADC0.1
				INT1.2	CMP0P.1
				CLU0OUT	CMP0N.1
				CLU0A.9	
				CLU2B.8	
				CLU3A.8	
3	P0.1	Multifunction I/O	Yes	P0MAT.1	ADC0.0
				INT0.1	CMP0P.0
				INT1.1	CMP0N.0
				CLU0B.8	AGND
				CLU2A.9	
				CLU3B.9	
4	P0.0	Multifunction I/O	Yes	P0MAT.0	VREF
				INT0.0	
				INT1.0	
				CLU0A.8	
				CLU2A.8	
				CLU3B.8	
5	GND	Ground			
6	VDD / VIO	Supply Power Input			
7	RSTb /	Active-low Reset /			
	C2CK	C2 Debug Clock			
8	P3.0 /	Multifunction I/O /			
	C2D	C2 Debug Data			
9	P2.3	Multifunction I/O	Yes	P2MAT.3	DAC3
				CLU1B.15	
				CLU2B.15	
				CLU3A.15	
10	P2.2	Multifunction I/O	Yes	P2MAT.2	DAC2
				CLU1A.15	
				CLU2B.14	
				CLU3A.14	

Pin	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
Number	D2.4	Multifunction 1/0	Vec		DAC1
	P2.1	Multifunction I/O	res		DACT
				CLU2A.15	
10	D 2 0	Multifunction I/O	Vaa		DACO
12	P2.0		res		DACU
				CLU2A.14	
12	D1 7	Multifunction I/O	Vaa	CLU3B.14	ADC0 12
13	P1.7		res		
				CLUUB. 13	
				CLUIB. 13	CMP IN.6
14	D1 6	Multifunction 1/0	Vaa	CLUZA. 13	ADC0 11
14	P1.0		res		
				CLU3OUT	CMP1P.5
				CLUUA.15	CMP1N.5
				CLU1B.12	
	D 4.5			CLU2A.12	
15	P1.5	Multifunction I/O	Yes	P1MA1.5	ADC0.10
				CLU2OUT	CMP1P.4
				CLU0B.14	CMP1N.4
				CLU1A.13	
				CLU2B.13	
				CLU3B.11	
16	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.9
				I2C0_SCL	CMP1P.3
				CLU0A.14	CMP1N.3
				CLU1A.12	
				CLU2B.12	
				CLU3B.10	
17	P1.3	Multifunction I/O	Yes	P1MAT.3	CMP1P.2
				I2C0_SDA	CMP1N.2
				CLU0B.13	
				CLU1B.11	
				CLU2B.11	
				CLU3A.13	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.8
				CLU0A.13	
				CLU1A.11	
				CLU2B.10	
				CLU3A.12	
				CLU3B.13	
19	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.7
				CLU0B.12	
				CLU1B.10	
				CLU2A.11	
				CLU3B.12	
20	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.6
				CLU0A.12	
				CLU1A.10	
				CLU2A.10	
21	P0.7	Multifunction I/O	Yes	P0MAT.7	ADC0.5
				INT0.7	CMP0P.5
				INT1.7	CMP0N.5
				CLU1OUT	CMP1P.1
				CLU0B.11	CMP1N.1
				CLU1B.9	
				CLU3A.11	
22	P0.6	Multifunction I/O	Yes	P0MAT.6	ADC0.4
				CNVSTR	CMP0P.4
				INT0.6	CMP0N.4
				INT1.6	CMP1P.0
				CLU0A.11	CMP1N.0
				CLU1B.8	
				CLU3A.10	
23	P0.5	Multifunction I/O	Yes	P0MAT.5	ADC0.3
				INT0.5	CMP0P.3
				INT1.5	CMP0N.3
				UART0_RX	
				CLU0B.10	
				CLU1A.9	

Dimension	Min	Мах		
Note:				
1. All dimensions shown are in millimeters	(mm) unless otherwise noted.			
2. Dimensioning and Tolerancing is per the	e ANSI Y14.5M-1994 specification.			
3. This Land Pattern Design is based on the	ne IPC-7351 guidelines.			
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabri- cation Allowance of 0.05mm.				
 All metal pads are to be non-solder mas minimum, all the way around the pad. 	sk defined (NSMD). Clearance between the so	older mask and the metal pad is to be 60 μm		
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release				
7. The stencil thickness should be 0.125 mm (5 mils).				
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.				
9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad.				

- 10. A No-Clean, Type-3 solder paste is recommended.
- 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).





The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

Dimension	Min	Тур	Мах	
е		0.40 BSC		
e1	0.45 BSC			
J	1.60	1.70	1.80	
К	1.60	1.70	1.80	
L	0.35	0.40	0.45	
L1	0.25	0.30	0.35	
ааа	_	0.10	—	
bbb	—	0.10	—	
ссс	_	0.08	—	
ddd	_	0.1	_	
eee	_	0.1	—	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to JEDEC Solid State Outline MO-248 but includes custom features which are toleranced per supplier designation.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 QFN24 PCB Land Pattern



Figure 9.2. QFN24 PCB Land Pattern Drawing

Table 9.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Мах	
C1	3.00		
C2	3.00		
e	0.4 REF		
X1	0.20		
X2	1.80		
Y1	0.80		
Y2	1.80		
Y3	0.4		
f	2.50 REF		
с	0.25 0.35		

Dimension	Min	Мах			
Note:					
1. All dimensions shown are in millimeters	(mm) unless otherwise noted.				
2. Dimensioning and Tolerancing is per the	ANSI Y14.5M-1994 specification.				
3. This Land Pattern Design is based on th	3. This Land Pattern Design is based on the IPC-SM-782 guidelines.				
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μn minimum, all the way around the pad.					
5. A stainless steel, laser-cut and electro-p	olished stencil with trapezoidal walls should b	be used to assure good solder paste release.			
6. The stencil thickness should be 0.125 mm (5 mils).					
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.					
8. A 2 x 1 array of 1.20 mm x 0.95 mm ope	enings on a 1.15 mm pitch should be used for	the center pad.			
9. A No-Clean, Type-3 solder paste is reco	mmended.				

10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN24 Package Marking



Figure 9.3. QFN24 Package Marking

The package marking consists of:

- PPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.
- # The device revision (A, B, etc.).

10. QSOP24 Package Specifications

10.1 QSOP24 Package Dimensions



Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Тур	Мах		
A	—	—	1.75		
A1	0.10	—	0.25		
b	0.20	_	0.30		
с	0.10	—	0.25		
D		8.65 BSC			
E	6.00 BSC				
E1	3.90 BSC				
е	0.635 BSC				
L	0.40	— 1.27			
theta	0°	_	8°		



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