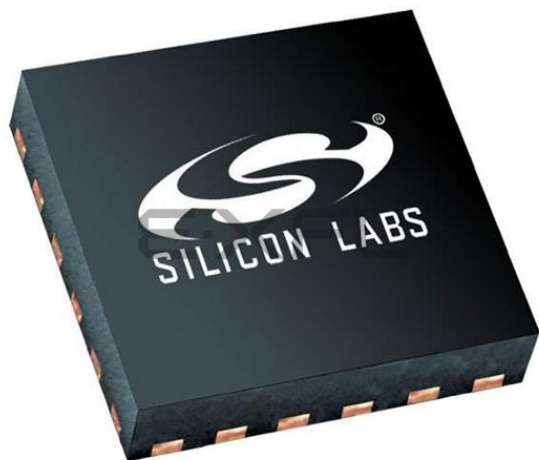




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Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I ² C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x14b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8lb11f32e-a-qfn24

3. System Overview

3.1 Introduction

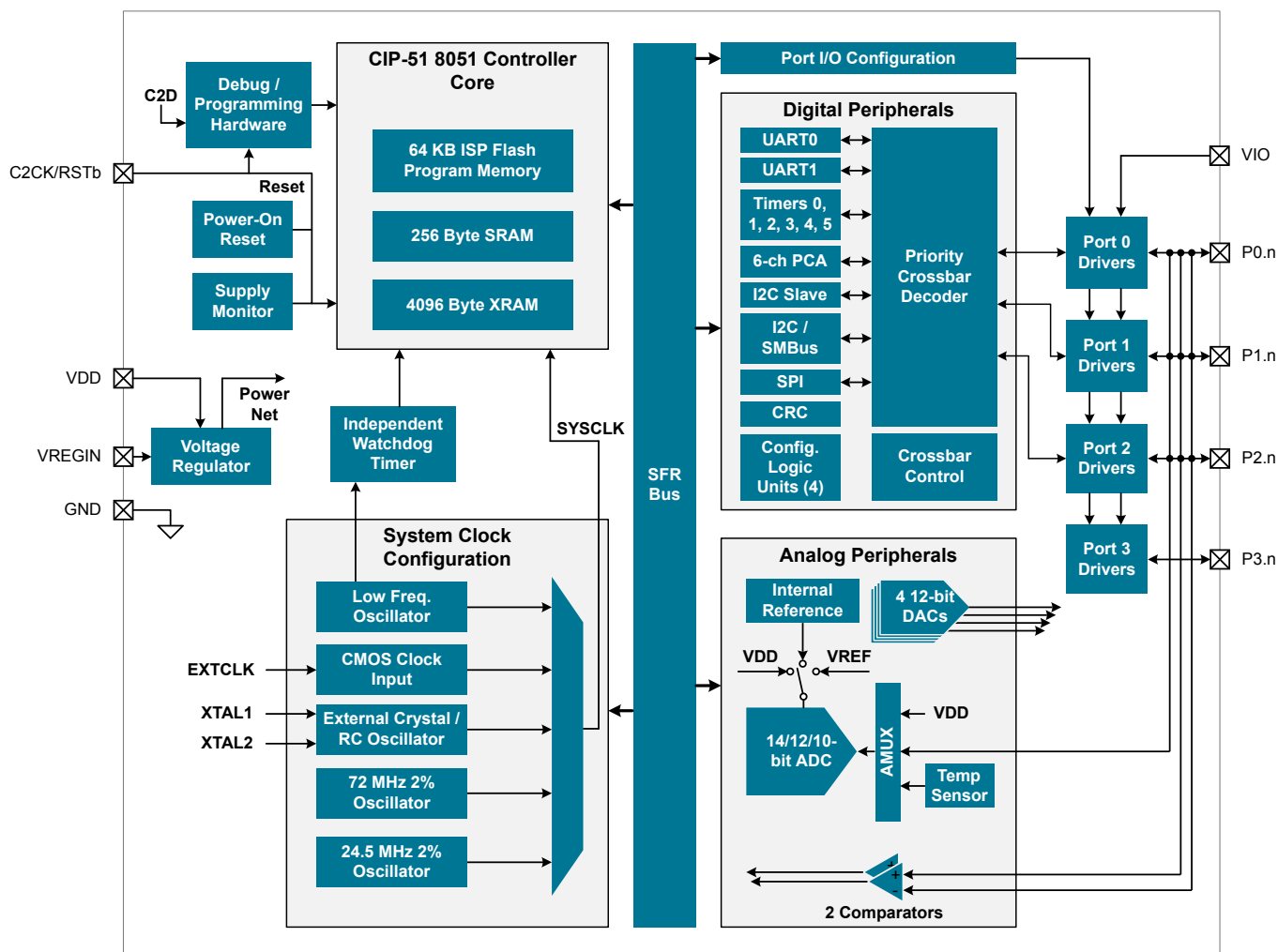


Figure 3.1. Detailed EFM8LB1 Block Diagram

3.7 Analog

14/12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 14-, 12-, and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 14-bit, 12-bit and 10-bit modes
- Supports an output update rate of up to 1 Msps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated factory-calibrated temperature sensor

12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
 - Internal connection to LDO output
 - Direct connection to GND
 - Direct connection to VDD
 - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

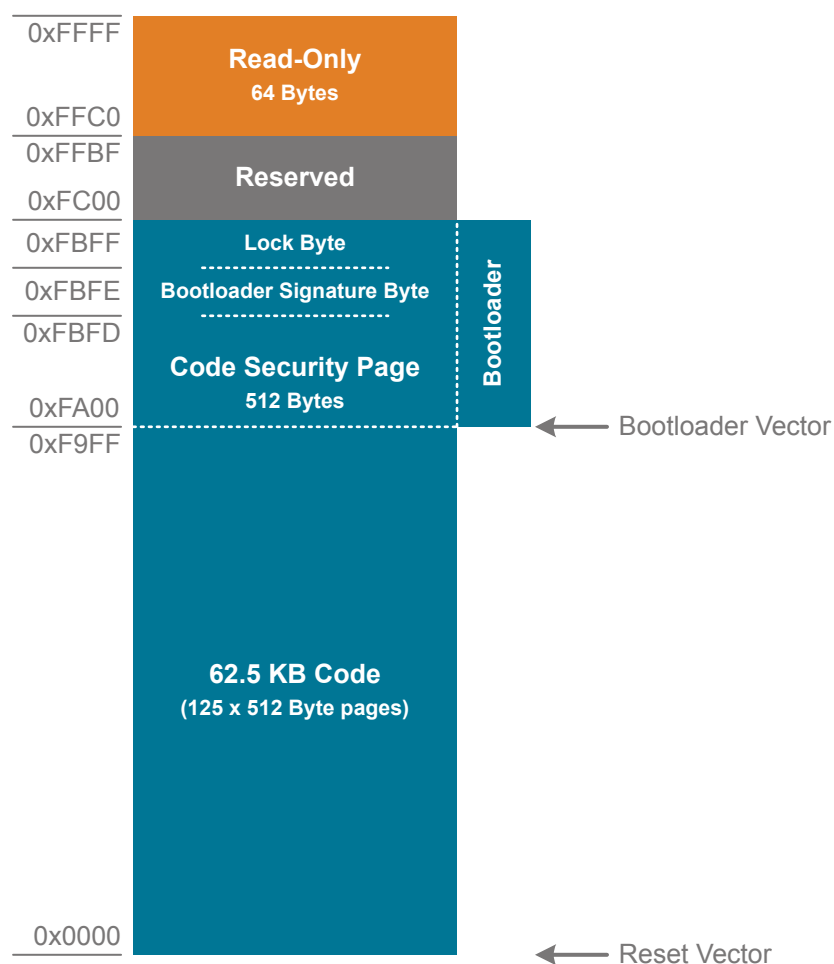


Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time ^{1,2}	t_{WRITE}	One Byte, $F_{\text{SYSCLK}} = 24.5 \text{ MHz}$	19	20	21	μs
Erase Time ^{1,2}	t_{ERASE}	One Page, $F_{\text{SYSCLK}} = 24.5 \text{ MHz}$	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming ³	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{\text{SUS-}}t_{\text{PENDWK}}$	$\text{SYSCLK} = \text{HFOSC0}$ $\text{CLKDIV} = 0x00$	—	170	—	ns
Snooze Mode Wake-up Time	t_{SLEEPWK}	$\text{SYSCLK} = \text{HFOSC0}$ $\text{CLKDIV} = 0x00$	—	12	—	μs

4.1.10 Voltage Reference

Table 4.10. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}		1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	μs
Power Supply Rejection	$PSRR_{\text{REFFS}}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	V_{DD}	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	V_{REFP}	1.2 V Output, T = 25 °C	TBD	1.2	TBD	V
		2.4 V Output, T = 25 °C	TBD	2.4	TBD	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	—	3	—	ms
		0.1 μF ceramic bypass on VREF pin	—	100	—	μs
Load Regulation	LR_{VREFP}	Load = 0 to 200 μA to GND	—	TBD	—	μV/μA
Load Capacitor	C_{VREFP}	Load = 0 to 200 μA to GND	0.1	—	—	μF
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{\text{VREFP}}$		—	TBD	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	ADC Sample Rate = 1 Msps; VREF = 3.0 V	—	5	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS _{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V _{IN}		-0.25	—	V _{IO} +0.25	V
Input Pin Capacitance	C _{CP}		—	7.5	—	pF
Internal Reference DAC Resolution	N _{bits}		6			bits
Common-Mode Rejection Ratio	CMRR _{CP}		—	70	—	dB
Power Supply Rejection Ratio	PSRR _{CP}		—	72	—	dB
Input Offset Voltage	V _{OFF}	T _A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC _{OFF}		—	3.5	—	μV/°

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay	t _{DLY}	Through single CLU	TBD	—	TBD	ns
Clocking Frequency	F _{CLK}	1 or 2 CLUs Cascaded	—	—	73.5	MHz
		3 or 4 CLUs Cascaded	—	—	36.75	MHz

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	$I_{OH} = -7 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -3.3 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.8 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (High Drive)	V_{OL}	$I_{OL} = 13.5 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 7 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 3.6 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output High Voltage (Low Drive)	V_{OH}	$I_{OH} = -4.75 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -2.25 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.2 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (Low Drive)	V_{OL}	$I_{OL} = 6.5 \text{ mA}$, $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 3.5 \text{ mA}$, $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 1.8 \text{ mA}$, $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Input High Voltage	V_{IH}		$0.7 \times V_{IO}$	—	—	V
Input Low Voltage	V_{IL}		—	—	$0.3 \times V_{IO}$	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current ($V_{IN} = 0 \text{ V}$)	I_{PU}	$V_{DD} = 3.6$	-30	-20	-10	μA
Input Leakage (Pullups off or Analog)	I_{LK}	$\text{GND} < V_{IN} < V_{IO}$	TBD	—	TBD	μA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	$V_{IO} < V_{IN} < V_{IO} + 2.5 \text{ V}$ Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	μA

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12 CLU3B.13	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.12	ADC0.7 CMP0P.7 CMP0N.7
25	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU1OUT CLU0A.12 CLU1A.10 CLU2A.10	ADC0.6 CMP0P.6 CMP0N.6 CMP1P.1 CMP1N.1
26	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU0B.11 CLU1B.9 CLU3A.11	ADC0.5 CMP0P.5 CMP0N.5 CMP1P.0 CMP1N.0
27	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU0A.11 CLU1B.8 CLU3A.10	ADC0.4 CMP0P.4 CMP0N.4

6.3 EFM8LB1x-QFN24 Pin Definitions

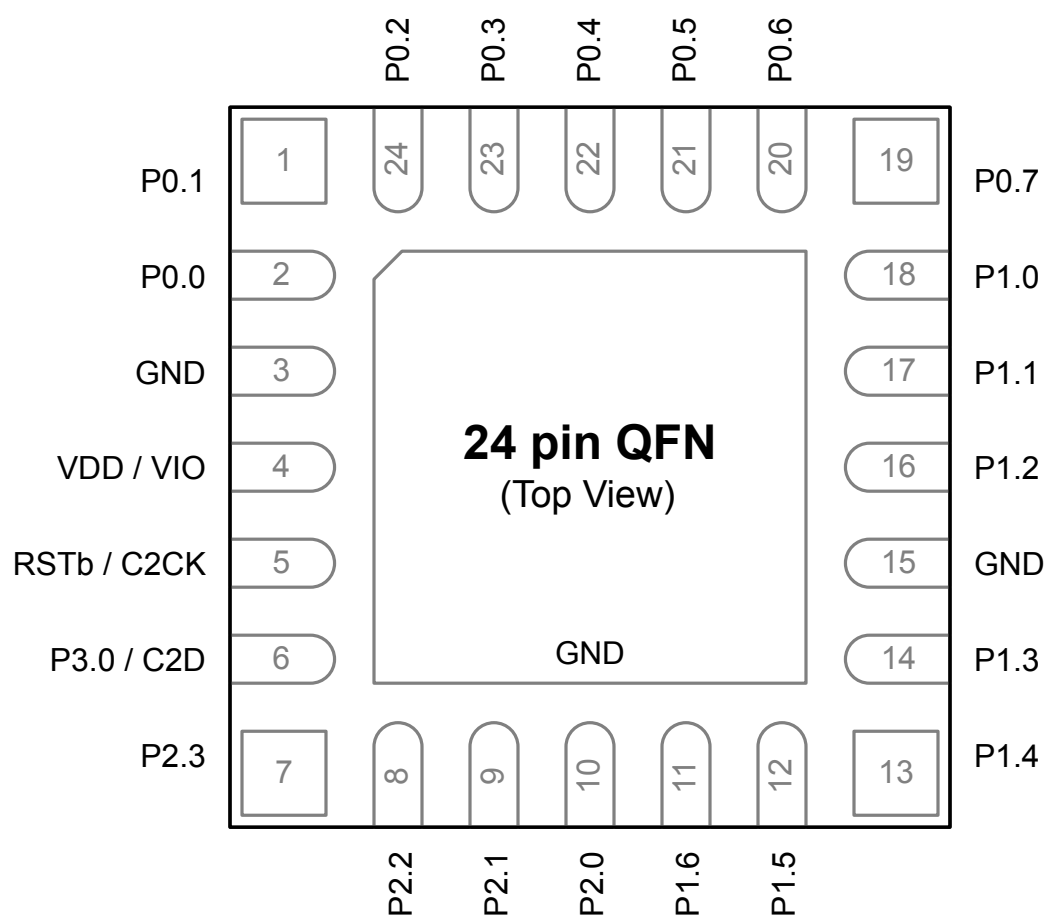


Figure 6.3. EFM8LB1x-QFN24 Pinout

Table 6.3. Pin Definitions for EFM8LB1x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.10 CMP1P.4 CMP1N.4
13	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.9 CMP1P.3 CMP1N.3
14	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2
15	GND	Ground			
16	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12 CLU3B.13	ADC0.8
17	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.12	ADC0.7
18	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0A.12 CLU1A.10 CLU2A.10	ADC0.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
12	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
13	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.12 CMP1P.6 CMP1N.6
14	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5
15	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.10 CMP1P.4 CMP1N.4
16	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.9 CMP1P.3 CMP1N.3
17	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8	ADC0.2 CMP0P.2 CMP0N.2

Dimension	Min	Typ	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to JEDEC Solid State Outline MO-220. 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.			

7.2 QFN32 PCB Land Pattern

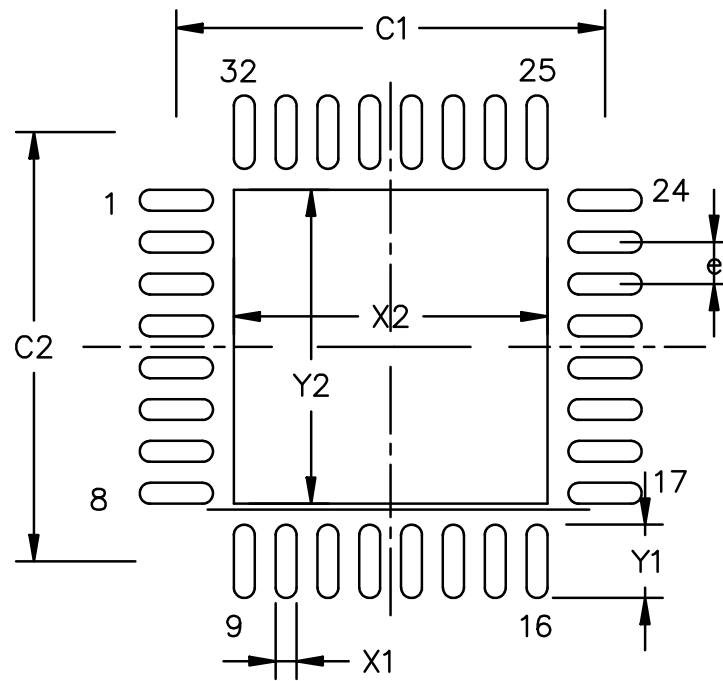


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	—	4.00
C2	—	4.00
X1	—	0.2
X2	—	2.8
Y1	—	0.75
Y2	—	2.8
e	—	0.4

Dimension	Min	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm. 5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 7. The stencil thickness should be 0.125 mm (5 mils). 8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad. 10. A No-Clean, Type-3 solder paste is recommended. 11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. QFN24 Package Specifications

9.1 QFN24 Package Dimensions

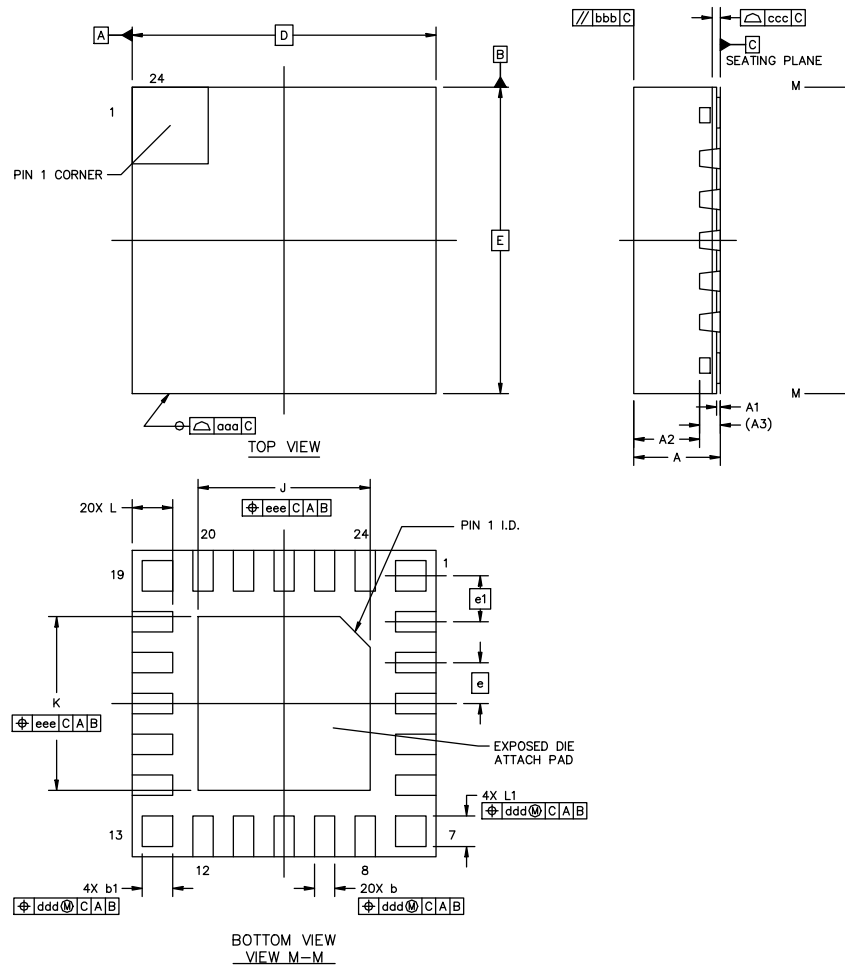


Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D	3.00 BSC		
E	3.00 BSC		

Dimension	Min	Typ	Max
aaa		0.20	
bbb		0.18	
ccc		0.10	
ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 QSOP24 PCB Land Pattern

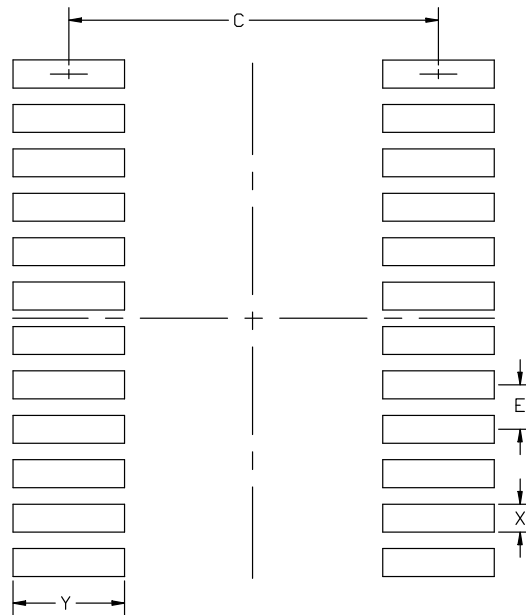


Figure 10.2. QSOP24 PCB Land Pattern Drawing

Table 10.2. QSOP24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Revision History

11.1 Revision 0.1

Initial release.

11.2 Revision 0.2

Added information on the bootloader to [3.10 Bootloader](#).

Updated some characterization TBD values.

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