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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 20x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f32e-a-qfp32">https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f32e-a-qfp32</a>

## 1. Feature List

The EFM8LB1 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 72 MHz maximum operating frequency
- Memory:
  - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
  - Up to 25 pins 5 V tolerant under bias
  - Selectable state retention through reset events
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 72 MHz oscillator with accuracy of  $\pm 2\%$
  - Internal 24.5 MHz oscillator with  $\pm 2\%$  accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
  - External crystal/RC/C Oscillator (up to 25 MHz)
- Analog:
  - 14/12/10-Bit Analog-to-Digital Converter (ADC)
  - Internal calibrated temperature sensor ( $\pm 3\text{ }^{\circ}\text{C}$ )
  - 4 x 12-Bit Digital-to-Analog Converters (DAC)
  - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
  - 2 x UART, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™/I2C™ Master / Slave, up to 400 kbps
  - I2C High-Speed Slave, up to 3.4 Mbps
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
  - 4 Configurable Logic Units
- Timers/Counters and PWM:
  - 6-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 6 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8LB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified (pending) and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

### 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

### 3.9 Debugging

The EFM8LB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

#### 4.1.8 Crystal Oscillator

**Table 4.8. Crystal Oscillator**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	$f_{XTAL}$		0.02	—	25	MHz
Crystal Drive Current	$I_{XTAL}$	XFCN = 0	—	0.5	—	$\mu A$
		XFCN = 1	—	1.5	—	$\mu A$
		XFCN = 2	—	4.8	—	$\mu A$
		XFCN = 3	—	14	—	$\mu A$
		XFCN = 4	—	40	—	$\mu A$
		XFCN = 5	—	120	—	$\mu A$
		XFCN = 6	—	550	—	$\mu A$
		XFCN = 7	—	2.6	—	mA

#### 4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	$V_{OH}$	$I_{OH} = -7 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -3.3 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.8 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (High Drive)	$V_{OL}$	$I_{OL} = 13.5 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 7 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 3.6 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output High Voltage (Low Drive)	$V_{OH}$	$I_{OH} = -4.75 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -2.25 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.2 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (Low Drive)	$V_{OL}$	$I_{OL} = 6.5 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 3.5 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 1.8 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Input High Voltage	$V_{IH}$		$0.7 \times V_{IO}$	—	—	V
Input Low Voltage	$V_{IL}$		—	—	$0.3 \times V_{IO}$	V
Pin Capacitance	$C_{IO}$		—	7	—	pF
Weak Pull-Up Current ( $V_{IN} = 0 \text{ V}$ )	$I_{PU}$	$V_{DD} = 3.6$	-30	-20	-10	$\mu\text{A}$
Input Leakage (Pullups off or Analog)	$I_{LK}$	$\text{GND} < V_{IN} < V_{IO}$	TBD	—	TBD	$\mu\text{A}$
Input Leakage Current with $V_{IN}$ above $V_{IO}$	$I_{LK}$	$V_{IO} < V_{IN} < V_{IO} + 2.5 \text{ V}$ Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	$\mu\text{A}$

## 4.2 Thermal Conditions

**Table 4.16. Thermal Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$\theta_{JA}$	QFN24 Packages	—	TBD	—	°C/W
		QFN32 Packages	—	TBD	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W
<b>Note:</b> 1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

## 4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.17 Absolute Maximum Ratings on page 27](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.17. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	$T_{BIAS}$		-55	125	°C
Storage Temperature	$T_{STG}$		-65	150	°C
Voltage on VDD	$V_{DD}$		GND-0.3	4.2	V
Voltage on VIO <sup>2</sup>	$V_{IO}$		GND-0.3	$V_{DD}+0.3$	V
Voltage on I/O pins or RSTb, excluding P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	$V_{IN}$	$V_{IO} > \text{TBD V}$	GND-0.3	TBD	V
		$V_{IO} < \text{TBD V}$	GND-0.3	TBD	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	$V_{IN}$		GND-0.3	$V_{DD}+0.3$	V
Total Current Sunk into Supply Pin	$I_{VDD}$		—	400	mA
Total Current Sourced out of Ground Pin	$I_{GND}$		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	$I_{IO}$		-100	100	mA
<b>Note:</b> 1. Exposure to maximum rating conditions for extended periods may affect device reliability. 2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.					

## 5. Typical Connection Diagrams

### 5.1 Power

Figure 5.1 Power Connection Diagram on page 28 shows a typical connection diagram for the power pins of the device.

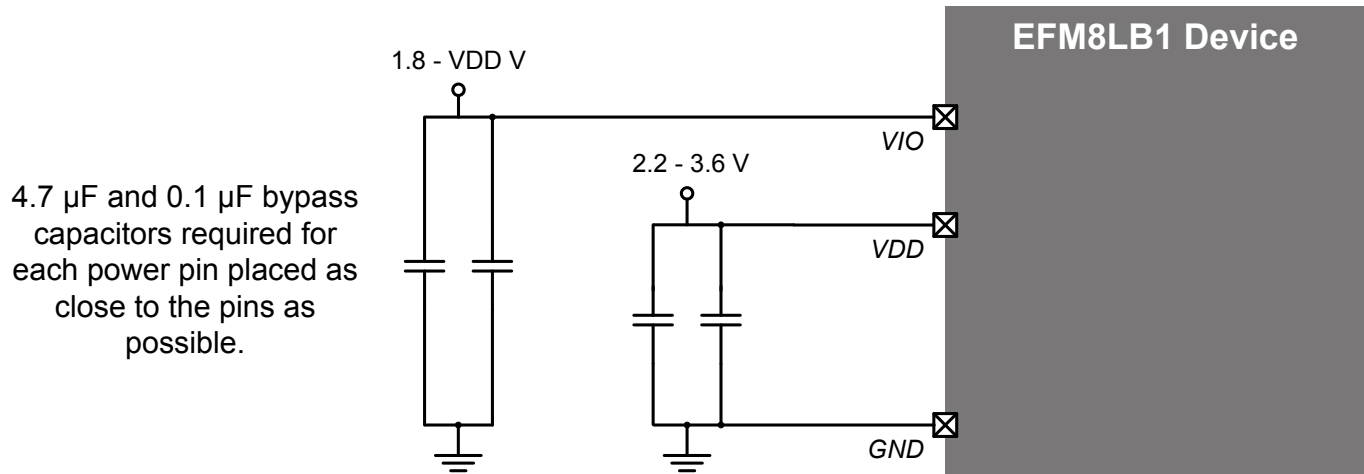


Figure 5.1. Power Connection Diagram

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
15	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU2OUT CLU1A.15 CLU2B.14 CLU3A.14	ADC0.15 CMP1P.4 CMP1N.4
16	P2.1	Multifunction I/O	Yes	P2MAT.1 I2C0_SCL CLU1B.14 CLU2A.15 CLU3B.15	ADC0.14 CMP1P.3 CMP1N.3
17	P2.0	Multifunction I/O	Yes	P2MAT.0 I2C0_SDA CLU1A.14 CLU2A.14 CLU3B.14	CMP1P.2 CMP1N.2
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.10



## 6.2 EFM8LB1x-QFP32 Pin Definitions

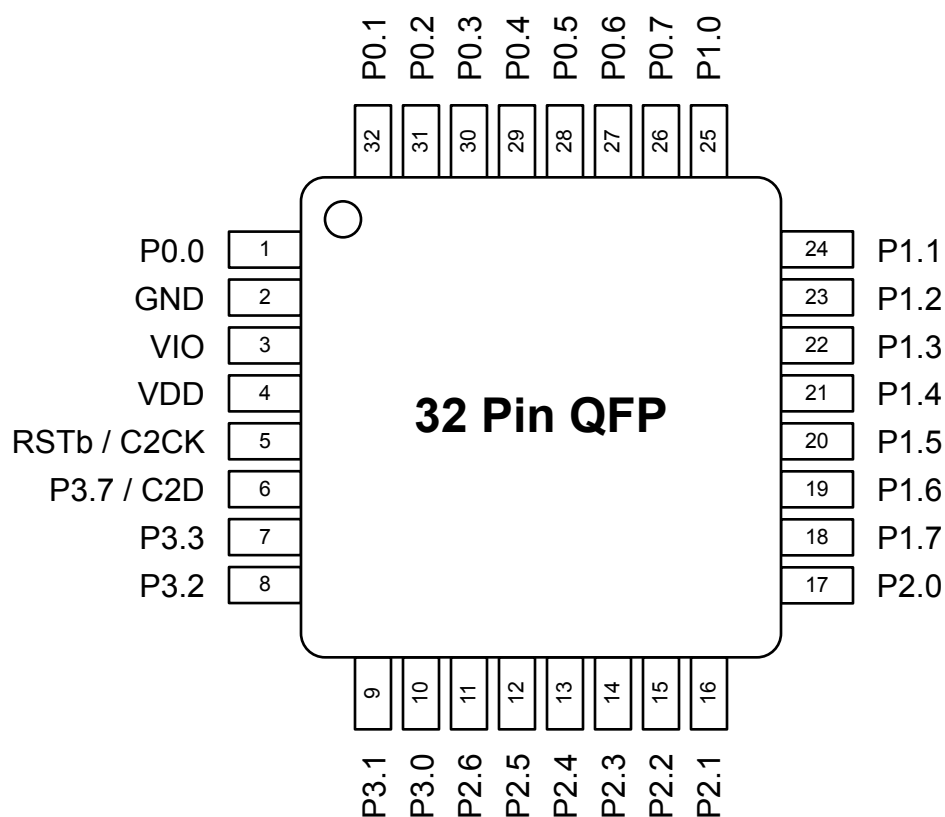


Figure 6.2. EFM8LB1x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8LB1x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
2	GND	Ground			
3	VIO	I/O Supply Power Input			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.13 CMP0P.9 CMP0N.9
19	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU0A.15 CLU1B.12 CLU2A.12	ADC0.12
20	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.11
21	P1.4	Multifunction I/O	Yes	P1MAT.4 CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.10
22	P1.3	Multifunction I/O	Yes	P1MAT.3 CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	ADC0.9
23	P1.2	Multifunction I/O	Yes	P1MAT.2 CLU0A.13 CLU1A.11 CLU2B.10 CLU3A.12 CLU3B.13	ADC0.8 CMP0P.8 CMP0N.8
24	P1.1	Multifunction I/O	Yes	P1MAT.1 CLU0B.12 CLU1B.10 CLU2A.11 CLU3B.12	ADC0.7 CMP0P.7 CMP0N.7

## 6.4 EFM8LB1x-QSOP24 Pin Definitions

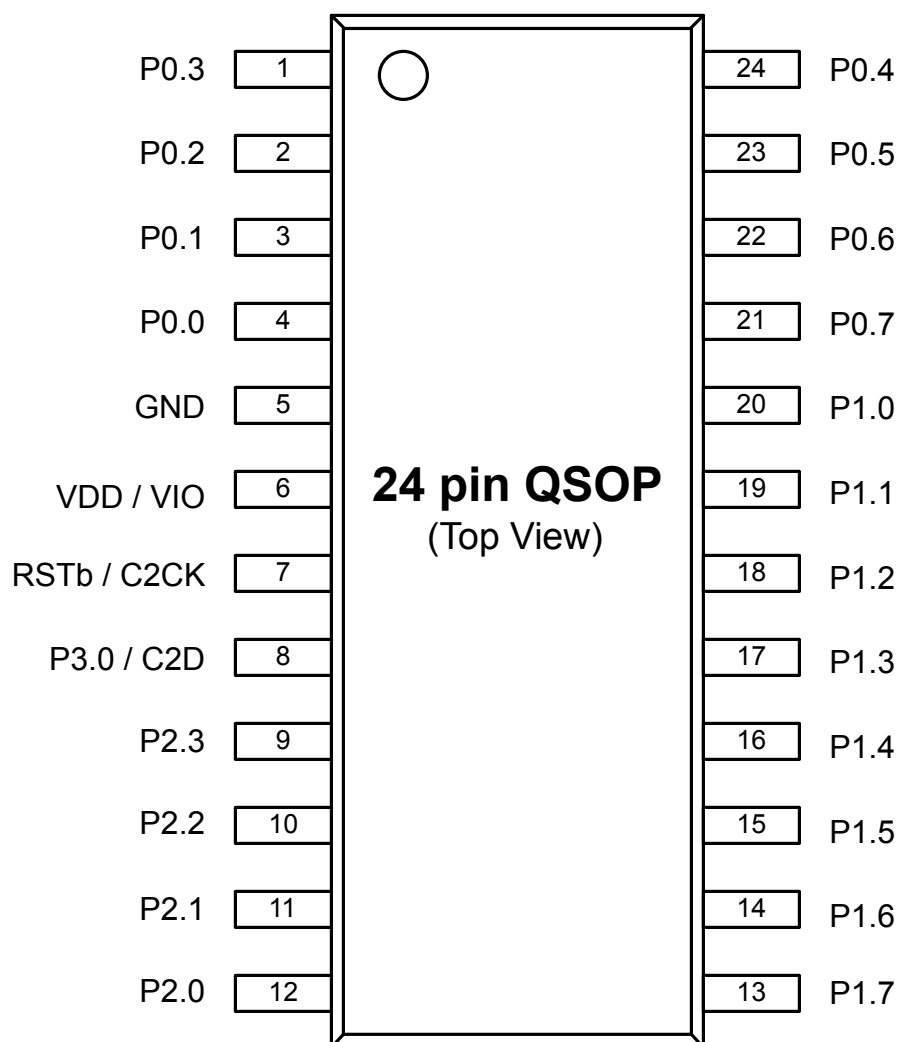


Figure 6.4. EFM8LB1x-QSOP24 Pinout

Table 6.4. Pin Definitions for EFM8LB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
24	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 UART0_TX CLU0A.10 CLU1A.8	ADC0.2 CMP0P.2 CMP0N.2

Dimension	Min	Max
<b>Note:</b> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.</li> <li>3. This Land Pattern Design is based on the IPC-7351 guidelines.</li> <li>4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.</li> <li>5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 <math>\mu</math>m minimum, all the way around the pad.</li> <li>6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>7. The stencil thickness should be 0.125 mm (5 mils).</li> <li>8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.</li> <li>9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad.</li> <li>10. A No-Clean, Type-3 solder paste is recommended.</li> <li>11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol>		

### 7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 8. QFP32 Package Specifications

### 8.1 QFP32 Package Dimensions

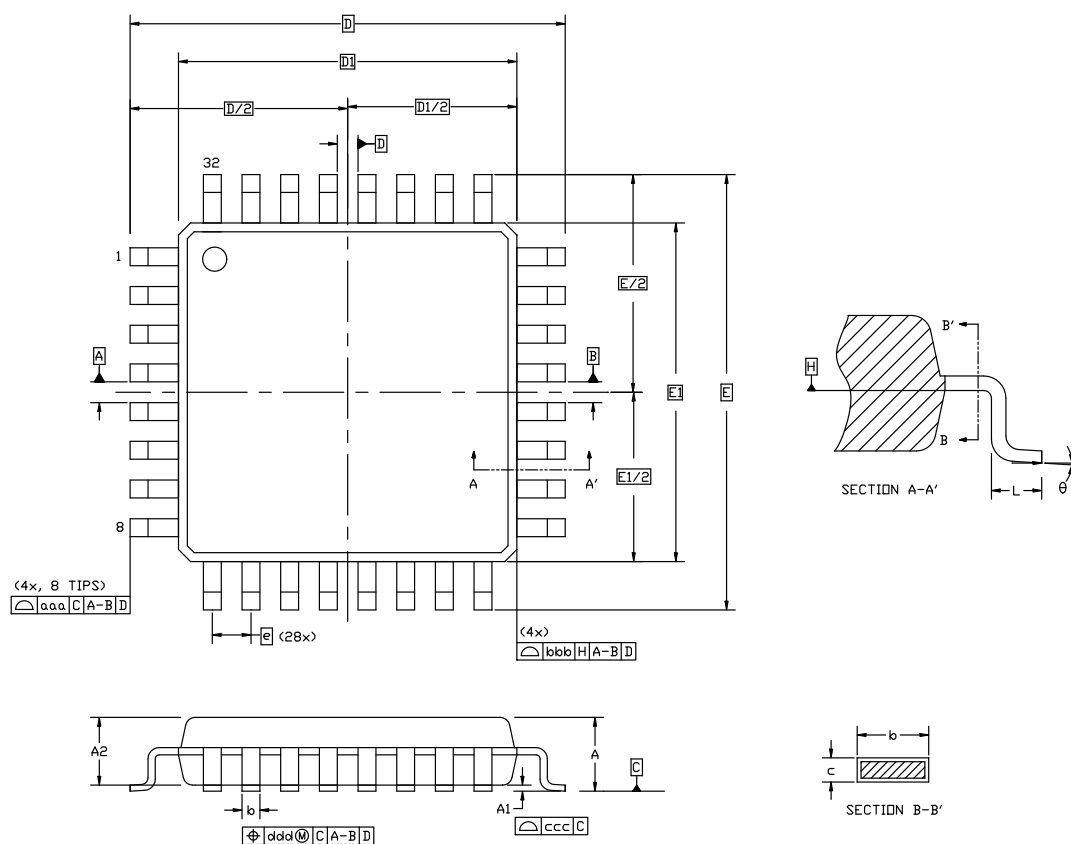


Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.50	0.60	0.70

### 8.3 QFP32 Package Marking

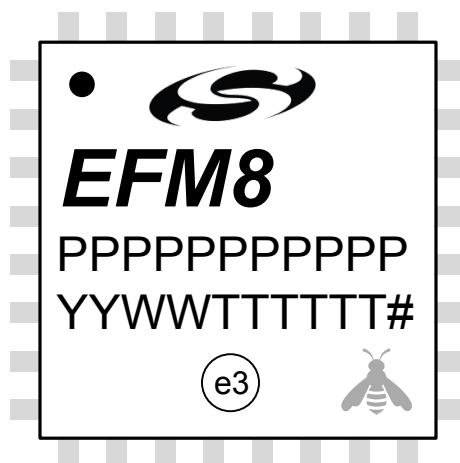


Figure 8.3. QFP32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 9. QFN24 Package Specifications

### 9.1 QFN24 Package Dimensions

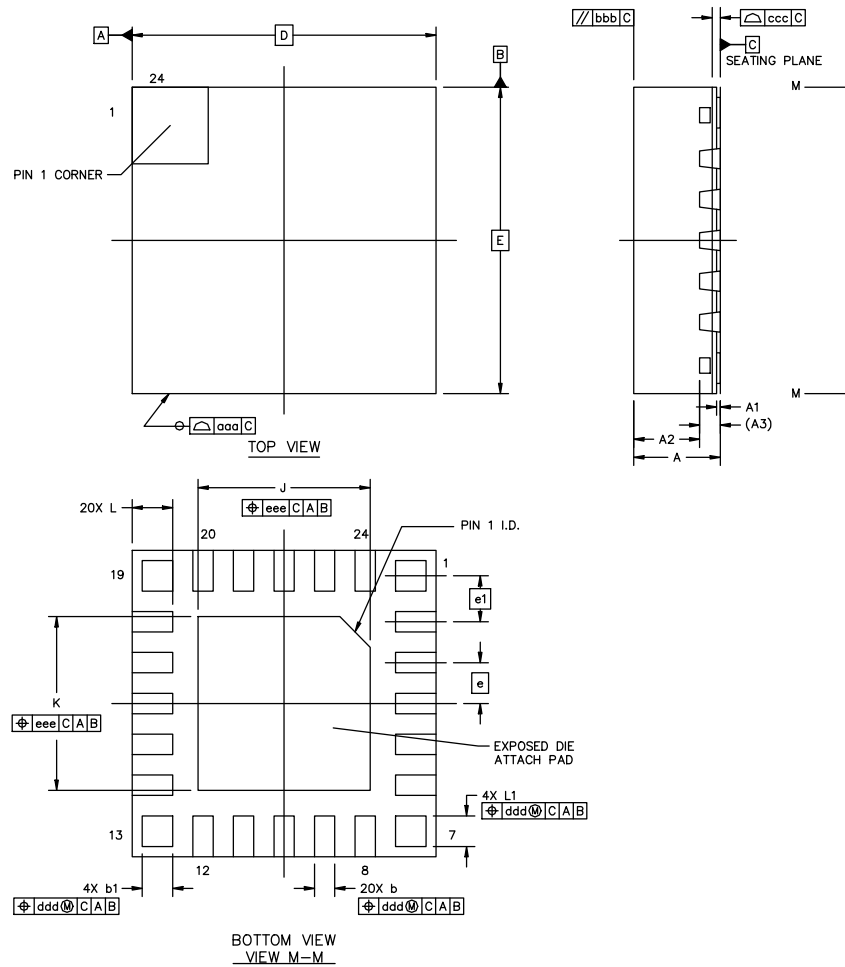


Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D	3.00 BSC		
E	3.00 BSC		



## 10. QSOP24 Package Specifications

### 10.1 QSOP24 Package Dimensions

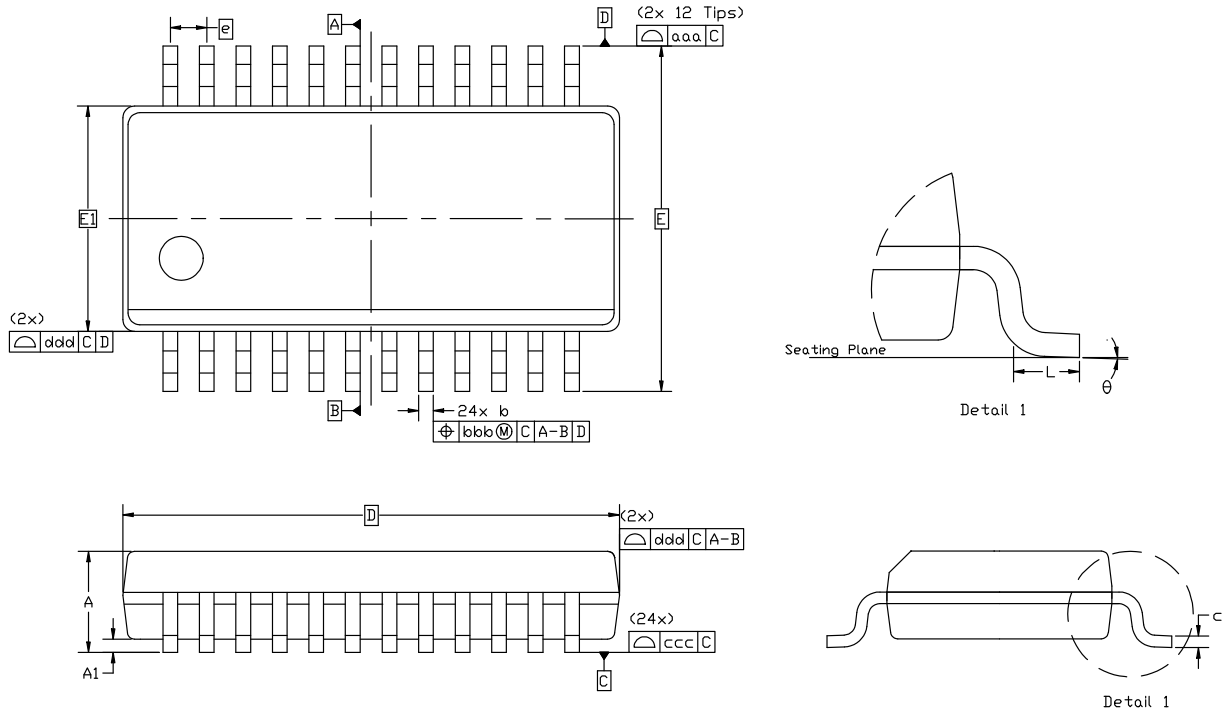
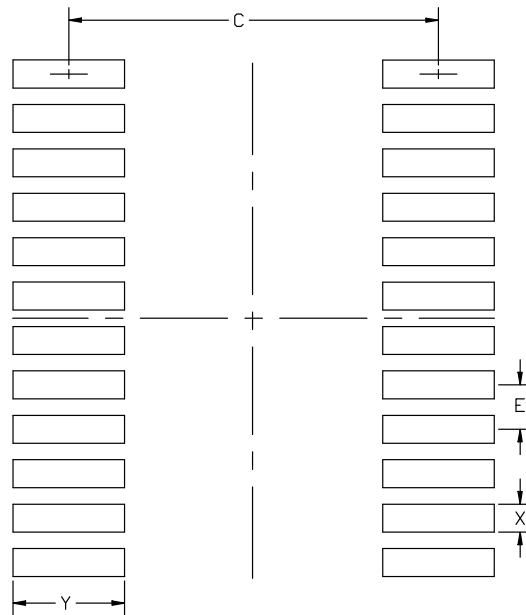


Figure 10.1. QSOP24 Package Drawing

Table 10.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27
theta	0°	—	8°

## 10.2 QSOP24 PCB Land Pattern



**Figure 10.2. QSOP24 PCB Land Pattern Drawing**

**Table 10.2. QSOP24 PCB Land Pattern Dimensions**

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 10.3 QSOP24 Package Marking



Figure 10.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 11. Revision History

### 11.1 Revision 0.1

Initial release.

### 11.2 Revision 0.2

Added information on the bootloader to [3.10 Bootloader](#).

Updated some characterization TBD values.

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