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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	72MHz
Connectivity	I <sup>2</sup> C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x14b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f64e-a-qfn24">https://www.e-xfl.com/product-detail/silicon-labs/efm8lb12f64e-a-qfn24</a>

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Voltage DACs	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8LB12F32E-A-QFN32	32	2304	29	20	4	10	9	Yes	-40 to +105 °C	QFN32
EFM8LB12F32E-A-QFP32	32	2304	28	20	4	10	9	Yes	-40 to +105 °C	QFP32
EFM8LB12F32E-A-QFN24	32	2304	20	12	4	6	6	Yes	-40 to +105 °C	QFN24
EFM8LB12F32E-A-QSOP24	32	2304	21	13	4	6	7	Yes	-40 to +105 °C	QSOP24
EFM8LB11F32E-A-QFN32	32	2304	29	20	2	10	9	Yes	-40 to +105 °C	QFN32
EFM8LB11F32E-A-QFP32	32	2304	28	20	2	10	9	Yes	-40 to +105 °C	QFP32
EFM8LB11F32E-A-QFN24	32	2304	20	12	2	6	6	Yes	-40 to +105 °C	QFN24
EFM8LB11F32E-A-QSOP24	32	2304	21	13	2	6	7	Yes	-40 to +105 °C	QSOP24
EFM8LB11F16E-A-QFN32	16	1280	29	20	2	10	9	Yes	-40 to +105 °C	QFN32
EFM8LB11F16E-A-QFP32	16	1280	28	20	2	10	9	Yes	-40 to +105 °C	QFP32
EFM8LB11F16E-A-QFN24	16	1280	20	12	2	6	6	Yes	-40 to +105 °C	QFN24
EFM8LB11F16E-A-QSOP24	16	1280	21	13	2	6	7	Yes	-40 to +105 °C	QSOP24
EFM8LB10F16E-A-QFN32	16	1280	29	20	0	10	9	Yes	-40 to +105 °C	QFN32
EFM8LB10F16E-A-QFP32	16	1280	28	20	0	10	9	Yes	-40 to +105 °C	QFP32
EFM8LB10F16E-A-QFN24	16	1280	20	12	0	6	6	Yes	-40 to +105 °C	QFN24
EFM8LB10F16E-A-QSOP24	16	1280	21	13	0	6	7	Yes	-40 to +105 °C	QSOP24

## Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

## Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

## 3.6 Communications and Other Digital Peripherals

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 8- or 9-bit data
- Automatic start and stop generation
- Single-byte buffer on transmit and receive

## 3.7 Analog

### 14/12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 14-, 12-, and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 14-bit, 12-bit and 10-bit modes
- Supports an output update rate of up to 1 Msps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated factory-calibrated temperature sensor

### 12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

### Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and  $\pm 20$  mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

### 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

### 3.9 Debugging

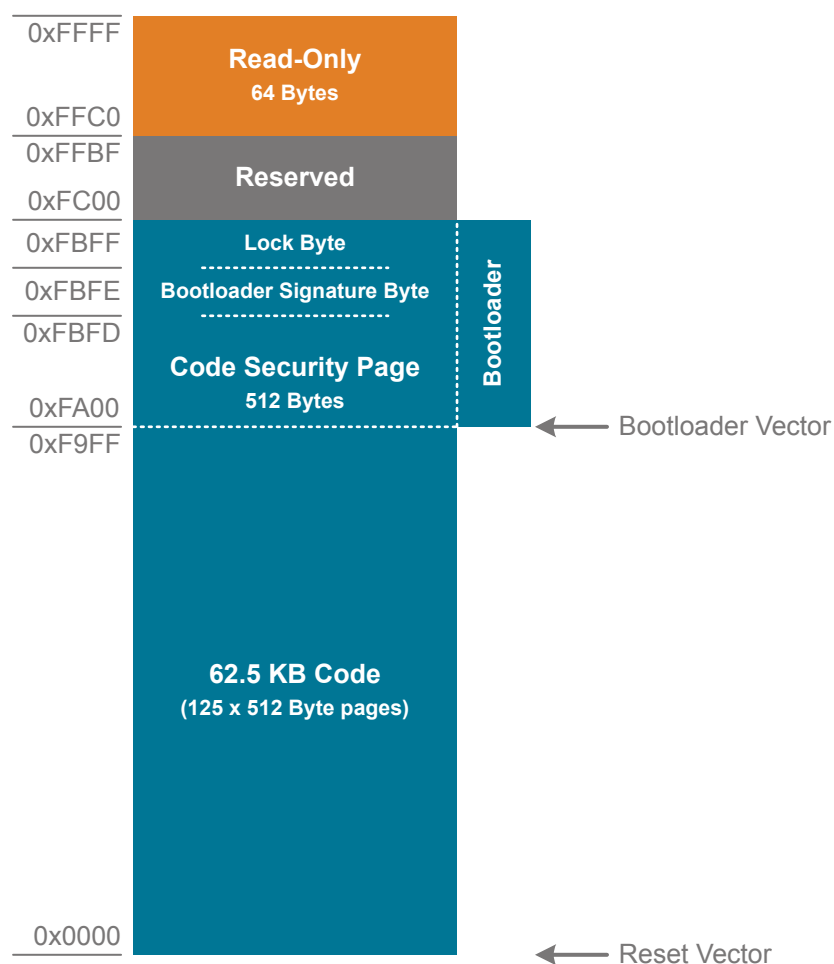
The EFM8LB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

### 3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.



**Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Sensor	$I_{TSENSE}$		—	75	120	$\mu A$
Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3) <sup>6</sup>	$I_{DAC}$		—	125	—	$\mu A$
Comparators (CMP0, CMP1)	$I_{CMP}$	CPMD = 11	—	0.5	—	$\mu A$
		CPMD = 10	—	3	—	$\mu A$
		CPMD = 01	—	10	—	$\mu A$
		CPMD = 00	—	25	—	$\mu A$
Comparator Reference	$I_{CPREF}$		—	TBD	—	$\mu A$
Voltage Supply Monitor (VMON0)	$I_{VMON}$		—	15	20	$\mu A$

**Note:**

1. Currents are additive. For example, where  $I_{DD}$  is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in low power mode. Total ADC + Reference current will depend on sampling rate.
6. DAC supply current for each enabled DA and not including external load on pin.

### 4.1.3 Reset and Supply Monitor

**Table 4.3. Reset and Supply Monitor**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	$V_{VDDM}$		1.85	1.95	2.1	V
Power-On Reset (POR) Threshold	$V_{POR}$	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	$t_{RMP}$	Time to $V_{DD} > 2.2$ V	10	—	—	$\mu s$
Reset Delay from POR	$t_{POR}$	Relative to $V_{DD} > V_{POR}$	3	10	31	ms
Reset Delay from non-POR source	$t_{RST}$	Time between release of reset source and code execution	—	50	—	$\mu s$
RST Low Time to Generate Reset	$t_{RSTL}$		15	—	—	$\mu s$
Missing Clock Detector Response Time (final rising edge to reset)	$t_{MCD}$	$F_{SYSCLK} > 1$ MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	$F_{MCD}$		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	$t_{MON}$		—	2	—	$\mu s$

## 4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N <sub>bits</sub>	14 Bit Mode	14			Bits
		12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f <sub>S</sub>	14 Bit Mode	—	—	900	ksps
		12 Bit Mode	—	—	1	Msps
		10 Bit Mode	—	—	1.125	Msps
Throughput Rate (Low Power Mode)	f <sub>S</sub>	14 Bit Mode	—	—	TBD	ksps
		12 Bit Mode	—	—	TBD	ksps
		10 Bit Mode	—	—	TBD	ksps
Tracking Time	t <sub>TRK</sub>	High Speed Mode	217.8 <sup>1</sup>	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t <sub>PWR</sub>		1.2	—	—	μs
SAR Clock Frequency	f <sub>SAR</sub>	High Speed Mode	—	—	18.36	MHz
		Low Power Mode	—	—	TBD	MHz
Conversion Time <sup>2</sup>	t <sub>CNV</sub>	14-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.	0.81			μs
		12-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.	0.7			μs
		10-Bit Conversion, SAR Clock =18 MHz, System Clock = 72 MHz.	0.59			μs
Sample/Hold Capacitor	C <sub>SAR</sub>	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C <sub>IN</sub>	High Quality Input	—	TBD	—	pF
		Normal Input	—	20	—	pF
Input Mux Impedance	R <sub>MUX</sub>	High Quality Input	—	TBD	—	Ω
		Normal Input	—	550	—	Ω
Voltage Reference Range	V <sub>REF</sub>		1	—	V <sub>IO</sub>	V
Input Voltage Range <sup>3</sup>	V <sub>IN</sub>	Gain = 1	0	—	V <sub>REF</sub> / Gain	V



### 4.1.13 Comparators

Table 4.13. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	$t_{RESP0}$	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	$t_{RESP3}$	+100 mV Differential	—	1.5	—	μs
		-100 mV Differential	—	3.5	—	μs
Positive Hysteresis Mode 0 (CPMD = 00)	$HYS_{CP+}$	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	$HYS_{CP-}$	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	$HYS_{CP+}$	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	$HYS_{CP-}$	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	$HYS_{CP+}$	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	$HYS_{CP-}$	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	$HYS_{CP+}$	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

#### 4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	$V_{OH}$	$I_{OH} = -7 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -3.3 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.8 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (High Drive)	$V_{OL}$	$I_{OL} = 13.5 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 7 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 3.6 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output High Voltage (Low Drive)	$V_{OH}$	$I_{OH} = -4.75 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	$V_{IO} - 0.7$	—	—	V
		$I_{OH} = -2.25 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	$V_{IO} \times 0.8$	—	—	V
		$I_{OH} = -1.2 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Output Low Voltage (Low Drive)	$V_{OL}$	$I_{OL} = 6.5 \text{ mA}$ , $V_{IO} \geq 3.0 \text{ V}$	—	—	0.6	V
		$I_{OL} = 3.5 \text{ mA}$ , $2.2 \text{ V} \leq V_{IO} < 3.0 \text{ V}$	—	—	$V_{IO} \times 0.2$	V
		$I_{OL} = 1.8 \text{ mA}$ , $1.71 \text{ V} \leq V_{IO} < 2.2 \text{ V}$				
Input High Voltage	$V_{IH}$		$0.7 \times V_{IO}$	—	—	V
Input Low Voltage	$V_{IL}$		—	—	$0.3 \times V_{IO}$	V
Pin Capacitance	$C_{IO}$		—	7	—	pF
Weak Pull-Up Current ( $V_{IN} = 0 \text{ V}$ )	$I_{PU}$	$V_{DD} = 3.6$	-30	-20	-10	$\mu\text{A}$
Input Leakage (Pullups off or Analog)	$I_{LK}$	$\text{GND} < V_{IN} < V_{IO}$	TBD	—	TBD	$\mu\text{A}$
Input Leakage Current with $V_{IN}$ above $V_{IO}$	$I_{LK}$	$V_{IO} < V_{IN} < V_{IO} + 2.5 \text{ V}$ Any pin except P3.0, P3.1, P3.2, or P3.3	0	5	150	$\mu\text{A}$

## 4.2 Thermal Conditions

**Table 4.16. Thermal Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$\theta_{JA}$	QFN24 Packages	—	TBD	—	°C/W
		QFN32 Packages	—	TBD	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QSOP24 Packages	—	65	—	°C/W
<b>Note:</b> 1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

## 4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.17 Absolute Maximum Ratings on page 27](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.17. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	$T_{BIAS}$		-55	125	°C
Storage Temperature	$T_{STG}$		-65	150	°C
Voltage on VDD	$V_{DD}$		GND-0.3	4.2	V
Voltage on VIO <sup>2</sup>	$V_{IO}$		GND-0.3	$V_{DD}+0.3$	V
Voltage on I/O pins or RSTb, excluding P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	$V_{IN}$	$V_{IO} > \text{TBD V}$	GND-0.3	TBD	V
		$V_{IO} < \text{TBD V}$	GND-0.3	TBD	V
Voltage on P2.0-P2.3 (QFN24 and QSOP24) or P3.0-P3.3 (QFN32 and QFP32)	$V_{IN}$		GND-0.3	$V_{DD}+0.3$	V
Total Current Sunk into Supply Pin	$I_{VDD}$		—	400	mA
Total Current Sourced out of Ground Pin	$I_{GND}$		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	$I_{IO}$		-100	100	mA
<b>Note:</b> 1. Exposure to maximum rating conditions for extended periods may affect device reliability. 2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.					

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2
31	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU0OUT CLU0A.9 CLU2B.8 CLU3A.8	XTAL1 ADC0.1 CMP0P.1 CMP0N.1
32	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0B.8 CLU2A.9 CLU3B.9	ADC0.0 CMP0P.0 CMP0N.0 AGND

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0 CLU0A.8 CLU2A.8 CLU3B.8	VREF
3	GND	Ground			
4	VDD / VIO	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P3.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P2.3	Multifunction I/O	Yes	P2MAT.3 CLU1B.15 CLU2B.15 CLU3A.15	DAC3
8	P2.2	Multifunction I/O	Yes	P2MAT.2 CLU1A.15 CLU2B.14 CLU3A.14	DAC2
9	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
10	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
11	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5

## 6.4 EFM8LB1x-QSOP24 Pin Definitions

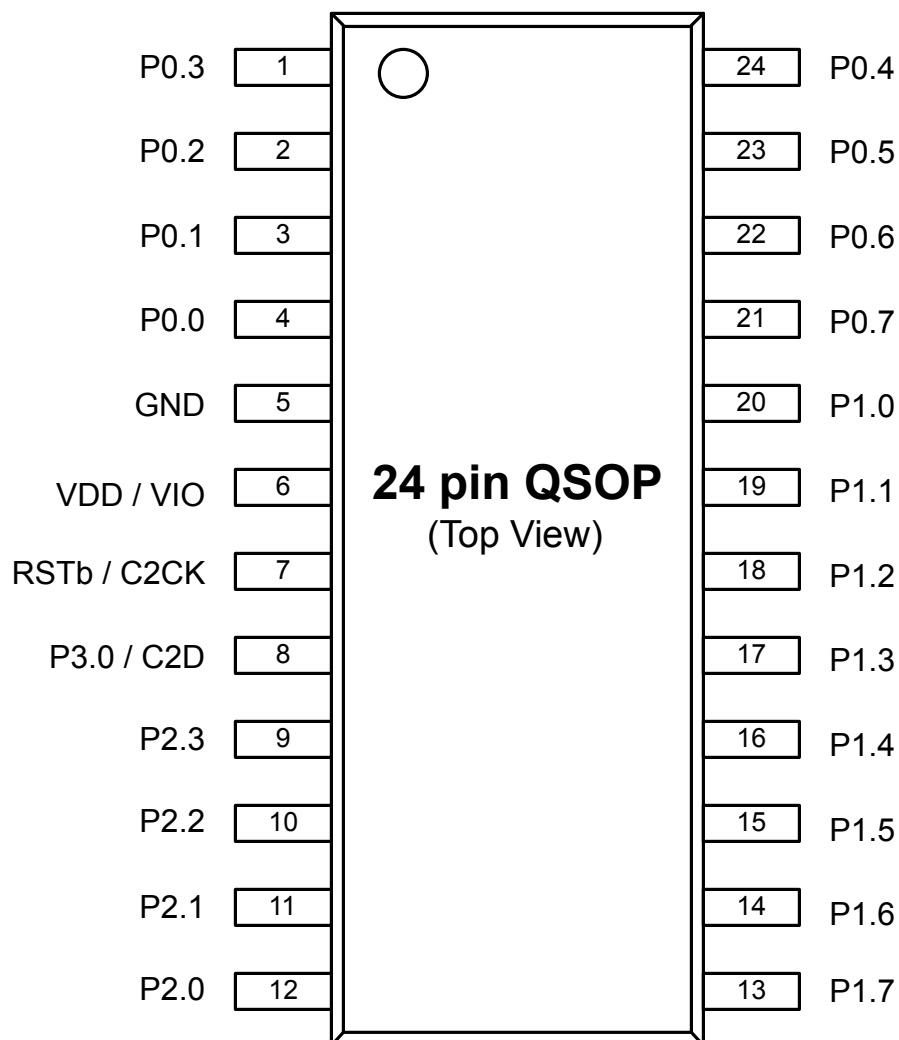


Figure 6.4. EFM8LB1x-QSOP24 Pinout

Table 6.4. Pin Definitions for EFM8LB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU0B.9 CLU2B.10 CLU3A.9	XTAL2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
11	P2.1	Multifunction I/O	Yes	P2MAT.1 CLU1B.14 CLU2A.15 CLU3B.15	DAC1
12	P2.0	Multifunction I/O	Yes	P2MAT.0 CLU1A.14 CLU2A.14 CLU3B.14	DAC0
13	P1.7	Multifunction I/O	Yes	P1MAT.7 CLU0B.15 CLU1B.13 CLU2A.13	ADC0.12 CMP1P.6 CMP1N.6
14	P1.6	Multifunction I/O	Yes	P1MAT.6 CLU3OUT CLU0A.15 CLU1B.12 CLU2A.12	ADC0.11 CMP1P.5 CMP1N.5
15	P1.5	Multifunction I/O	Yes	P1MAT.5 CLU2OUT CLU0B.14 CLU1A.13 CLU2B.13 CLU3B.11	ADC0.10 CMP1P.4 CMP1N.4
16	P1.4	Multifunction I/O	Yes	P1MAT.4 I2C0_SCL CLU0A.14 CLU1A.12 CLU2B.12 CLU3B.10	ADC0.9 CMP1P.3 CMP1N.3
17	P1.3	Multifunction I/O	Yes	P1MAT.3 I2C0_SDA CLU0B.13 CLU1B.11 CLU2B.11 CLU3A.13	CMP1P.2 CMP1N.2

## 7. QFN32 Package Specifications

### 7.1 QFN32 Package Dimensions

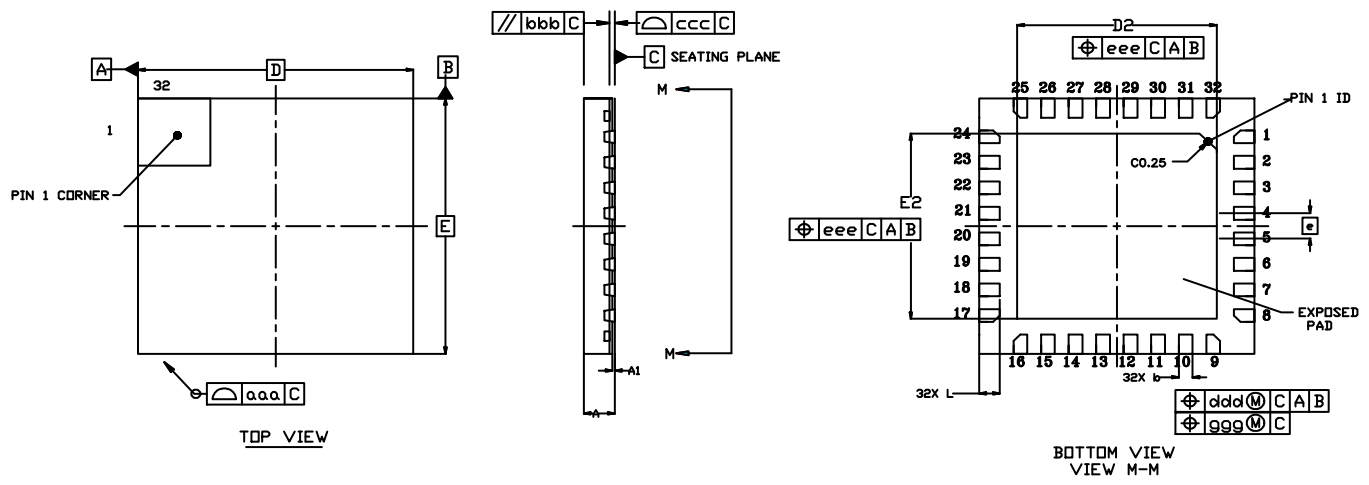


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.035	0.05
b	0.15	0.20	0.25
D	4.00 BSC.		
D2	2.80	2.90	3.00
e	0.40 BSC.		
E	4.00 BSC.		
E2	2.80	2.90	3.00
L	0.20	0.30	0.40
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10
ggg	—	—	0.05



Dimension	Min	Max
<b>Note:</b> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.</li> <li>3. This Land Pattern Design is based on the IPC-7351 guidelines.</li> <li>4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.</li> <li>5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 <math>\mu</math>m minimum, all the way around the pad.</li> <li>6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>7. The stencil thickness should be 0.125 mm (5 mils).</li> <li>8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.</li> <li>9. A 2 x 2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center pad.</li> <li>10. A No-Clean, Type-3 solder paste is recommended.</li> <li>11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol>		

### 7.3 QFN32 Package Marking



Figure 7.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 8.2 QFP32 PCB Land Pattern

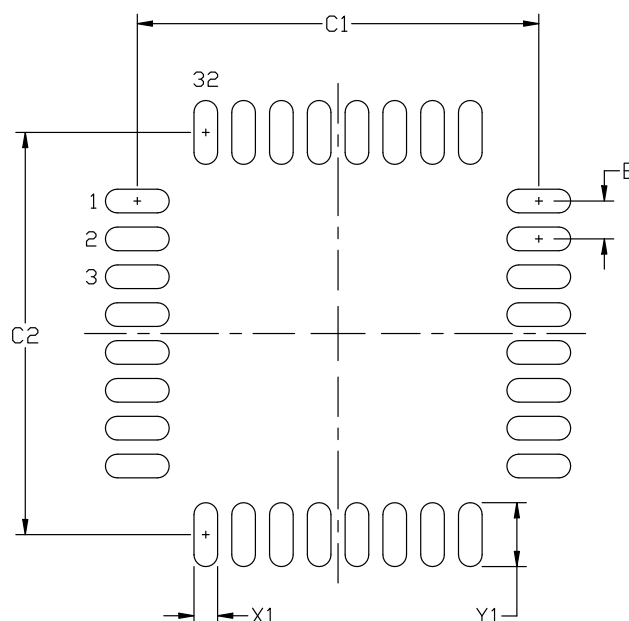


Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.55	
Y1	1.5	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

### 8.3 QFP32 Package Marking

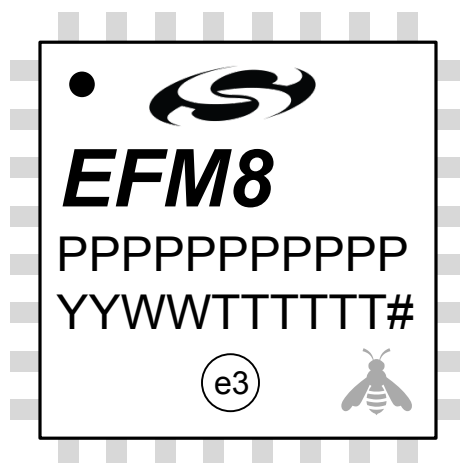


Figure 8.3. QFP32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 9. QFN24 Package Specifications

### 9.1 QFN24 Package Dimensions

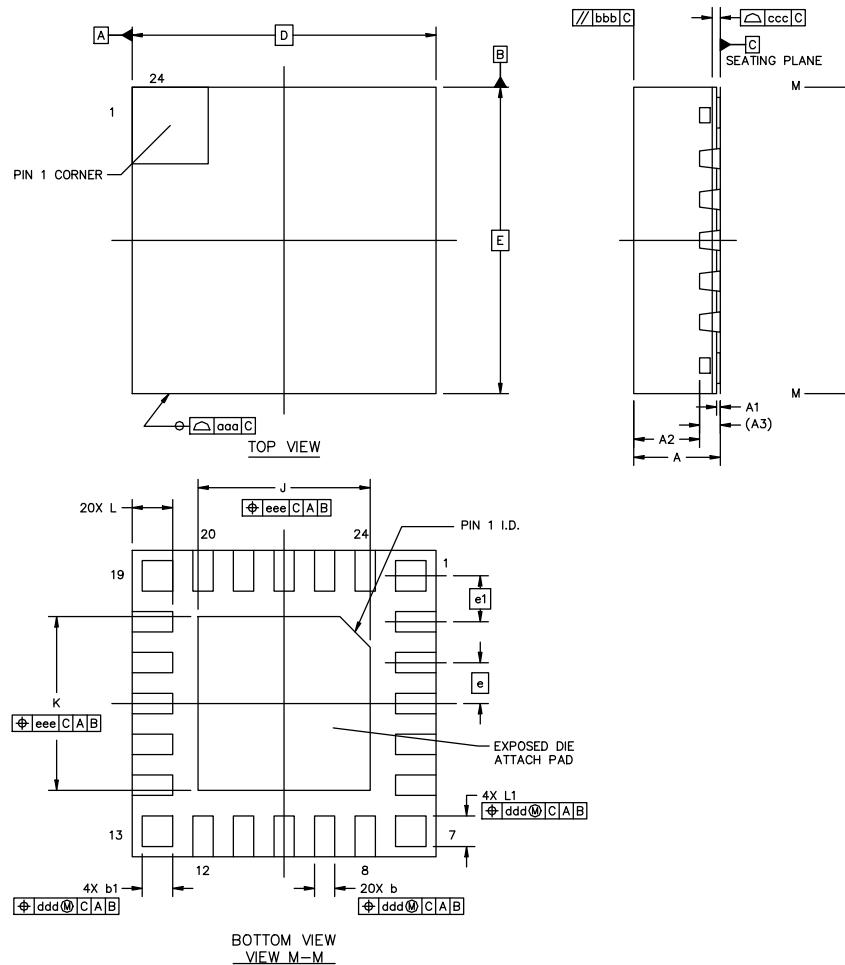
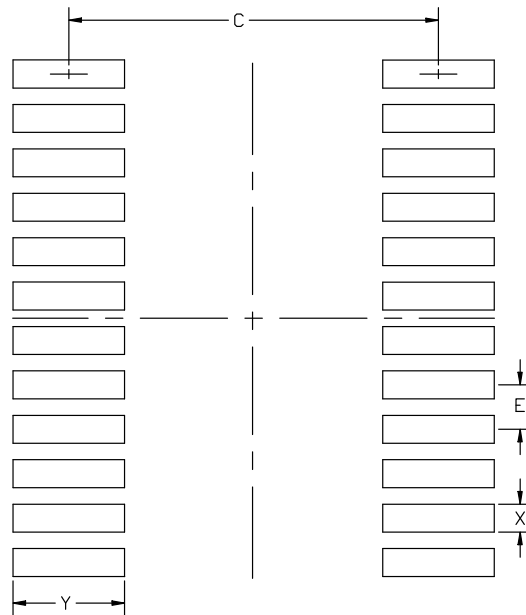


Figure 9.1. QFN24 Package Drawing

Table 9.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.8	0.85	0.9
A1	0.00	—	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
D	3.00 BSC		
E	3.00 BSC		

## 10.2 QSOP24 PCB Land Pattern



**Figure 10.2. QSOP24 PCB Land Pattern Drawing**

**Table 10.2. QSOP24 PCB Land Pattern Dimensions**

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.