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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1507-e-p

Pin	Pin name	Pin function	Description
40 to 44	P0.21 to P0.25	Digital I/O	General purpose I/O pin.
45	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O pin. ADC/LPCOMP input 0. Connection for 32.768 kHz crystal.
46	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O pin. ADC/LPCOMP input 1. Connection for 32.768 kHz crystal or external 32.768 kHz clock reference.
47, 48	P0.28 and P0.29	Digital I/O	General purpose I/O pin.

1. The exposed center pad of the QFN48 package must be connected to ground for proper device operation.

Table 1 *Pin functions QFN48 packet*

2.2.2 CDAB WLCSP ball assignment and functions

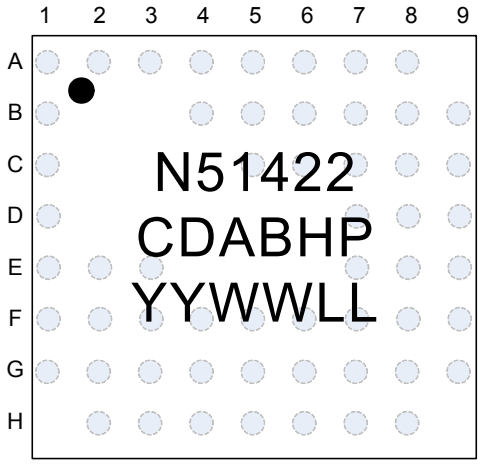

Figure 3 *Ball assignment CDAB packet (top side view)*

3.2.1 Code organization

Chip variant	Code size	Page size	No of pages
nRF51422-QFAA nRF51422-CEAA	256 kB	1024 byte	256
nRF51422-QFAB nRF51422-CDAB	128 kB	1024 byte	128
nRF51422-QFAC nRF51422-CFAC	256 kB	1024 byte	256

Table 4 *Code organization*

3.2.2 RAM organization

RAM is divided into blocks for separate power management which is controlled by the POWER System Block. Each block is divided into two 4 kByte RAM sections with separate RAM AHB slaves.
Please see the *nRF51 Series Reference Manual* for more information.

Chip variant	RAM size	Block	Size
nRF51422-QFAA nRF51422-CEAA	16 kB	Block0 Block1	8 kB 8 kB
nRF51422-QFAB nRF51422-CDAB	16 kB	Block0 Block1	8 kB 8 kB
nRF51422-QFAC nRF51422-CFAC	32 kB	Block0 Block1 Block2 Block3	8 kB 8 kB 8 kB 8 kB

Table 5 *RAM organization*

How to organize the use of the RAM

For the best performance we recommend the following use of the RAM AHB slaves (Note that the Crypto consists of CCM, ECB, and AAR modules):

- If the Radio and Crypto buffers together are larger in size than one RAM section, the buffers should be separated so the memory used by the Radio is in one RAM section while the memory used by the Crypto is in another RAM section.
- The sections used by CODE should not be combined with sections used by the Radio, Crypto, or SPI.
- The Stack and Heap should be placed at the top section and should not be combined with sections used by the Radio, Crypto, or SPI.

3.4.2.2 System ON mode

In system ON mode the system is fully operational and the CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending on the sub-power mode selected.

There are two sub-power modes:

- Low power
- Constant latency

Low Power

In Low Power mode the automatic power management system is optimized to save power. This is done by keeping as much as possible of the system powered down. The cost of this is that you will have varying CPU wakeup latency and PPI task response.

The CPU wakeup latency will be affected by the startup time of the 1V7 regulator. The PPI task response will vary depending on the resources required by the peripheral where the task originated.

The resources that could be involved are:

- 1V7 with the startup time $\mathbf{t_{1V7}}$
- 1V2 with the startup time $\mathbf{t_{1V2}}$
- One of the following clock sources
  - RC16 with the startup time $\mathbf{t_{START,RC16}}$
  - XO16M/XO32M with the startup time the clock management system $\mathbf{t_{XO}}$[1]

Constant Latency

In Constant Latency mode the system is optimized towards keeping the CPU latency and the PPI task response constant and at a minimum. This is secured by forcing a set of base resources on while in sleep mode. The cost is that the system will have higher power consumption.

The following resources are kept active while in sleep mode:

- 1V7 regulator with the standby current of I_{1V7}
- 1V2 regulator. Here the current consumption is specified in combination with the clock source
- One of the following clock sources:
  - RC16 with the standby current of $I_{1V2RC16}$
  - XO16M with the standby current of $I_{1V2XO16}$
  - XO32M with the standby current of $I_{1V2XO32}$

1. For the clock source XO16M and XO32M we assume that the crystal is already running (standby). This will give an increase of the power consumption in sleep mode given by $\mathbf{I_{STBY,X16M}}$ / $\mathbf{I_{STBY,X32M}}$.

4.5 AES CCM Mode Encryption (CCM)

Cipher Block Chaining - Message Authentication Code (CCM) Mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication.

Note: The CCM terminology "Message Authentication Code (MAC)" is called the "Message Integrity Check (MIC)" in *Bluetooth* terminology and this document and the *nRF51 Series Reference Manual* are consistent with *Bluetooth* terminology.

The CCM block generates an encrypted keystream, applies it to the input data using the XOR operation, and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously, as described in the *nRF51 Series Reference Manual*. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the Radio. All operations can complete within the packet RX or TX time.

CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF RFC3610, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in the NIST Special Publication 800-38C. The *Bluetooth* Core Specification v4.0 describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

4.6 Accelerated Address Resolver (AAR)

Accelerated Address Resolver is a cryptographic support function to implement the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core Specification* v4.1. "Resolvable Private Address Generation" should be achieved using ECB and is not supported by AAR. The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address.

The AAR block enables real-time address resolution on incoming packets when configured according to the description in the *nRF51 Series Reference Manual*. This allows real-time packet filtering (whitelisting) using a list of known shared secrets (Identity Resolving Keys (IRK) in *Bluetooth*).

The following table outlines the properties of the AAR.

Instance	Number of IRKs supported for simultaneous resolution
AAR	8

***Table 14** AAR properties*

4.7 Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers derived from thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

4.8 Watchdog Timer (WDT)

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

8.1.2 16 MHz crystal oscillator (16M XOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{NOM,X16M}$	Crystal frequency.			16		MHz	N/A
$f_{TOL,X16M,ANT}$	Frequency tolerance, ANT.[1]				±50[2]	ppm	N/A
$f_{TOL,X16M,BLE}$	Frequency tolerance, *Bluetooth* low energy applications.[1]				±40[2]	ppm	N/A
$R_{S,X16M}$	Equivalent series resistance.	C0 ≤ 7 pF, $C_{L,MAX}$ ≤ 16 pF C0 ≤ 5 pF, $C_{L,MAX}$ ≤ 12 pF C0 ≤ 3 pF, $C_{L,MAX}$ ≤ 12 pF		50 75 100	100 150 200	Ω Ω Ω	N/A N/A N/A
$P_{D,X16M}$	Drive level.				100	µW	N/A
C_{pin}	Input capacitance on XC1 and XC2 pads.			4		pF	1
I_{X16M}	Run current for 16 MHz crystal oscillator.	SMD 2520 CL = 8 pF		470[3]		µA	1
$I_{X16M,1M}$	Run current for the 16 MHz crystal oscillator when used only for a Timer at 1 MHz or less.	SMD 2520 CL = 8pF		250[3]		µA	1
$I_{STBY,X16M}$	Standby current for 16 MHz crystal oscillator.[4]	SMD 2520 CL = 8 pF		25		µA	1
$I_{START,XOSC}$	Startup current for 16 MHz crystal oscillator.			1.1		mA	3
$t_{START,XOSC}$	Startup time for 16 MHz crystal oscillator.	SMD 2520 CL = 8 pF		400	500[5]	µs	2
$t_{START,X16M}$	Total startup time ($t_{START,XOSC}$ + debounce period).[6]	SMD 2520 CL = 8 pF		800		µs	1

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See ***Table 38*** on page 51.
2. Includes initial tolerance of the crystal, drift over temperature, aging, and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 16M, meaning there is no clock management active (see ***Table 33*** on page 48). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.

Table 22 *16 MHz crystal oscillator*

8.2 Power management

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
V_{POF}	Nominal power level warning thresholds (falling supply voltage).	Accuracy as defined by V_{TOL}		2.1 2.3 2.5 2.7		V	2
V_{TOL}	Threshold voltage tolerance.				±5	%	3
V_{HYST}	Threshold voltage hysteresis.	V_{POF} = 2.1 V V_{POF} = 2.3 V V_{POF} = 2.5 V V_{POF} = 2.7 V		46 62 79 100		mV	3

Table 28 *Power Fail Comparator*

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$t_{HOLDRESETNORMAL}$	Hold time for reset pin when doing a pin reset.[1]	0.2			µs	1
$t_{HOLDRESETDEBUG}$	Hold time for reset pin when doing a pin reset during debug.[1,2]	100			µs	1

1. SWDCLK pin must be kept low during reset.
2. Bit 0 in the RESET register in the power management module must be set to 1 to enable reset during debug.

Table 29 *Pin Reset*

Power on reset time (t_{POR}) is the time from when the supply starts rising to when the device comes out of reset and the CPU starts. The time increases with, and is inclusive of, supply rise time from 0 V to VDD. ***Table 30*** gives t_{POR} for a number of supply rise times, simulated with a linear ramp from 0 V to VDD, over the supply voltage range 1.8 V to 3.6 V.

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$t_{POR, 10\ \mu s}$	Power on reset time, 10 µs rise time (0 V to VDD).		0.7	2.4	19	ms	1
$t_{POR, 1\ ms}$	Power on reset time, 10 µs rise time (0 V to VDD).		1.7	3.4	20	ms	1
$t_{POR, 10\ ms}$	Power on reset time, 10 µs rise time (0 V to VDD).		11	12	28	ms	1
$t_{POR, 100\ ms}$	Power on reset time, 10 µs rise time (0 V to VDD).		68	101	115	ms	1

Table 30 *Power on reset time*

The data in ***Figure 10*** and ***Table 31*** show measured $t_{\_POR}$ data. Measurements were taken using the reference circuit shown in ***Section 11.3.1 "QFAA QFN48 schematic with internal LDO setup"*** on page 79 with the given supply voltage and temperature conditions.

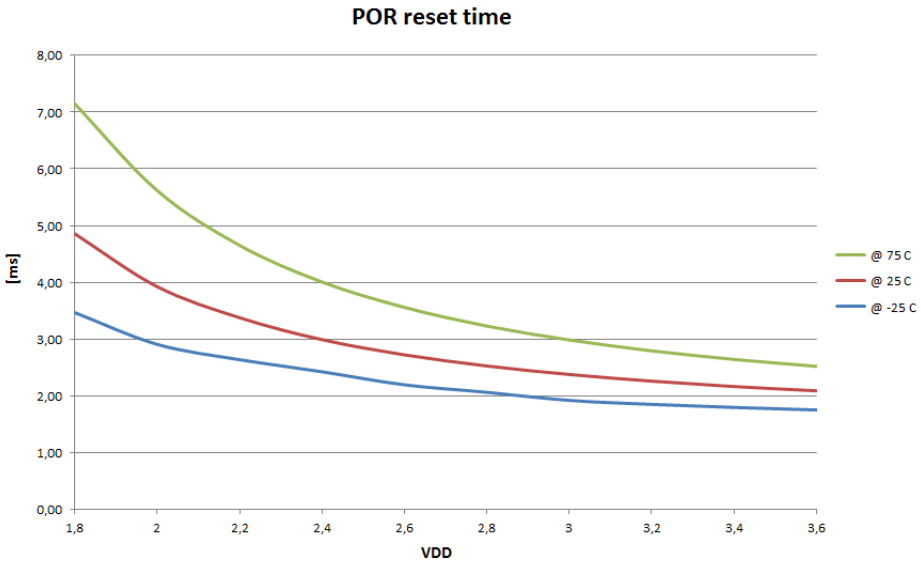

Figure 10 *Power on reset time (Test level 2)*

VDD	Rise Time from 10% to 90% of VDD
1.8	570 µs
3.0	605 µs
3.6	635 µs

Table 31 *Supply rise time at sample voltages for the measured data shown in* ***Figure 10****.*

8.10 I2C compatible Two Wire Interface (TWI) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{2W100K}	Run current for TWI at 100 kbps.			380		µA	1
I_{2W400K}	Run current for TWI at 400 kbps.			400		µA	1
f_{2W}	Bit rates for TWI.		100		400	kbps	N/A
$t_{TWI,START}$	Time from STARTRX/STARTTX task is given until start condition.	Low power mode.[1] Constant latency mode.[1]		3 1	4.4	µs	1

1. For more information on how to control the sub power modes, see the *nRF51 Series Reference Manual*.

Table 48 *TWI specifications*

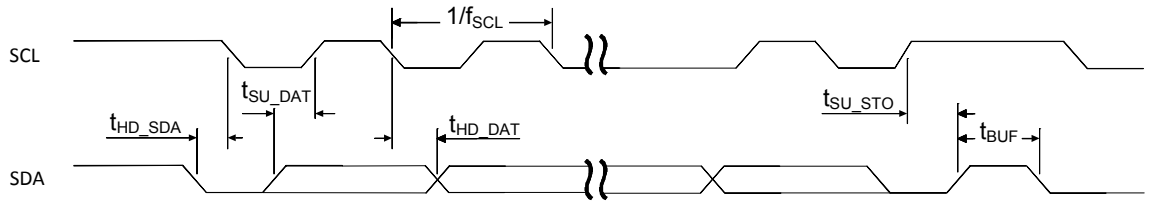

Figure 14 *SCL/SDA timing*

Symbol	Description	Standard Min.	Standard Max.	Fast Min.	Fast Max.	Units	Test level
f_{SCL}	SCL clock frequency.		100		400	kHz	1
t_{HD_STA}	Hold time for START and repeated START condition.	5200		1300		ns	1
t_{SU_DAT}	Data setup time before positive edge on SCL.	300		300		ns	1
t_{HD_DAT}	Data hold time after negative edge on SCL.	300		300		ns	1
t_{SU_STO}	Setup time from SCL goes high to STOP condition.	5200		1300		ns	1
t_{BUF}	Bus free time between STOP and START conditions.	4700		1300		ns	1

Table 49 *TWI timing parameters*

8.12 Analog to Digital Converter (ADC) specifications

Note: HFCLK XOSC is required to get the stated ADC accuracy.

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
DNL_{10b}	Differential non-linearity (10 bit mode).			< 1		LSB	2
INL_{10b}	Integral non-linearity (10 bit mode).			2		LSB	2
V_{OS}	Offset error.		-2		+2	%	2
e_G	Gain error.	1	-2		+2	%	2
V_{REF_VBG}	Internal Band Gap reference voltage (VBG).			1.20 V		V	2
$V_{REF\_VBG\_ERR}$	Internal Band Gap reference voltage error.		-1.5		+1.5	%	2
$TC_{REF\_VBG\_DRIFT}$	Internal Band Gap reference voltage drift.		-200		+200	ppm/°C	2
V_{REF_EXT}	External reference voltage (AREF0/1).		0.83	1.2	1.3	V	1
$V_{REF\_VDD\_LIM}$	Limited supply voltage range for ADC using VDD with prescaler as the reference. CONFIG.REFSEL = SupplyOneHalfPrescaling CONFIG.REFSEL = SupplyOneThirdPrescaling		1.7 2.5		2.6 3.6	V V	1 1
t_{ADC10b}	Time required to convert a single sample in 10 bit mode.			68		µs	1
t_{ADC9b}	Time required to convert a single sample in 9 bit mode.			36		µs	1
t_{ADC8b}	Time required to convert a single sample in 8 bit mode.			20		µs	1
I_{ADC}	Current drawn by ADC during conversion.			260		µA	1
ADC_ERR_1V8	Absolute error when used for battery measurement at 1.8 V, 2.2 V, 2.6 V, 3.0 V, and 3.4 V.	2		3		LSB	2
ADC_ERR_2V2				2		LSB	2
ADC_ERR_2V6				1		LSB	2
ADC_ERR_3V0				1		LSB	2
ADC_ERR_3V4				1		LSB	2

1. Source impedance less than 5 kΩ.
2. Internal reference, input from VDD/3, 10 bit mode.

Table 51 *Analog to Digital Converter (ADC) specifications*

8.22 Non-Volatile Memory Controller (NVMC) specifications

Flash write is done by executing a program that writes one word (32 bit) consecutively after the other to the flash memory.

The program doing the flash writes could be set up to run from flash or from RAM. The timing of one flash write operation depends on whether the next instructions following the flash write will be fetched from flash or from RAM. Any fetch from flash done before the write operation is finished will give $t_{WRITE,FLASH}$ timing.

The flash memory is organized in 256 byte rows starting at CODE and UICR start address. Crossing from one row to another will affect the flash write timing when running from RAM.

The time it takes to program the flash memory will depend on different parameters:

- Whether the program doing the flash write is running from RAM or running from flash.
- When running from RAM we will have different timing for:
  - First write operation.
  - Repeated write operations within the same row.
  - Repeated write operation that are crossing from one row to another.

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$t_{ERASEALL}$	Erase flash memory.	1, 2			22.3	ms	1
$t_{PAGEERASEALL}$	Erase page in flash memory.	1, 2			22.3	ms	1
$t_{WRITE,FLASH}$	Program running from flash. Write one word to flash memory.	1, 3			46.3	µs	1
$t_{WRITE,RAM,1st}$	Program running from RAM. Write the first word to flash memory.	1			39.3	µs	1
$t_{WRITE,RAM,2nd}$	Program running from RAM. Repeated writes operations following the first, within the same row.	1			22.3	µs	1
$t_{WRITE,RAM,3rd}$	Program running from RAM. Repeated write operation, new word is located on a different row compare to the previous write.	1			46.3	µs	1

1. Max timing is assuming using RC16M, worst case tolerance.
2. The CPU will be halted for the duration of NVMC operations if the CPU tries to fetch data/code from the flash memory.
3. The CPU will be halted for the duration of NVMC operations.

Table 61 *NVMC specifications*

<WW>	Description
[1. .52]	Week of production

Table 78 *Week codes*

<LL>	Description
[AA. .ZZ]	Wafer production lot identifier

Table 79 *Lot codes*

<CC>	Description
R7	7″ Reel
R	13″ Reel
T	Tray

Table 80 *Container codes*

10.7 Product options

10.7.1 nRF ICs

Order code	MOQ[1]
nRF51422-QFAA-R7 nRF51422-QFAB-R7 nRF51422-QFAC-R7	1000
nRF51422-QFAA-R nRF51422-QFAB-R nRF51422-QFAC-R	3000
nRF51422-CEAA-R7 nRF51422-CDAB-R7 nRF51422-CFAC-R7	1500
nRF51422-CEAA-R nRF51422-CDAB-R nRF51422-CFAC-R	7000
nRF51422-QFAA-T nRF51422-QFAB-T nRF51422-QFAC-T	490

1. Minimum Order Quantity.

Table 81 *Order code*

10.7.2 Development tools

Order code	Description
nRF51-DK[1]	nRF51 *Bluetooth* Smart/ANT/2.4 GHz RF Development Kit
nRF51-Dongle[1]	nRF51 USB dongle for emulator, sniffer, firmware development
ANT-Dongle	ANTUSB-m Stick

1. Uses the nRF51422-QFAC version of the chip (capable of running both *Bluetooth* low energy and ANT).

Table 82 *Development tools*

11.3.1.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51422-QFAA	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 84 *QFAA QFN48 with internal LDO setup*

11.3.2 QFAA QFN48 schematic with low voltage mode setup

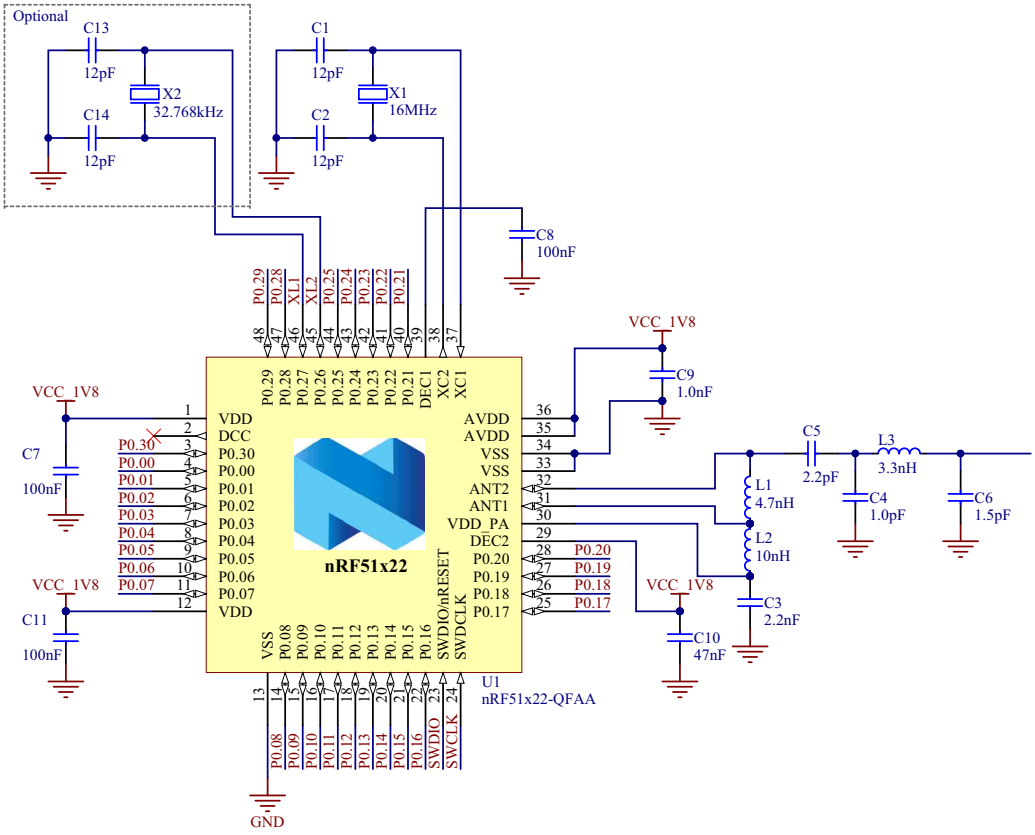

Figure 23 *QFAA QFN48 with low voltage mode setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.4.1.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51422-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 87 *QFAB QFN48 with internal LDO setup*

11.4.2.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51422-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 88 *QFAB QFN48 with low voltage mode setup*

11.6 CDAB WLCSP package

Documentation for the CDAB WLCSP package reference circuit, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from www.nordicsemi.com.

11.6.1 CDAB WLCSP schematic with internal LDO setup

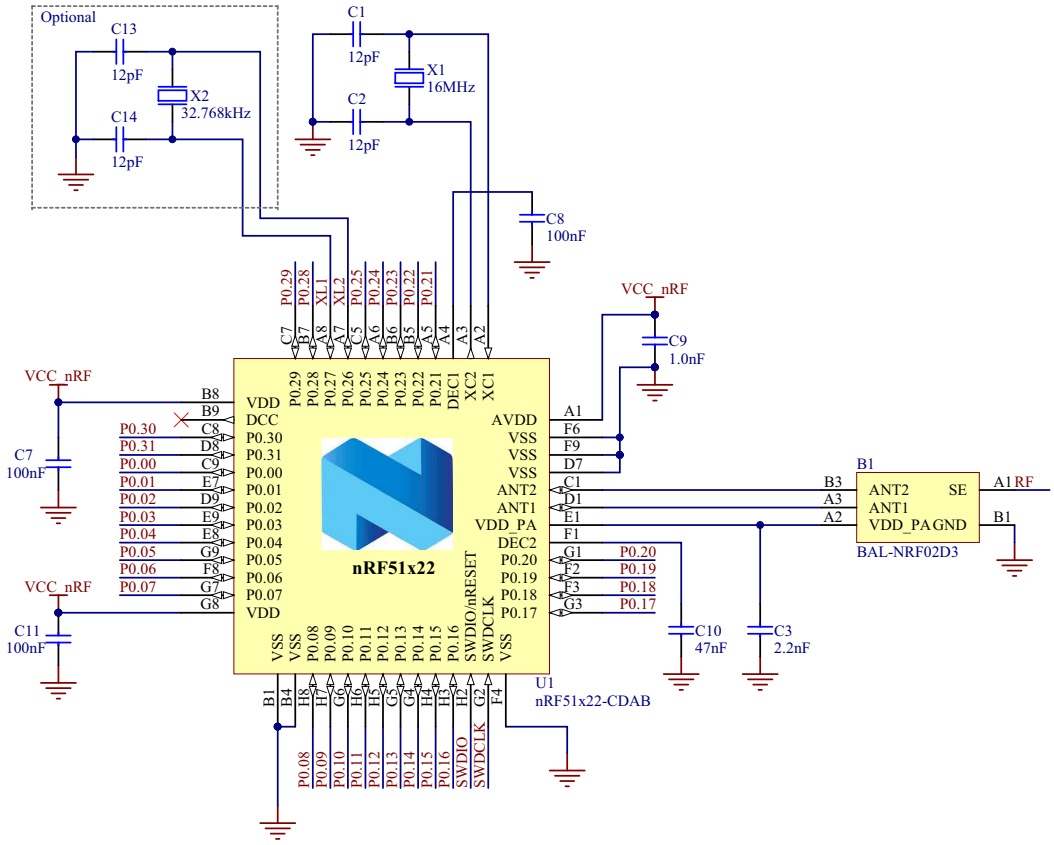

Figure 31 *CDAB WLCSP with internal LDO setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.6.2 CDAB WLCSP schematic with low voltage mode setup

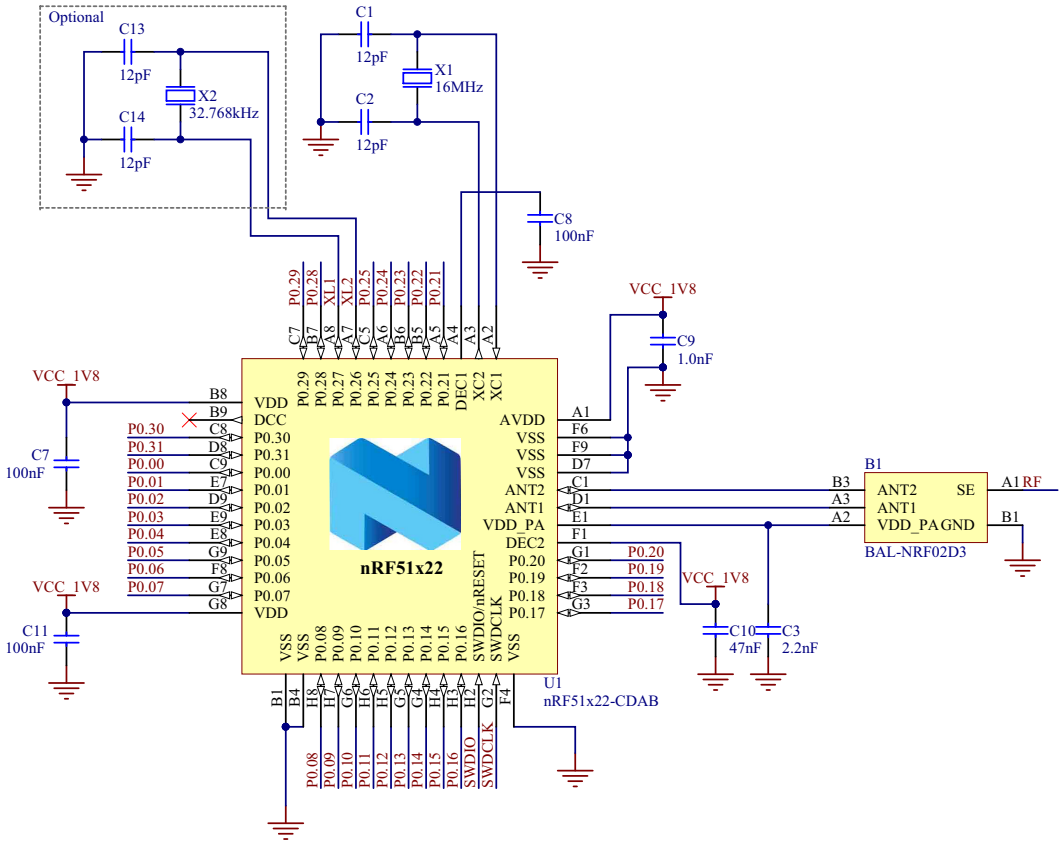

Figure 32 *CDAB WLCSP with low voltage mode setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.8.2.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
U1	nRF51422-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 100 *CFAC WLCSP with low voltage mode setup*

11.8.3 CFAC WLCSP schematic with DC/DC converter setup

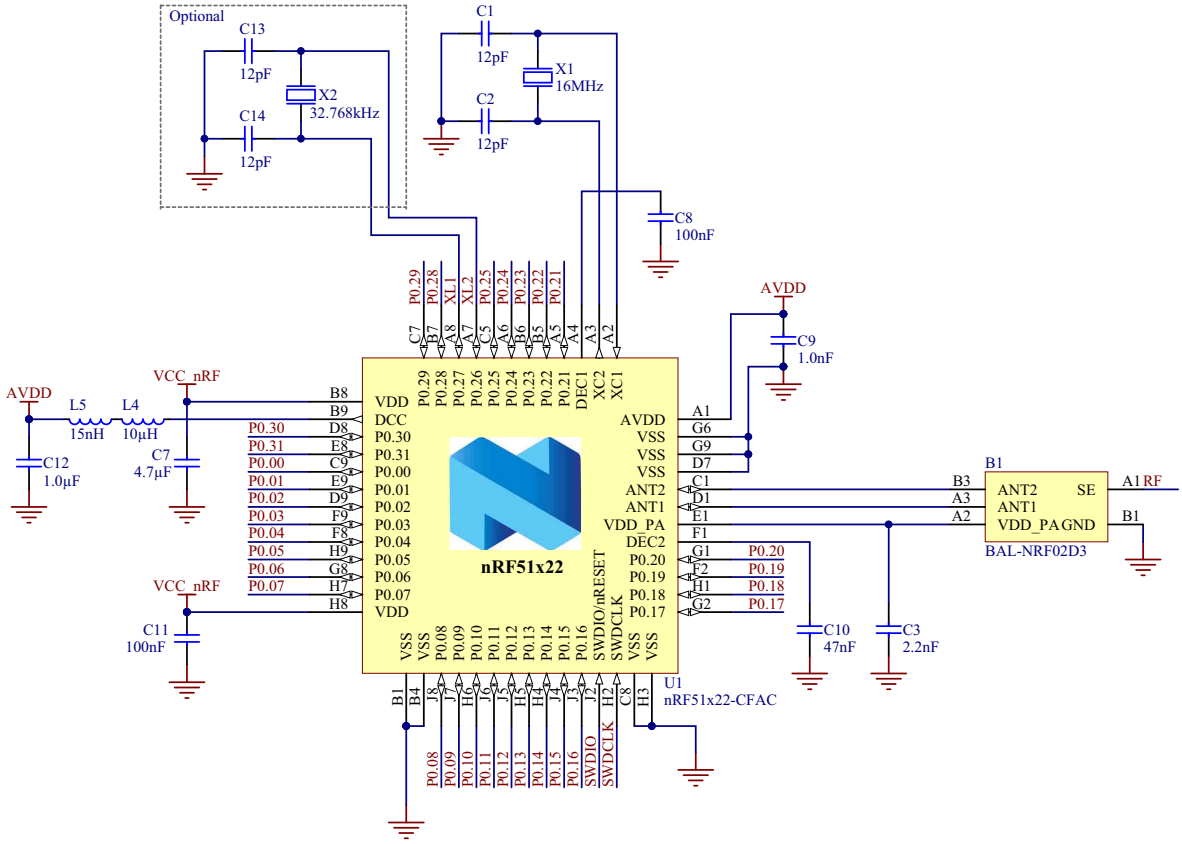

Figure 39 *CFAC WLCSP with DC/DC converter setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.