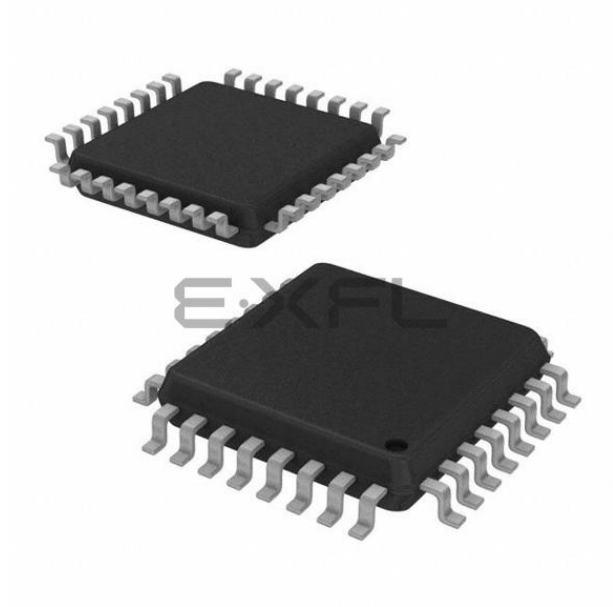

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-VQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5115-ratum

Table 4. Timers SFRs (Continued)

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
T2CON	C8h	Timer/Counter 2 control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
T2MOD	C9h	Timer/Counter 2 Mode							T2OE	DCEN
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High byte								
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program						S2	S1	S0

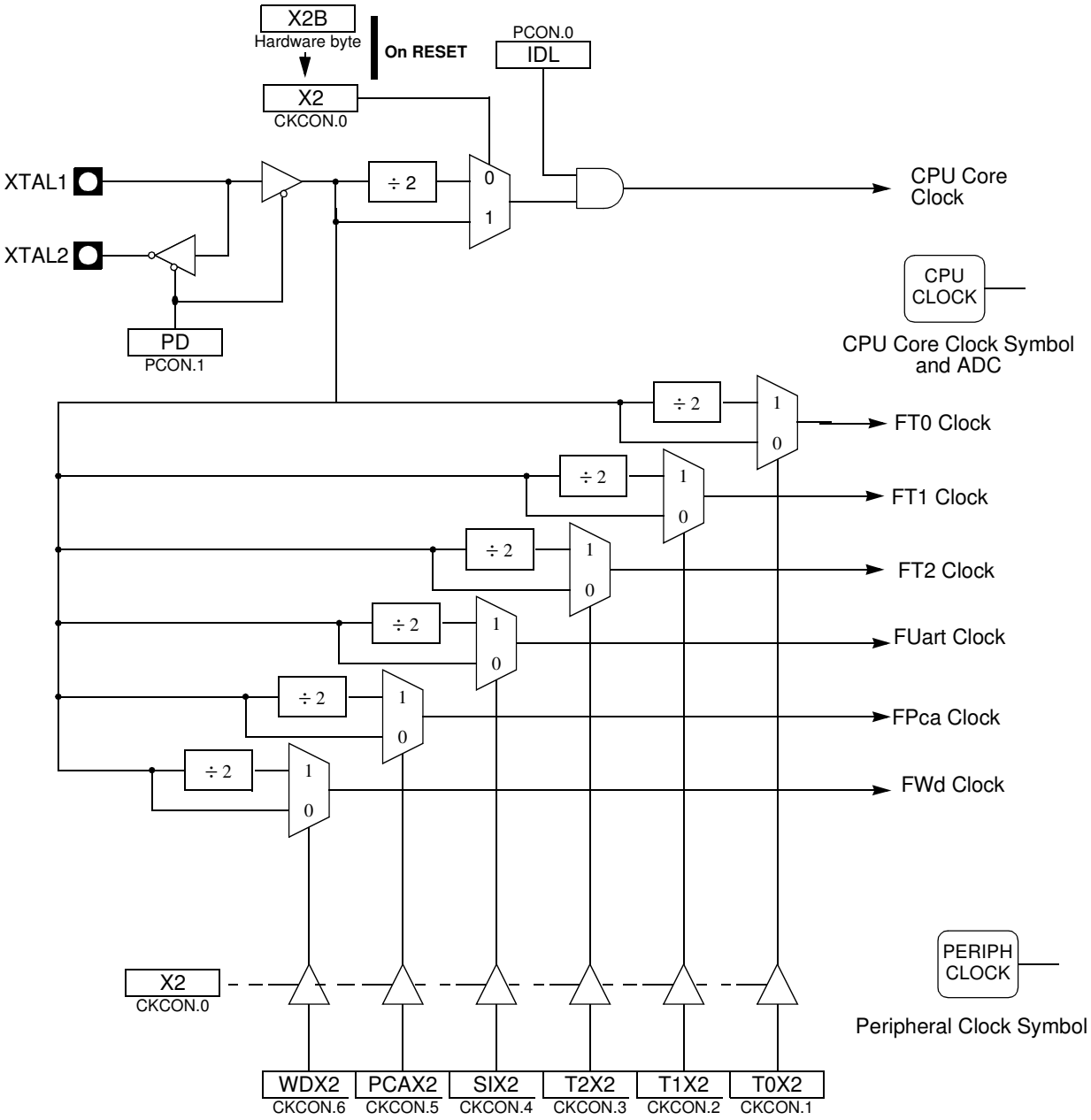
Table 5. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								

Table 6. PCA SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL					CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low byte								
CH	F9h	PCA Timer/Counter High byte								
CCAPM0 CCAPM1	DAh DBh	PCA Timer/Counter Mode 0 PCA Timer/Counter Mode 1		ECOM0 ECOM1	CAPP0 CAPP1	CAPN0 CAPN1	MAT0 MAT1	TOG0 TOG1	PWM0 PWM1	ECCF0 ECCF1
CCAP0H CCAP1H	FAh FBh	PCA Compare Capture Module 0 H PCA Compare Capture Module 1 H	CCAP0H7 CCAP1H7	CCAP0H6 CCAP1H6	CCAP0H5 CCAP1H5	CCAP0H4 CCAP1H4	CCAP0H3 CCAP1H3	CCAP0H2 CCAP1H2	CCAP0H1 CCAP1H1	CCAP0H0 CCAP1H0

Figure 3. Clock CPU Generation Diagram



Reset Recommendation to Prevent Flash Corruption

When a Flash program memory is embedded on-chip, it is strongly recommended to use an external reset chip (brown out device) to apply a reset (Figure 7). It prevents system malfunction during periods of insufficient power-supply voltage (power-supply failure, power supply switched off, etc.).

Idle Mode

Idle mode is a power reduction mode that reduces the power consumption. In this mode, program execution halts. Idle mode freezes the clock to the CPU at known states while the peripherals continue to be clocked. The CPU status before entering Idle mode is preserved, i.e., the program counter and program status word register retain their data for the duration of Idle mode. The contents of the SFRs and RAM are also retained. The status of the Port pins during Idle mode is detailed in Table 12.

Entering Idle Mode

To enter Idle mode, set the IDL bit in PCON register (See Table 15). The T89C5115 enters Idle mode upon execution of the instruction that sets IDL bit. The instruction that sets IDL bit is the last instruction executed.

Note: If IDL bit and PD bit are set simultaneously, the T89C5115 enters Power-down mode. Then it does not go in Idle mode when exiting Power-down mode.

Exiting Idle Mode

There are two ways to exit Idle mode:

1. Generate an enabled interrupt.

   Hardware clears IDL bit in PCON register which restores the clock to the CPU. Execution resumes with the interrupt service routine. Upon completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Idle mode. The general purpose flags (GF1 and GF0 in PCON register) may be used to indicate whether an interrupt occurred during normal operation or during Idle mode. When Idle mode is exited by an interrupt, the interrupt service routine may examine GF1 and GF0.

2. Generate a reset.

   A logic high on the RST pin clears IDL bit in PCON register directly and asynchronously. This restores the clock to the CPU. Program execution momentarily resumes with the instruction immediately following the instruction that activated the Idle mode and may continue for a number of clock cycles before the internal reset algorithm takes control. Reset initializes the T89C5115 and vectors the CPU to address C:0000h.

Notes: 1. During the time that execution resumes, the internal RAM cannot be accessed; however, it is possible for the Port pins to be accessed. To avoid unexpected outputs at the Port pins, the instruction immediately following the instruction that activated Idle mode should not write to a Port pin or to the external RAM.
2. If Idle mode is invoked by ADC Idle, the ADC conversion completion will exit Idle.

Power-down Mode

The Power-down mode places the T89C5115 in a very low power state. Power-down mode stops the oscillator, freezes all clock at known states. The CPU status prior to entering Power-down mode is preserved, i.e., the program counter, program status word register retain their data for the duration of Power-down mode. In addition, the SFRs and RAM contents are preserved. The status of the Port pins during Power-down mode is detailed in Table 14.

Entering Power-down Mode

To enter Power-down mode, set PD bit in PCON register. The T89C5115 enters the Power-down mode upon execution of the instruction that sets PD bit. The instruction that sets PD bit is the last instruction executed.

Registers

Table 15. PCON Register
PCON (S:87h)
Power Control Register

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-off Flag** Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-down Mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle Mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

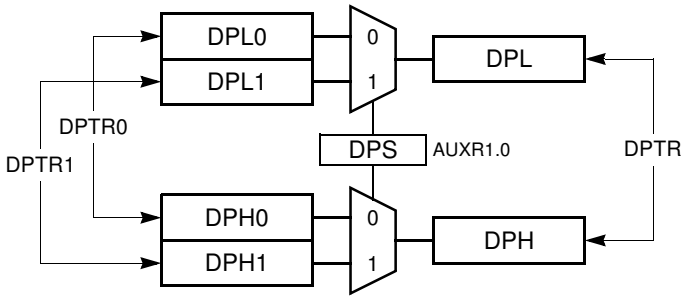
Reset Value = 00X1 0000b
Not bit addressable

Dual Data Pointer

Description

The T89C5115 implements a second data pointer for speeding up code execution and reducing code size in case of intensive usage of external memory accesses.
DPTR0 and DPTR1 are Seen by the CPU as DPTR and are accessed using the SFR addresses 83h and 84h that are the DPH and DPL addresses. The DPS bit in AUXR1 register (See Figure 18) is used to select whether DPTR is the data pointer 0 or the data pointer 1 (See Figure 11).

Figure 11. Dual Data Pointer Implementation



Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare…) are well served by using one data pointer as a “source” pointer and the other one as a “destination” pointer. Hereafter is an example of block move implementation using the two pointers and coded in assembler. The latest C compiler takes also advantage of this feature by providing enhanced algorithm libraries.
The INC instruction is a short (2 Bytes) and fast (6 machine cycle) way to manipulate the DPS bit in the AUXR1 register. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is 0 or 1 on entry.

```
; ASCII block move using dual data pointers
; Modifies DPTR0, DPTR1, A and PSW
; Ends when encountering NULL character
; Note: DPS exits opposite to the entry state unless an extra INC AUXR1 is
added

AUXR1EQU0A2h

move:movDPTR,#SOURCE ; address of SOURCE
  incAUXR1 ; switch data pointers
  movDPTR,#DEST ; address of DEST
mv_loop:incAUXR1; switch data pointers
  movxA,@DPTR; get a byte from SOURCE
  incDPTR; increment SOURCE address
  incAUXR1; switch data pointers
  movx@DPTR,A; write the byte to DEST
  incDPTR; increment DEST address
  jnzmv_loop; check for NULL terminator
end_move:
```

EEPROM Data Memory

The 2K bytes on-chip EEPROM memory block is located at addresses 0000h to 07FFh of the XRAM/XRAM memory space and is selected by setting control bits in the EECON register. A read in the EEPROM memory is done with a MOVX instruction.

A physical write in the EEPROM memory is done in two steps: write data in the column latches and transfer of all data latches into an EEPROM memory row (programming).

The number of data written on the page may vary from 1 up to 128 Bytes (the page size). When programming, only the data written in the column latch is programmed and a ninth bit is used to obtain this feature. This provides the capability to program the whole memory by Bytes, by page or by a number of Bytes in a page. Indeed, each ninth bit is set when the writing the corresponding byte in a row and all these ninth bits are reset after the writing of the complete EEPROM row.

Write Data in the Column Latches

Data is written by byte to the column latches as for an external RAM memory. Out of the 11 address bits of the data pointer, the 4 MSBs are used for page selection (row) and 7 are used for byte selection. Between two EEPROM programming sessions, all the addresses in the column latches must stay on the same page, meaning that the 4 MSB must no be changed.

The following procedure is used to write to the column latches:

- Save and disable interrupt
- Set bit EEE of EECON register
- Load DPTR with the address to write
- Store A register with the data to be written
- Execute a MOVX @DPTR, A
- If needed loop the three last instructions until the end of a 128 Bytes page
- Restore interrupt

Note: The last page address used when loading the column latch is the one used to select the page programming address.

Programming

The EEPROM programming consists of the following actions:

- Write one or more Bytes of one page in the column latches. Normally, all Bytes must belong to the same page; if not, the last page address will be latched and the others discarded.
- Launch programming by writing the control sequence (50h followed by A0h) to the EECON register.
- EEBUSY flag in EECON is then set by hardware to indicate that programming is in progress and that the EEPROM segment is not available for reading.
- The end of programming is indicated by a hardware clear of the EEBUSY flag.

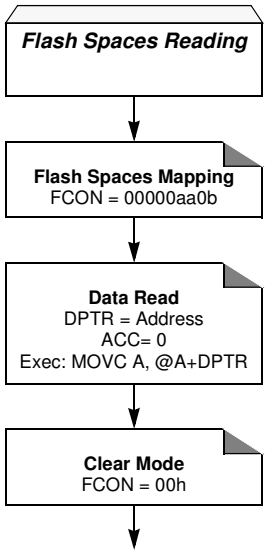
Note: The sequence 5xh and Axh must be executed without instructions between then otherwise the programming is aborted.

Read Data

The following procedure is used to read the data stored in the EEPROM memory:

- Save and disable interrupt
- Set bit EEE of EECON register
- Load DPTR with the address to read
- Execute a MOVX A, @DPTR
- Restore interrupt

Figure 17. Reading Procedure



Note: aa = 10 for the Hardware Security Byte.

Flash Protection from Parallel Programming

The three lock bits in Hardware Security Byte (See 'In-System Programming' section) are programmed according to Table 23 provide different level of protection for the on-chip code and data located in FM0 and FM1.

The only way to write this bits are the parallel mode. They are set by default to level 3.

Table 23. Program Lock bit

Program Lock bits				
Security Level	LB0	LB1	LB2	**Protection Description**
1	U	U	U	No program lock features enabled.
2	P	U	U	Parallel programming of the Flash is disabled.
3	U	P	U	Same as 2, also verify through parallel programming interface is disabled. This is the factory defaul programming.
4	U	U	P	Same as 3

Note: 1. Program Lock bits
U: unprogrammed
P: programmed

WARNING: Security level 2, 3 and 4 should only be programmed after Flash and Core verification.

Preventing Flash Corruption

See Section "Power Management".

Registers

Table 24. FCON Register
FCON Register FCON (S:D1h)
Flash Control Register

7	6	5	4	3	2	1	0
FPL3	**FPL2**	**FPL1**	**FPL0**	**FPS**	**FMOD1**	**FMOD0**	**FBUSY**

Bit Number	Bit Mnemonic	Description
7 - 4	FPL3:0	**Programming Launch Command bits** Write 5Xh followed by AXh to launch the programming according to FMOD1:0. (See Table 22.)
3	FPS	**Flash Map Program Space** Set to map the column latch space in the data memory space. Clear to re-map the data memory space.
2 - 1	FMOD1:0	**Flash Mode** See Table 21 or Table 22.
0	FBUSY	**Flash Busy** Set by hardware when programming is in progress. Clear by hardware when programming is done. Can not be changed by software.

Reset Value = 0000 0000b

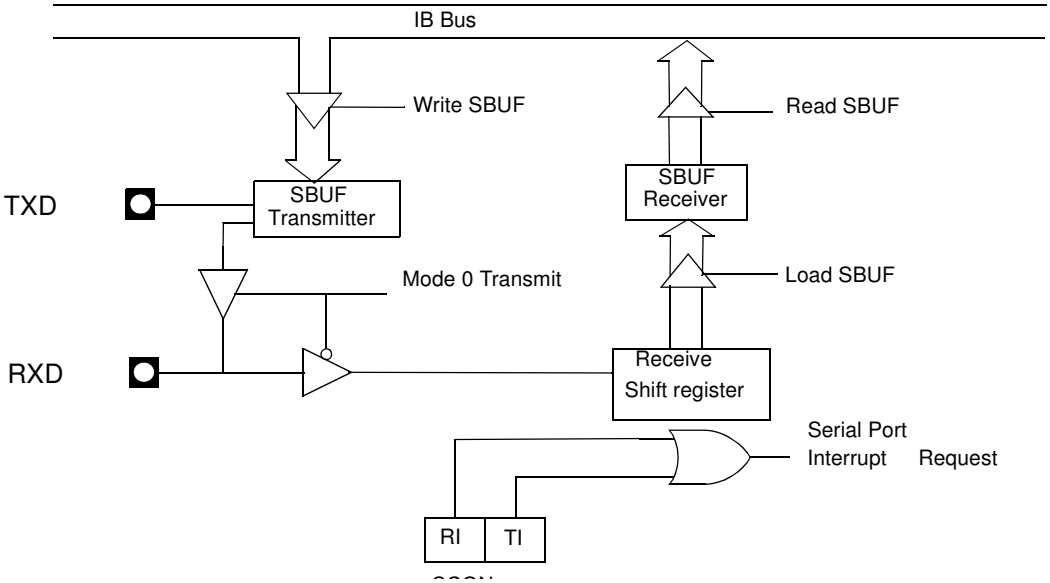
Serial I/O Port

The T89C5115 I/O serial port is compatible with the I/O serial port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as a Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

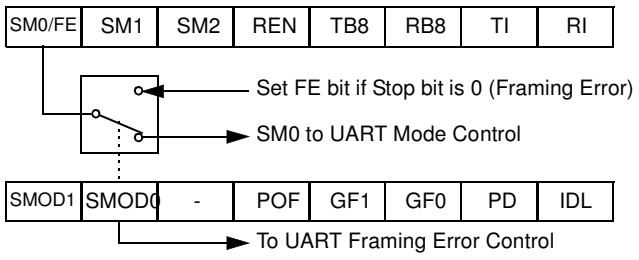
Figure 20. Serial I/O Port Block Diagram



Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register.

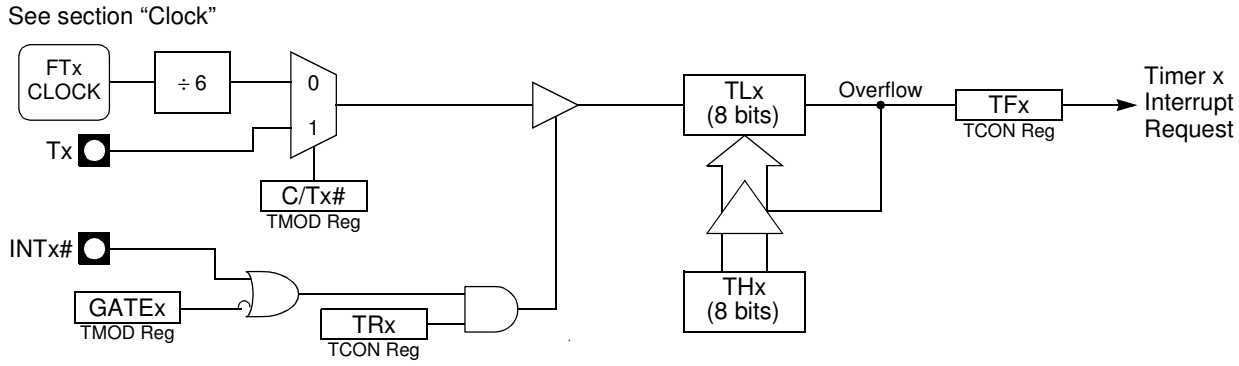
Figure 21. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register bit is set.

The software may examine the FE bit after each reception to check for data errors. Once set, only software or a reset clears the FE bit. Subsequently received frames with valid stop bits cannot clear the FE bit. When the FE feature is enabled, RI rises on the stop bit instead of the last data bit (See Figure 22 and Figure 23).

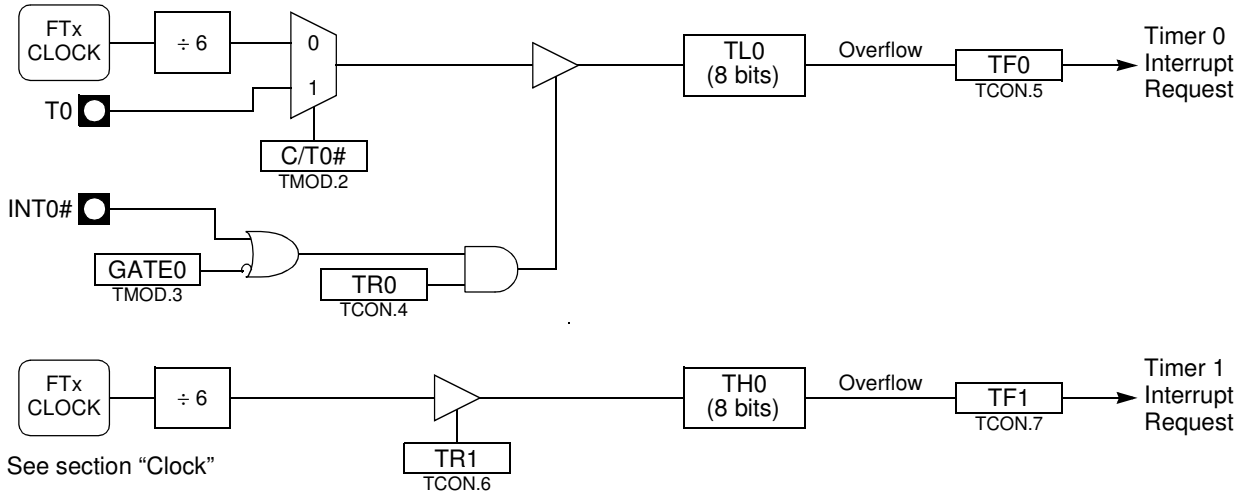
Figure 26. Timer/Counter x (x= 0 or 1) in Mode 2



Mode 3 (Two 8-bit Timers)

Mode 3 configures Timer 0 such that registers TL0 and TH0 operate as separate 8-bit Timers (See Figure 27). This mode is provided for applications requiring an additional 8-bit Timer or Counter. TL0 uses the Timer 0 control bits C/T0# and GATE0 in TMOD register, and TR0 and TF0 in TCON register in the normal manner. TH0 is locked into a Timer function (counting F_{PER} /6) and takes over use of the Timer 1 interrupt (TF1) and run control (TR1) bits. Thus, operation of Timer 1 is restricted when Timer 0 is in mode 3.

Figure 27. Timer/Counter 0 in Mode 3: Two 8-bit Counters



Timer 1

Timer 1 is identical to Timer 0 excepted for Mode 3 which is a hold-count mode. Following comments help to understand the differences:

- Timer 1 functions as either a Timer or event Counter in three modes of operation. Figure 24 to Figure 26 show the logical configuration for modes 0, 1, and 2. Timer 1’s mode 3 is a hold-count mode.
- Timer 1 is controlled by the four high-order bits of TMOD register (See Figure 38) and bits 2, 3, 6 and 7 of TCON register (See Figure 37). TMOD register selects the method of Timer gating (GATE1), Timer or Counter operation (C/T1#) and mode of operation (M11 and M01). TCON register provides Timer 1 control functions: overflow flag (TF1), run control bit (TR1), interrupt flag (IE1) and interrupt type control bit (IT1).
- Timer 1 can serve as the Baud Rate Generator for the Serial Port. Mode 2 is best suited for this purpose.

Watchdog Timer

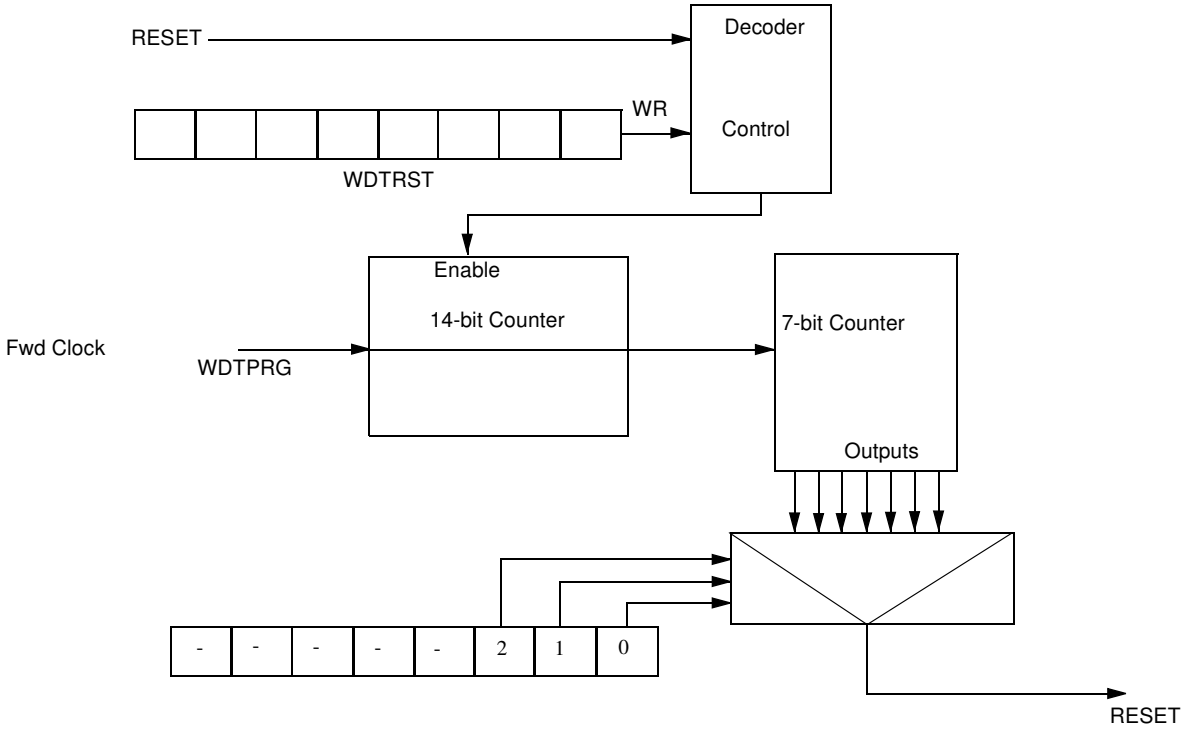
T89C5115 contains a powerful programmable hardware Watchdog Timer (WDT) that automatically resets the chip if it software fails to reset the WDT before the selected time interval has elapsed. It permits large Timeout ranging from 16ms to 2s @f_{OSC} = 12 MHz in X1 mode.

This WDT consists of a 14-bit counter plus a 7-bit programmable counter, a Watchdog Timer reset register (WDTRST) and a Watchdog Timer programming (WDTPRG) register. When exiting reset, the WDT is -by default- disable.

To enable the WDT, the user has to write the sequence 1EH and E1H into WDTRST register with no instruction between the two writes. When the Watchdog Timer is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 96xT_{OSC}, where T_{OSC}=1/f_{OSC}. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset

Note: When the watchdog is enable it is impossible to change its period.

Figure 31. Watchdog Timer



16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

Figure 35. PCA 16-bit Software Timer and High Speed Output Mode

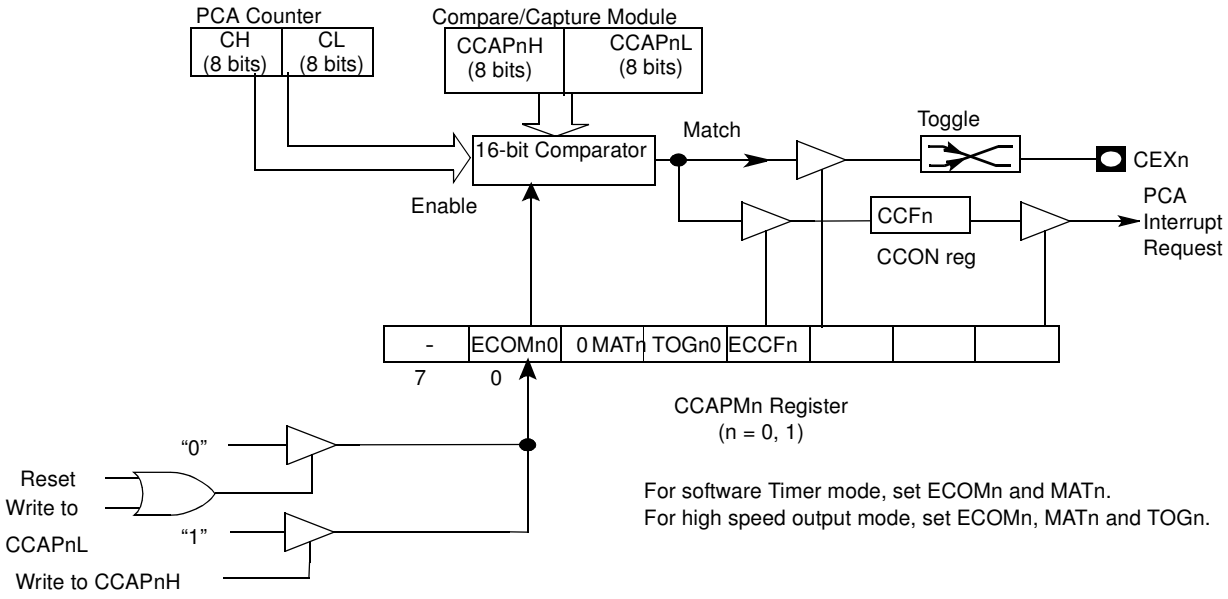


Table 54. CCON Register

CCON (S:D8h)
PCA Counter Control Register

7	6	5	4	3	2	1	0
CF	**CR**	**-**	**-**	**-**	**-**	**CCF1**	**CCF0**

Bit Number	Bit Mnemonic	Description
7	CF	**PCA Timer/Counter Overflow flag** Set by hardware when the PCA Timer/Counter rolls over. This generates a PCA interrupt request if the ECF bit in CMOD register is set. Must be cleared by software.
6	CR	**PCA Timer/Counter Run Control bit** Clear to turn the PCA Timer/Counter off. Set to turn the PCA Timer/Counter on.
5-2	-	**Reserved** The value read from these bist are indeterminate. Do not set these bits.
1	CCF1	**PCA Module 1 Compare/Capture Flag** Set by hardware when a match or capture occurs. This generates a PCA interrupt request if the ECCF 1 bit in CCAPM 1 register is set. Must be cleared by software.
0	CCF0	**PCA Module 0 Compare/Capture Flag** Set by hardware when a match or capture occurs. This generates a PCA interrupt request if the ECCF 0 bit in CCAPM 0 register is set. Must be cleared by software.

Reset Value = 00xx xx00b

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register. This register also contains a global disable bit which must be cleared to disable all the interrupts at the same time.

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority registers. The Table below shows the bit values and priority levels associated with each combination.

Table 66. Priority Level bit Values

IPH.x	IPL.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of the higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence, See Table 67.

Table 67. Interrupt Priority Within Level

Interrupt Name	Interrupt Address Vector	Priority Number
External interrupt (INT0)	0003h	1
Timer0 (TF0)	000Bh	2
External interrupt (INT1)	0013h	3
Timer 1 (TF1)	001Bh	4
PCA (CF or CCFn)	0033h	5
UART (RI or TI)	0023h	6
Timer 2 (TF2)	002Bh	7
ADC (ADCI)	0043h	9

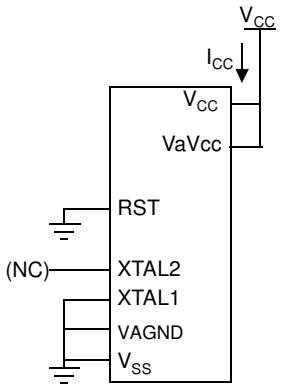
Table 70. IPH0 Register
IPH0 (B7h)
Interrupt High Priority Register

7	6	5	4	3	2	1	0
-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCH	**PCA Interrupt Priority Level Most Significant bit** **PPCH PPC Priority level** 0 0 Lowest 0 1 1 0 1 1 Highest priority
5	PT2H	**Timer 2 Overflow Interrupt High Priority bit** **PT2H PT2 Priority Level** 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	**Serial Port High Priority bit** **PSH PS Priority Level** 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 Overflow Interrupt High Priority bit** **PT1H PT1 Priority Level** 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External Interrupt 1 High Priority bit** **PX1H PX1 Priority Level** 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 Overflow Interrupt High Priority bit** **PT0H PT0 Priority Level** 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External Interrupt 0 High Priority bit** **PX0H PX0 Priority Level** 0 0 Lowest 0 1 1 0 1 1 Highest

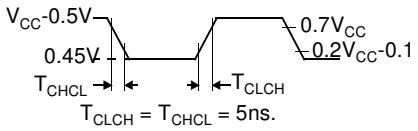
Reset Value = X000 0000b

Figure 47. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 48. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



DC Parameters for A/D Converter

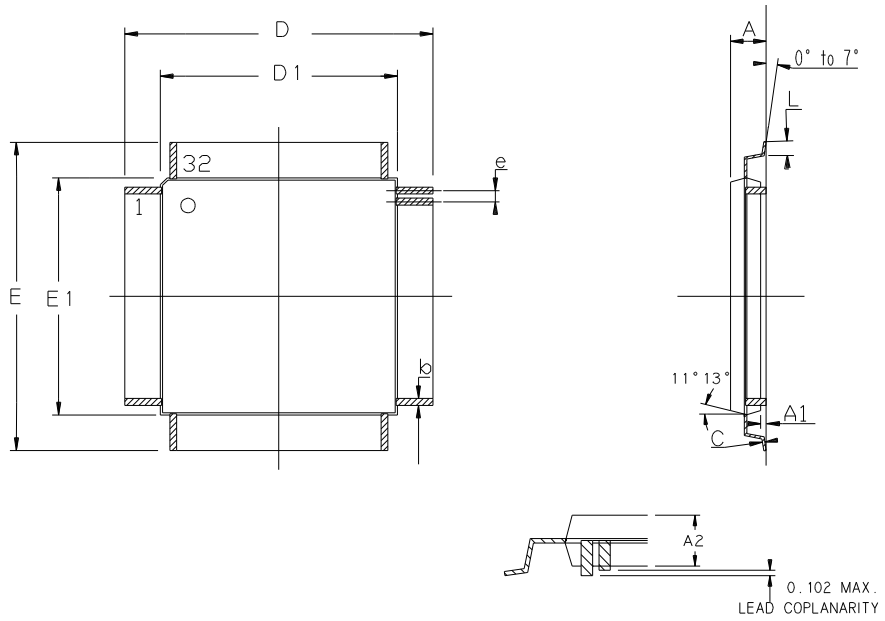
Table 73. DC Parameters for AD Converter in Precision Conversion

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
AVin	Analog input voltage	Vss- 0.2		Max Vref + 0.6	V	
VaVcc	Analog supply voltage	Vref	Vcc	Vcc + 10%	V	
Rref(2)	Resistance between Vref and Vss	12	16	24	KΩ	
Vref	Reference voltage	2.40		3.00	V	
Rai	Analog input Resistor			400	Ω	During sampling
Cai	Analog input Capacitance		60		pF	During sampling
INL	Integral non linearity		1	2	lsb	
DNL	Differential non linearity		0.5	1	lsb	
OE	Offset error	-2		2	lsb	

Notes: 1. Typicals are based on a limited number of samples and are not guaranteed.
2. With ADC enabled.

Package Drawings

VQFP32



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.05	0.15	.002	.006
A2	1.35	1.45	.053	.057
C	0.09	0.20	.004	.008
D	9.00 BSC		.354 BSC	
D1	7.00 BSC		.276 BSC	
E	9.00 BSC		.354 BSC	
E1	7.00 BSC		.276 BSC	
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
b	0.30	0.45	.012	.018