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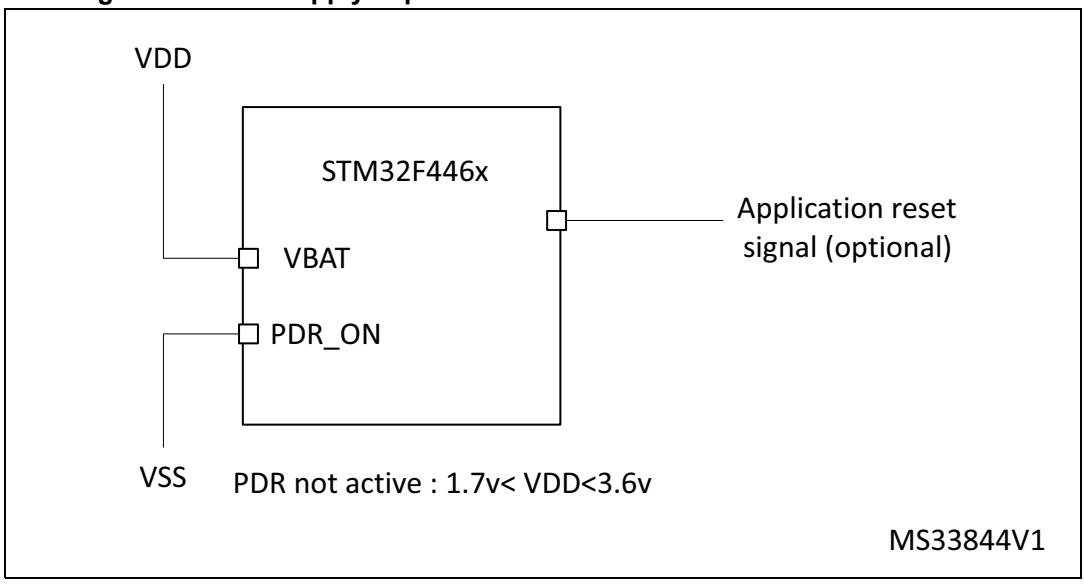
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446rct6

Figure 6. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All packages, except for the LQFP100/LQFP64, allow to disable the internal reset through the PDR_ON signal.

3.17 Voltage regulator

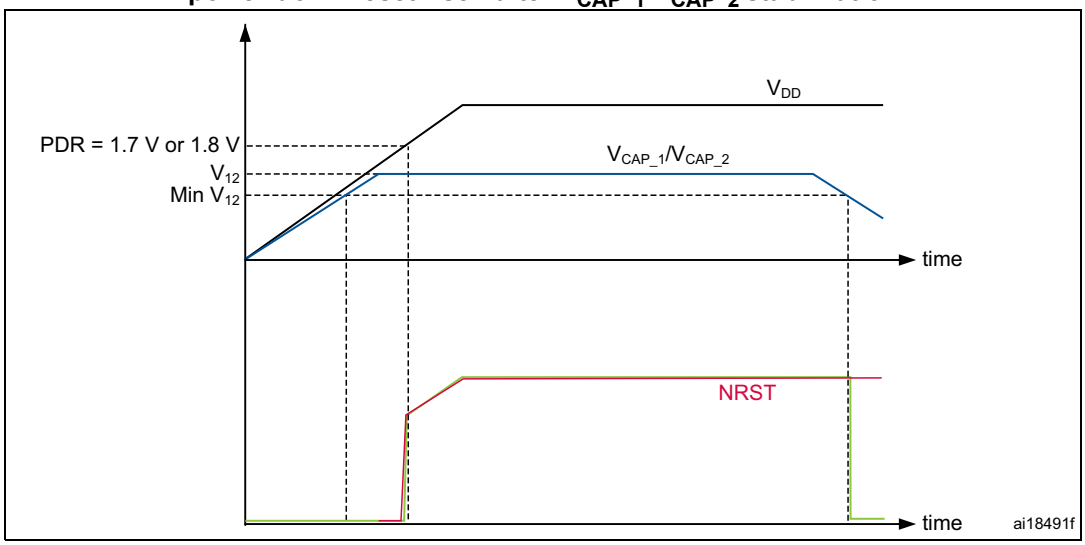
The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

3.17.1 Regulator ON

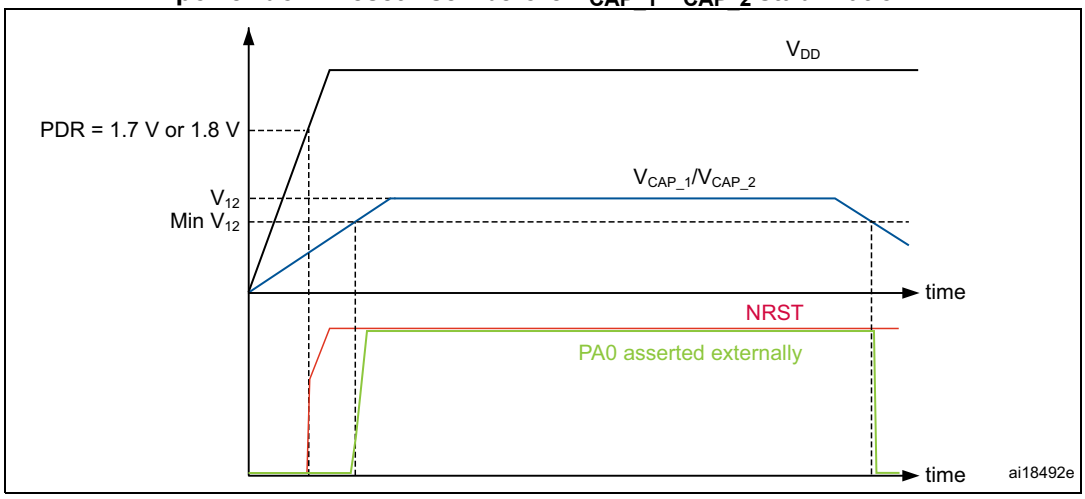
On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

Figure 8. Startup in regulator OFF: slow V_{DD} slope power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 9. Startup in regulator OFF mode: fast V_{DD} slope power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

3.17.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP64 LQFP100	Yes	No	Yes	No

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

3.38 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT}, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.39 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 10-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.40 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5V tolerant IO, I2C FM+ option
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F446xx pin and ball descriptions

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	1	D7	A3	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, FMC_A23, EVENTOUT	-
-	2	D6	A2	2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
-	3	A9	B2	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, EVENTOUT	-
-	4	-	B3	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, EVENTOUT	-

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	61	-	K11	85	PD14	I/O	FTf	-	TIM4_CH3, FMPI2C1_SCL, SAI2_SCK_A, FMC_D0, EVENTOUT	-
-	62	-	K12	86	PD15	I/O	FTf	-	TIM4_CH4, FMPI2C1_SDA, FMC_D1, EVENTOUT	-
-	-	-	J12	87	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	-	-	J11	88	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	-	-	J10	89	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	-	-	H12	90	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, DCMI_D12, EVENTOUT	-
-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, FMC_INT, DCMI_D13, EVENTOUT	-
-	-	-	G11	93	PG8	I/O	FT	-	SPDIFRX_IN2, USART6_RTS, FMC_SDCLK, EVENTOUT	-
-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	F10	-	VDD	S	-	-	-	-
-	-	E1	C11	95	VDDUSB	S	-	-	-	-
37	63	F1	G12	96	PC6	I/O	FTf	-	TIM3_CH1, TIM8_CH1, FMPI2C1_SCL, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, EVENTOUT	-
38	64	F2	F12	97	PC7	I/O	FTf	-	TIM3_CH2, TIM8_CH2, FMPI2C1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, SPDIFRX_IN1, USART6_RX, SDIO_D7, DCMI_D1, EVENTOUT	-
39	65	F3	F11	98	PC8	I/O	FT	-	TRACED0, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
63	99	B7	E6	-	VSS	S	-	-	-	-
-	-	B8	E5	143	PDR_ON	S	-	-	-	-
64	100	A8	F5	144	VDD	S	-	-	-	-

1. PA11, PA12, PB14 and PB15 I/Os are supplied by VDDUSB

Table 23. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(2)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	External clock, PLL ON, all peripherals enabled(3)(4)	180	72	83.0(5)	100.0	110.0(5)	mA
			168	65	71.0	95.3	101.0	
			150	59	63.6	85.4	100.8	
			144(6)	54	58.4	78.8	91.2	
			120	40	44.9	62.1	73.2	
			90	30	35.3	50.7	60.0	
			60	21	25.5	39.2	46.8	
			30	12	16.2	28.1	36.0	
			25	10	14.41	26.17	32.4	
		HSI, PLL OFF, all peripherals enabled	16	6	11.4	23.1	25.2	
			8	3	9.5	20.3	22.5	
			4	2.3	8.3	18.9	21.1	
			2	1.8	7.7	18.1	20.5	
		External clock, PLL ON, all Peripherals disabled(3)	180	32	42.0(5)	59.0	75.0(5)	
			168	29	35.5	51.4	55.7	
			150	26	31.5	47.8	51.9	
			144(6)	24	29.2	44.7	48.6	
			120	18	23.3	36.8	40.4	
			90	14	19.0	31.8	35.1	
			60	10	14.7	26.9	29.9	
			30	6	10.7	22.1	24.9	
			25	5	9.96	21.24	24.02	
		HSI, PLL OFF, all peripherals disabled(3)	16	3	8.7	18.9	21.9	
			8	2	8.1	17.8	20.9	
			4	1.7	7.64	17.23	20.32	
			2	1.4	7.4	16.94	20.03	

1. Code and data processing running from SRAM1 using boot pins.
2. Guaranteed based on test during characterization.
3. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
4. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
5. Tested in production.
6. Overdrive OFF

Table 26. Typical and maximum current consumption in Sleep mode(1)

Symbol	Parameter	Conditions		fHCLK (MHz)	Typ	Max			Unit
						T_A = 25 °C	T_A = 25 °C	T_A = 25 °C	
IDD	Supply current in Sleep mode	all peripherals enabled	External clock, PLL ON, Flash on	180	51.2	59.00	77.25	102.00	mA
				168(2)	46.8	53.94	66.48	79.40	
				150	42.2	49.26	60.84	73.41	
				144(2)	38.6	45.37	55.47	66.96	
				120	29.3	35.70	42.49	51.46	
				90	22.8	29.17	34.78	43.12	
				60	16.3	22.41	27.12	34.83	
				30	10.1	16.03	19.72	26.86	
				25	9.0	14.92	18.41	25.38	
			HSI, PLL off, Flash on	16	6.5	13.10	15.1	22.3	
				8	5.2	12.31	13.5	20.4	
				4	4.5	11.63	12.5	19.3	
				2	4.1	11.23	12.0	18.8	

Table 26. Typical and maximum current consumption in Sleep mode(1) (continued)

Symbol	Parameter	Conditions		fHCLK (MHz)	Typ	Max			Unit
						T_A = 25 °C	T_A = 25 °C	T_A = 25 °C	
IDD	Supply current in Sleep mode	HSI, PLL off, all peripherals disabled	Flash on	16	3.89	4.93	11.72	18.54	mA
				8	2.45	3.29	11.66	18.46	
				4	1.69	2.56	11.60	18.40	
				2	1.28	2.22	11.57	18.37	
			Flash in Deep Power Down mode	16	1.0	6.65	16.54	19.50	
				8	0.9	6.93	16.48	19.45	
				4	0.9	6.90	16.43	19.39	
				2	0.9	6.88	16.41	19.37	
			Flash in STOP mode	16	1.0	6.7	16.5	19.5	
				8	0.9	6.9	16.5	19.5	
				4	0.9	6.9	16.4	19.4	
				2	0.9	6.9	16.4	19.4	

1. Guaranteed based on test during characterization unless otherwise specified.
2. Overdrive OFF

Table 30. Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), VDD=1.7 V(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode from V_{DD} supply	All Peripherals enabled	168	65.11	70.0	79.7	90.0	mA
			150	58.31	62.8	73.4	79.9	
			144	53.14	57.1	69.9	75.3	
			120	39.58	47.2	60.7	71.4	
			90	29.99	34.70	45.23	49.34	
			60	20.37	25.2	35.2	38.2	
			30	11.37	12.9	28.4	33.2	
			25	9.65	10.9	17.8	24.3	
		All Peripherals disabled	168	29.74	32.43	42.4	48.5	
			150	25.81	29.12	39.4	43.8	
			144	24.57	26.61	36.0	41.9	
			120	17.69	22.09	32.9	40.8	
			90	13.58	15.92	30.0	36.5	
			60	9.41	11.05	24.4	30.2	
			30	5.44	6.64	15.0	22.0	
			25	4.73	5.72	12.57	19.06	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

6.3.17 I/O port characteristics

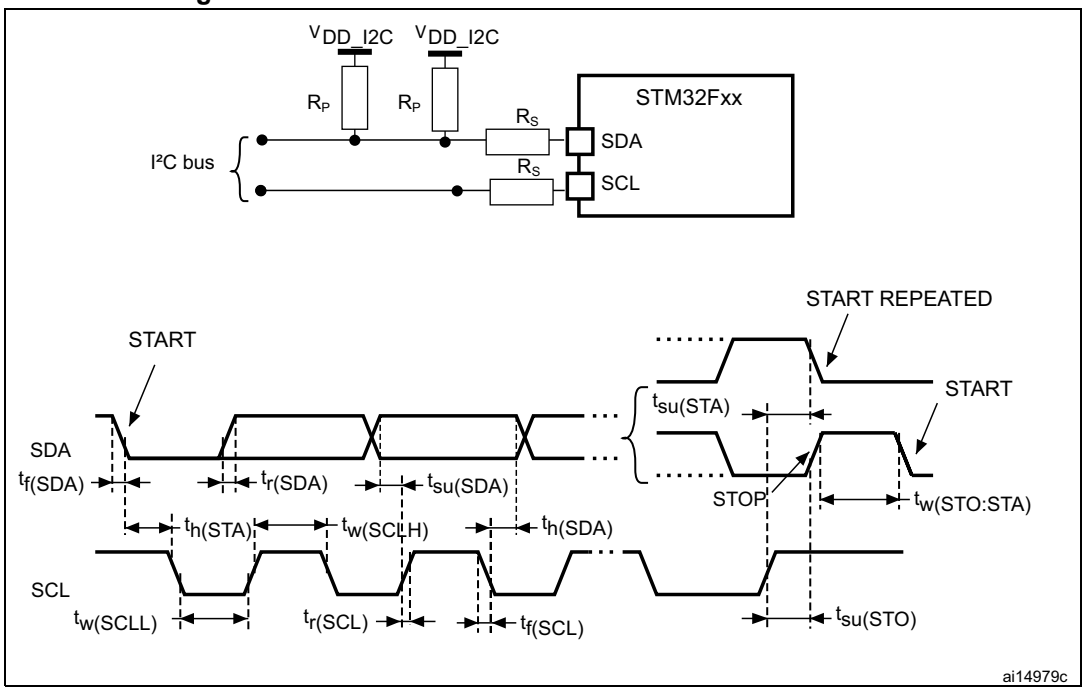
General input/output characteristics

Unless otherwise specified, the parameters given in *Table 56: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 16*. All I/Os are CMOS and TTL compliant.

Table 56. I/O static characteristics

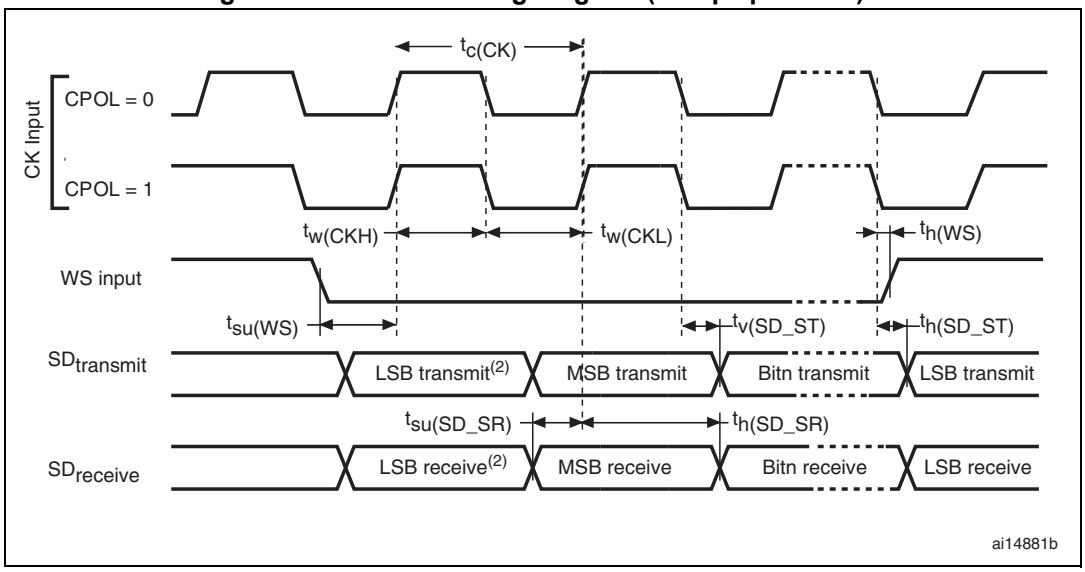
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, FTf, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}-0.04$(1) $0.3V_{DD}$(2)	V
	BOOT0 I/O input low level voltage	1.75 V ≤ V_{DD} ≤ 3.6 V, – 40 °C≤ T_A ≤ 105 °C	-	-	$0.1V_{DD}+0.1$(1)	
		1.7 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤105 °C	-	-		
V_{IH}	FT, FTf, TTa and NRST I/O input high level voltage(4)	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3$(1) $0.7V_{DD}$(2)	-	-	V
	BOOT0 I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, – 40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7$(1)	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
V_{HYS}	FT, FTf, TTa and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	-	$10\%V_{DD}$	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	-	100m	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	-		-	
I_{lkg}	I/O input leakage current (3)	V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (4)	V_{IN} = 5 V	-	-	3	

Figure 34. I²C bus AC waveforms and measurement circuit



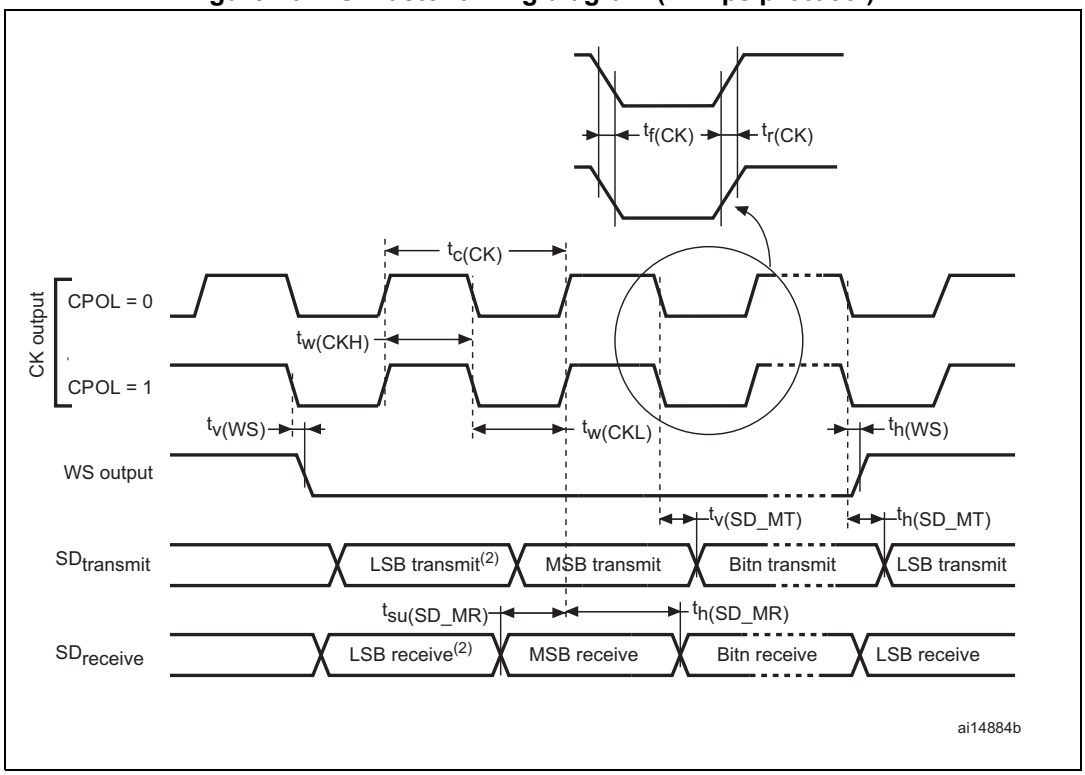
1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.

Figure 39. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 40. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 74. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.16.2: Internal reset OFF*).
2. Guaranteed based on test during characterization.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 74*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 75. ADC static accuracy at f_{ADC} = 18 MHz(1)

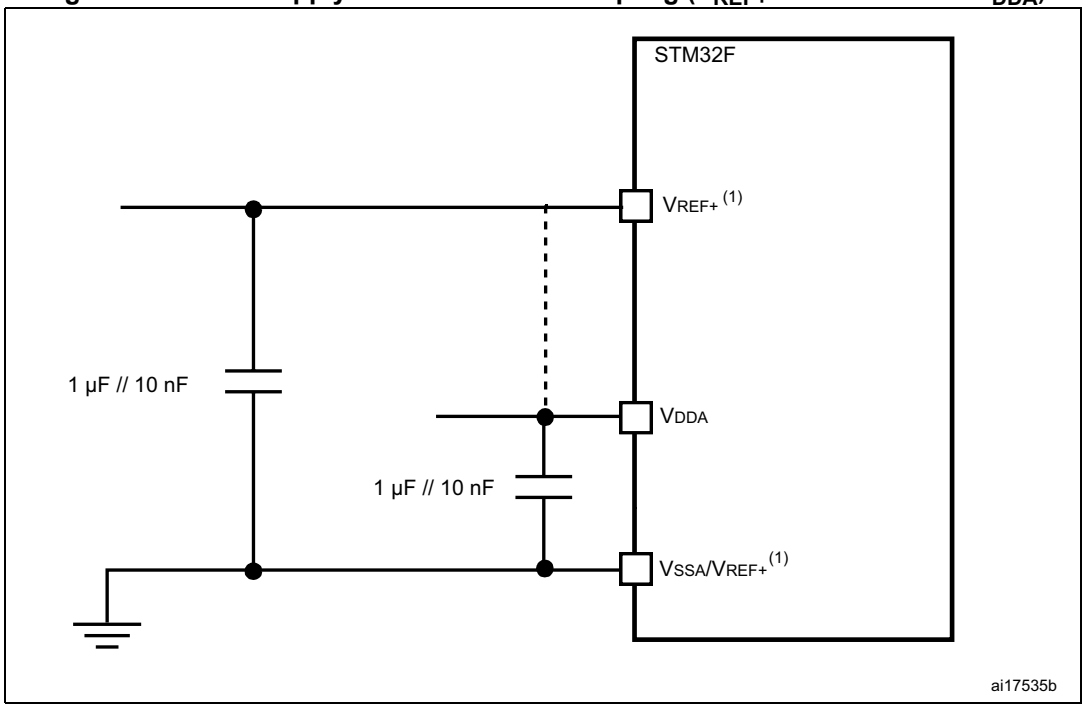
Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed based on test during characterization.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 47* or *Figure 48*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 47. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



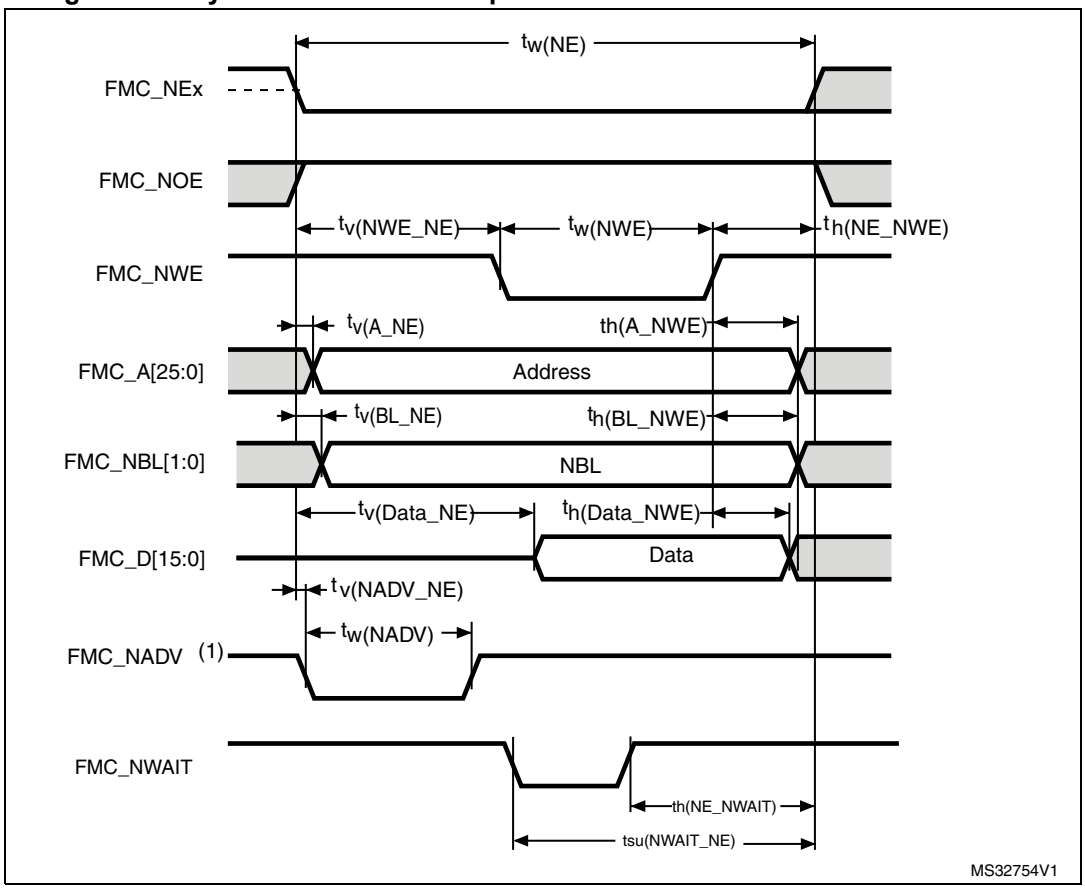
1. V_{REF+} and V_{REF-} inputs are both available on UFBGA144. V_{REF+} is also available on LQFP100, LQFP144, and WLCSP81. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
INL(4)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(4)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(4)	Gain error	-	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(4)	Total Harmonic Distortion Buffer ON	-	-	3	6	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
THD(4)	-	-	-	-	-	dB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	- 67	- 40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.16.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed based on test during characterization.

Figure 51. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

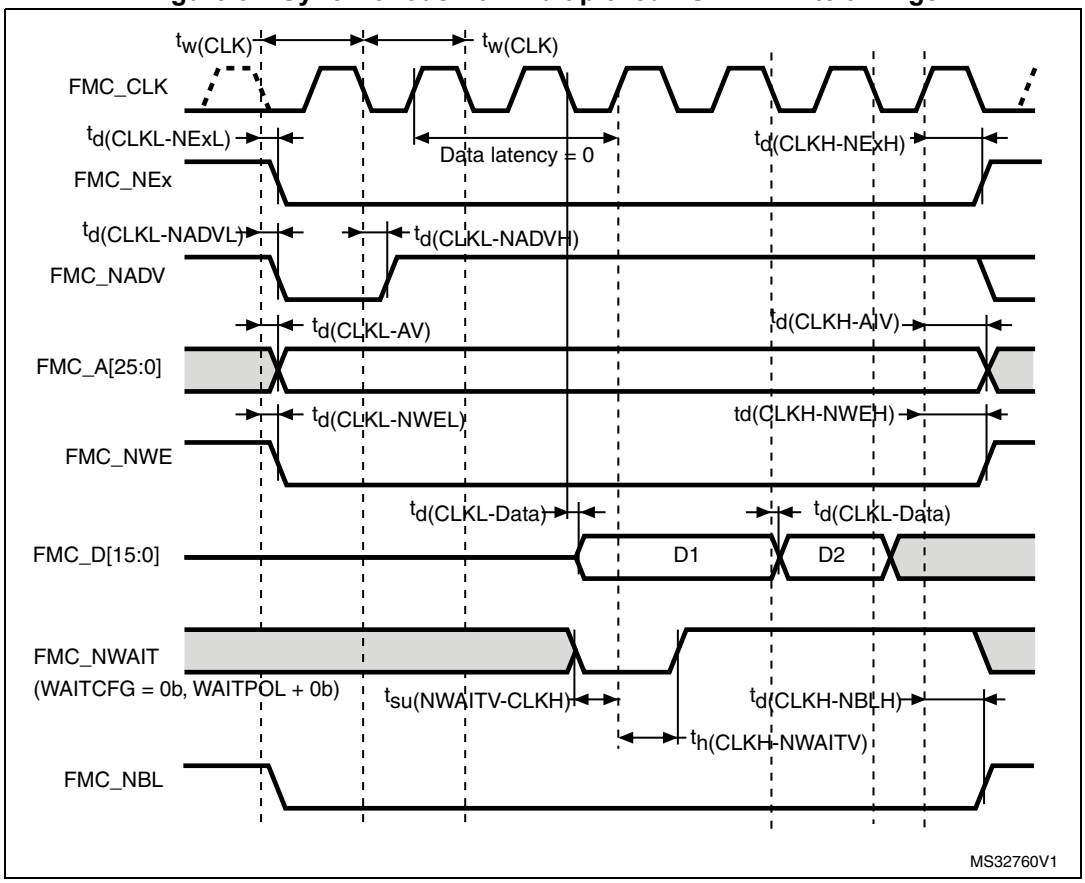
Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3 T_{HCLK} - 2	3 T_{HCLK} +0.5	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK} – 0.5	T_{HCLK} + 0.5	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}	T_{HCLK}+ 0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK} + 0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK} - 0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK} + 0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	T_{HCLK} + 2	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK} + 0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+ 0.5	

1. C_L = 30 pF.
2. Guaranteed based on test during characterization.

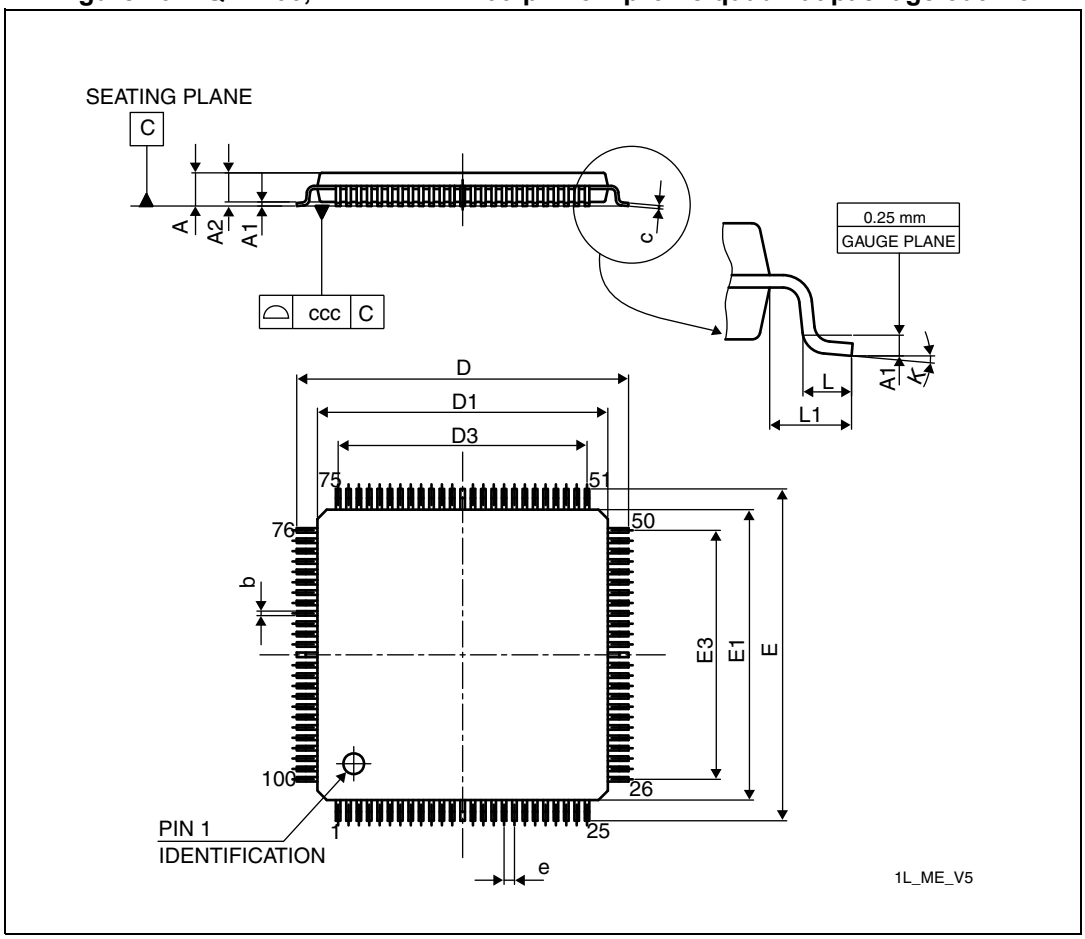
1. C_L = 30 pF.
2. Guaranteed based on test during characterization.

Figure 57. Synchronous non-multiplexed PSRAM write timings



7.2 LQFP100 package information

Figure 70. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 109. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

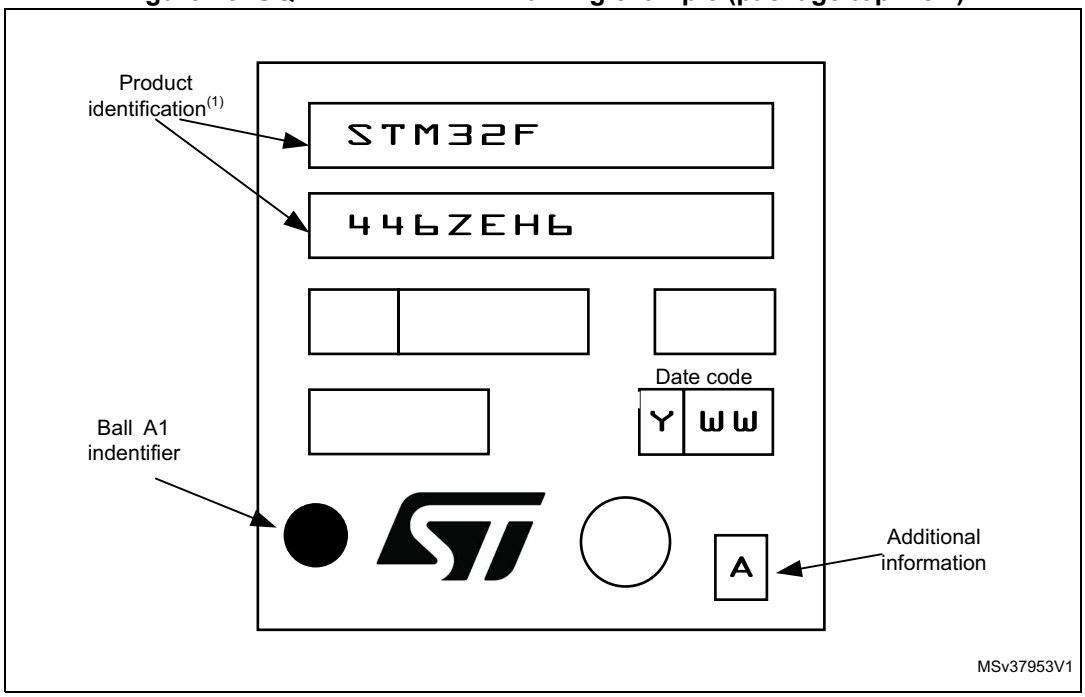
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Device marking for UFBGA144 7 x 7 mm package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 78. UQFP144 7 x 7 mm marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.