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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446rct7

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3.14 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial (UART, I²C, CAN, SPI and USB) communication interface. Refer to application note AN2606 for details.

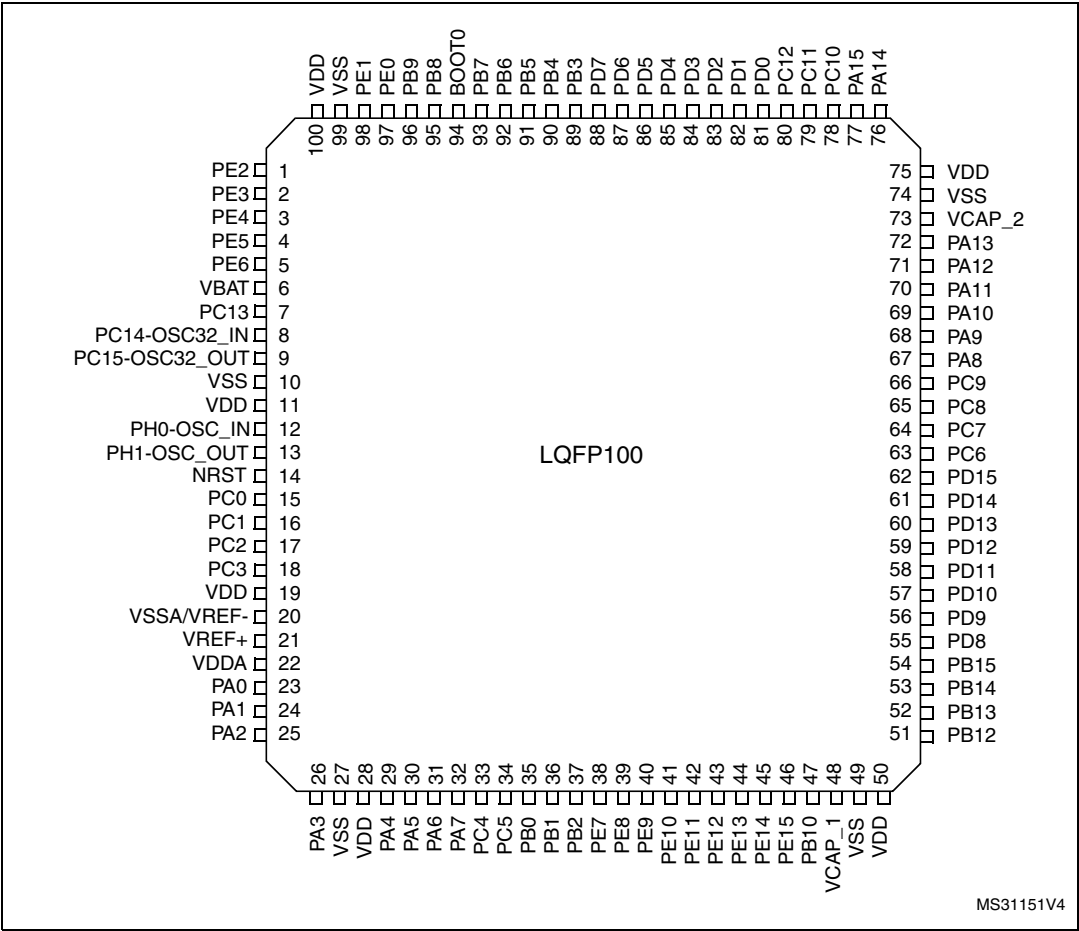
3.15 Power supply schemes

- $V_{DD} = 1.7$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.7$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.16.2: Internal reset OFF](#)). Refer to [Table 3: Voltage regulator configuration mode versus device operating mode](#) to identify the packages supporting this option.

- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers.
For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB} . When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions V_{DDUSB} must be respected:
 - During power-on phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
 - During power-down phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
 - V_{DDUSB} rising and falling time rate specifications must be respected.
 - In operating mode phase, V_{DDUSB} could be lower or higher than V_{DD} :
 - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX} . The V_{DDUSB} supply both USB transceiver (USB OTG_HS and USB OTG_FS).
 - If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB} .
 - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX} .

Figure 11. STM32F446xC/xE LQFP100 pinout



1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5V tolerant IO, I2C FM+ option
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F446xx pin and ball descriptions

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	1	D7	A3	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, FMC_A23, EVENTOUT	-
-	2	D6	A2	2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
-	3	A9	B2	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, EVENTOUT	-
-	4	-	B3	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, EVENTOUT	-

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	-	-	H6	61	VSS	S	-	-	-	-
-	-	-	G6	62	VDD	S	-	-	-	-
-	41	J4	J7	63	PE10	I/O	FT	-	TIM1_CH2N, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-
-	42	-	H8	64	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, SAI2_SD_B, FMC_D8, EVENTOUT	-
-	43	-	J8	65	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_D9, EVENTOUT	-
-	44	-	K8	66	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_D10, EVENTOUT	-
-	45	-	L8	67	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11, EVENTOUT	-
-	46	-	M8	68	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, EVENTOUT	-
29	47	H4	M9	69	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, SAI1_SCK_A, USART3_TX, OTG_HS_ULPI_D3, EVENTOUT	-
-	-	-	M10	70	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, USART3_RX, SAI2_SD_A, EVENTOUT	-
30	48	J3	H7	71	VCAP_1	S	-	-	-	-
31	49	H3	-	-	VSS	S	-	-	-	-
32	50	J2	G7	72	VDD	S	-	-	-	-
33	51	G4	M11	73	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SAI1_SCK_B, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, OTG_HS_ID, EVENTOUT	-

Table 21. reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{RUSH}^{(1)}$	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
$E_{RUSH}^{(1)}$	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	$V_{DD} = 1.7\text{ V}$, $T_A = 105\text{ }^{\circ}\text{C}$, $I_{RUSH} = 171\text{ mA}$ for $31\text{ }\mu\text{s}$	-	-	5.4	μC

1. Guaranteed based on test during characterization.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in [Table 22](#). They are subject to general operating conditions for T_A .

Table 22. Over-drive switching characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	μs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed based on test during characterization.

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 19: Current consumption measurement scheme](#).

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 29. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions ⁽¹⁾	Typ			Max ⁽²⁾		Unit
			T _A = 25 °C			T _A = 85 °C	T _A = 105 °C	
			V _{BAT} = 1.7 V	V _{BAT} = 2.4 V	V _{BAT} = 3.3 V	V _{BAT} = 3.6 V		
I _{DD_VBAT}	Backup domain supply current	Backup SRAM ON, RTC ON and LSE oscillator in low power mode	1.46	1.62	1.83	6	11	μA
		Backup SRAM OFF, RTC ON and LSE oscillator in low power mode	0.72	0.85	1.00	3	5	
		Backup SRAM ON, RTC ON and LSE oscillator in high drive mode	2.24	2.40	2.64	-	-	
		Backup SRAM OFF, RTC ON and LSE oscillator in high drive mode	1.50	1.64	1.86	-	-	
		Backup SRAM ON, RTC and LSE OFF	0.74	0.75	0.78	5	10	
		Backup SRAM OFF, RTC and LSE OFF	0.05	0.05	0.05	2	4	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.

2. Guaranteed based on test during characterization.

**Figure 21. Typical V_{BAT} current consumption
(RTC ON/backup RAM OFF and LSE in low power mode)**

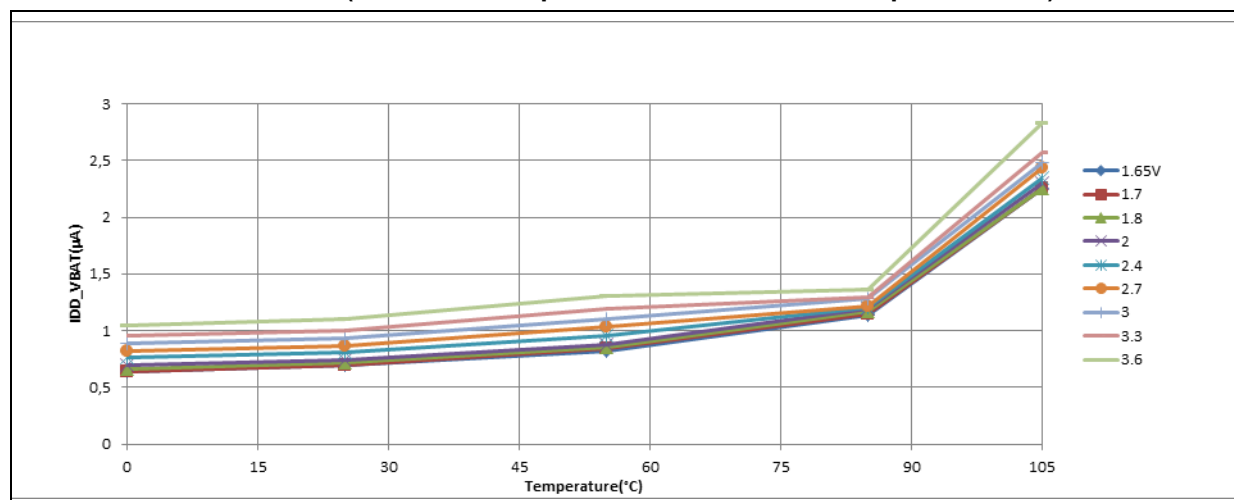


Table 34. Switching output I/O current consumption⁽¹⁾ (continued)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw)	Typ	Unit
I _{DDIO}	I/O switching Current	V _{DD} = 3.3 V C _{EXT} = 10 pF C = C _{INT} + C _{EXT} + C _S	2 MHz	0.18	mA
			8 MHz	0.67	
			25 MHz	2.09	
			50 MHz	3.6	
			60 MHz	4.5	
			84 MHz	7.8	
			90 MHz	9.8	
		V _{DD} = 3.3 V C _{EXT} = 22 pF C = C _{INT} + C _{EXT} + C _S	2 MHz	0.26	
			8 MHz	1.01	
			25 MHz	3.14	
			50 MHz	6.39	
			60 MHz	10.68	
		V _{DD} = 3.3 V C _{EXT} = 33 pF C = C _{INT} + C _{EXT} + C _S	2 MHz	0.33	
			8 MHz	1.29	
			25 MHz	4.23	
			50 MHz	11.02	

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).

2. This test is performed by cutting the LQFP144 package pin (pad removal).

On-chip peripheral current consumption

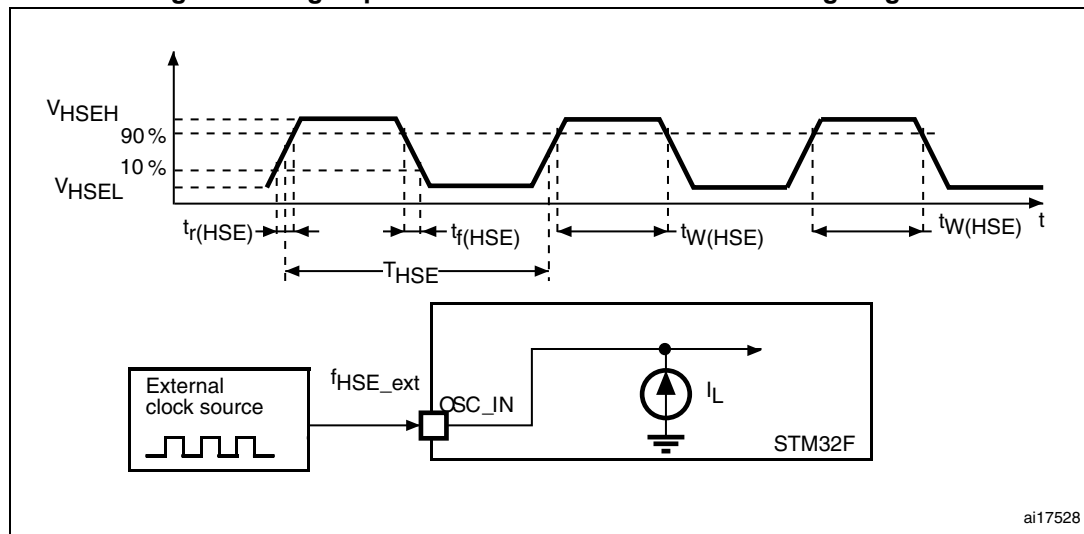
The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- HCLK is the system clock. f_{PCLK1} = f_{HCLK}/4, and f_{PCLK2} = f_{HCLK}/2.

The given value is calculated by measuring the difference of current consumption

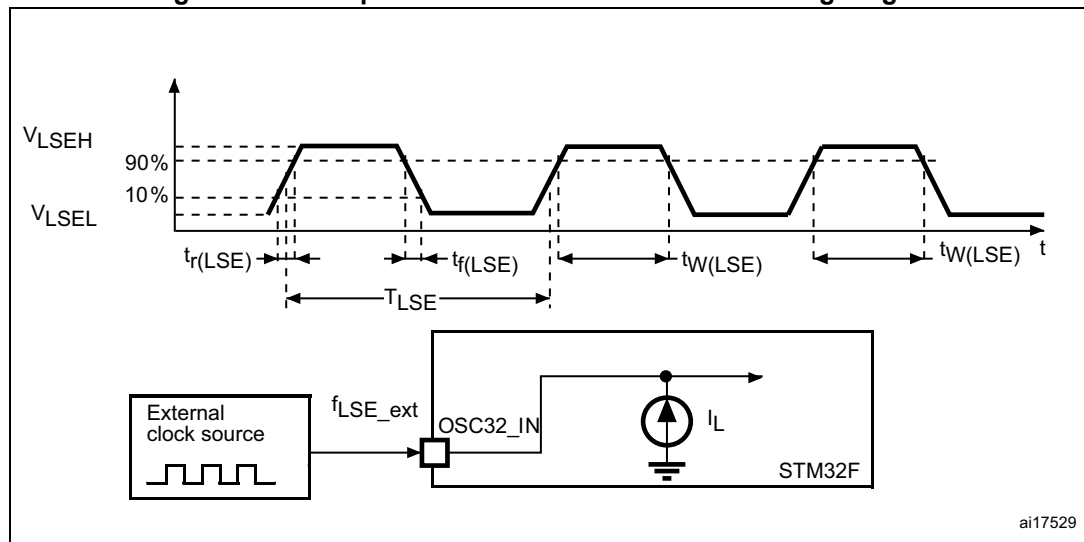
- with all peripherals clocked off
- with only one peripheral clocked on
- f_{HCLK} = 180 MHz (Scale1 + over-drive ON), f_{HCLK} = 144 MHz (Scale 2), f_{HCLK} = 120 MHz (Scale 3)"
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Figure 23. High-speed external clock source AC timing diagram



ai17528

Figure 24. Low-speed external clock source AC timing diagram



ai17529

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 39](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

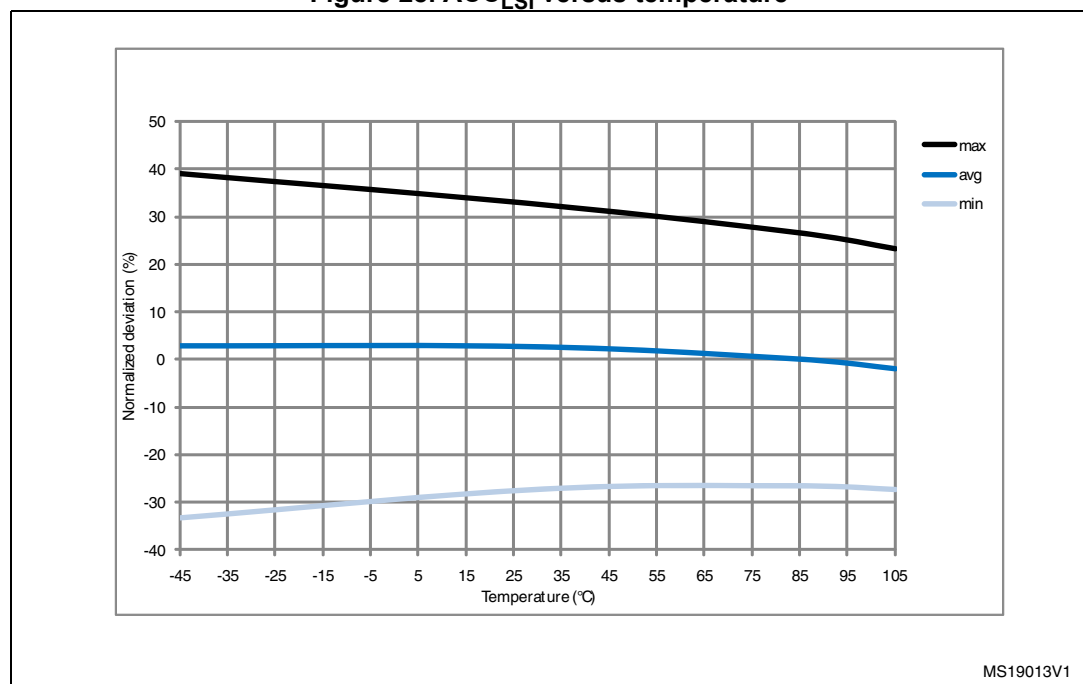
Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Frequency	17	32	47	kHz
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	15	40	μs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	0.4	0.6	μA

- $V_{DD} = 3 V$, $T_A = -40$ to $105^\circ C$ unless otherwise specified.
- Guaranteed based on test during characterization..
- Guaranteed by design.

Figure 28. ACC_{LSI} versus temperature



6.3.11 PLL characteristics

The parameters given in [Table 43](#) and [Table 44](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 16](#).

Table 43. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock ⁽¹⁾	-	0.95 ⁽²⁾	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	12.5	-	180	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	MHz
f_{VCO_OUT}	PLL VCO output	-	100	-	432	MHz

Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
INL ⁽⁴⁾	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset ⁽⁴⁾	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	-	±3	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6$ V
		-	-	-	±12	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6$ V
Gain error ⁽⁴⁾	Gain error	-	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$ ⁽⁴⁾	Total Harmonic Distortion Buffer ON	-	-	3	6	μs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
THD ⁽⁴⁾	-	-	-	-	-	dB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate ⁽²⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP} ⁽⁴⁾	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	μs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ ⁽²⁾	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	- 67	- 40	dB	No R_{LOAD} , $C_{LOAD} = 50$ pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.16.2: Internal reset OFF](#)).

2. Guaranteed by design.

3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.

4. Guaranteed based on test during characterization.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK} - 0.5$	$8T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK} - 0.5$	$6T_{HCLK} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} - 0.5$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 2$	-	

1. $C_L = 30$ pF.

2. Guaranteed based on test during characterization.

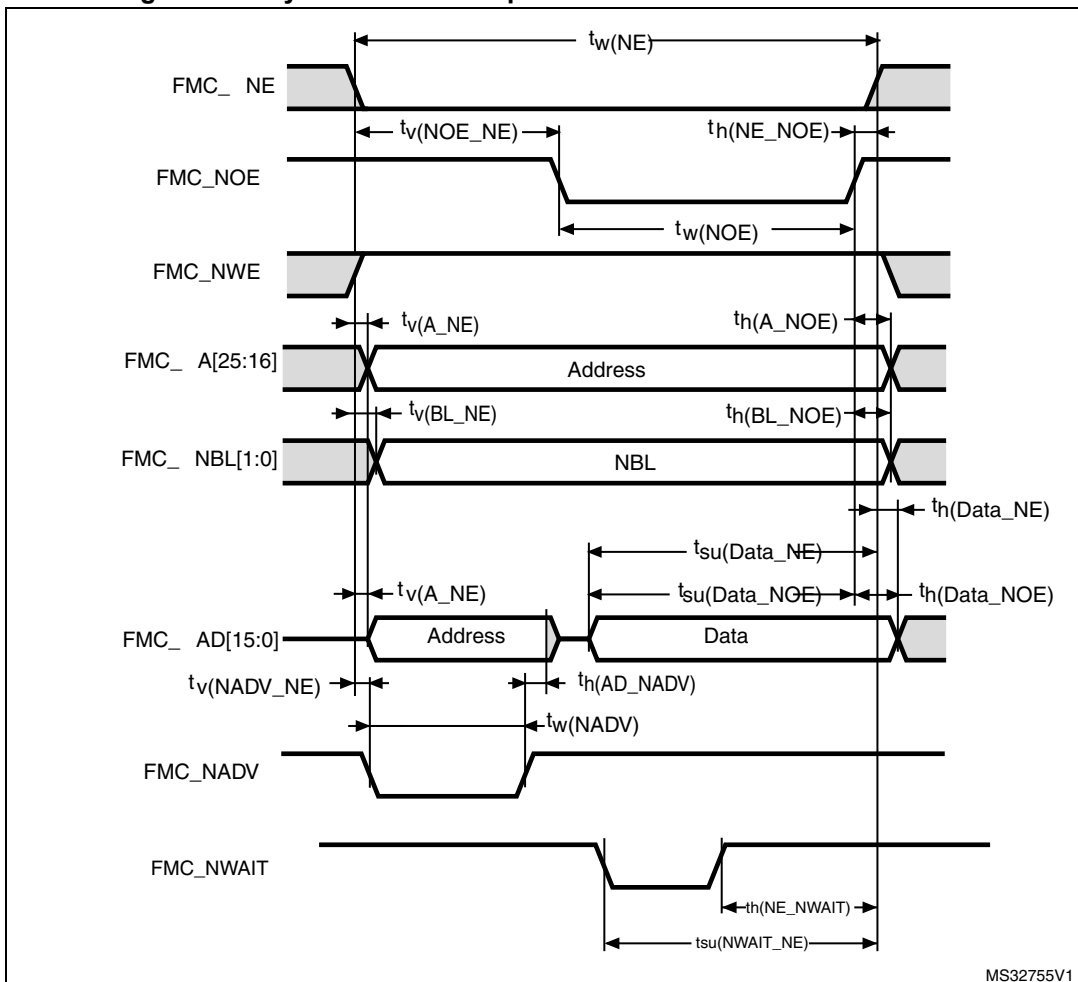
Figure 52. Asynchronous multiplexed PSRAM/NOR read waveforms

Table 94. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low ($x=0..2$)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high ($x=0..2$)	$T_{HCLK} - 0.5$	-	
$t_{d(CLKL-NADV_L)}$	FMC_CLK low to FMC_NADV low	-	0	
$t_{d(CLKL-NADV_H)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid ($x=16..25$)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid ($x=16..25$)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	0.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1	-	
$t_h(CLKH-ADV)$	FMC_A/D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1	-	
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. $C_L = 30$ pF.

2. Guaranteed based on test during characterization.

Figure 60. NAND controller waveforms for common memory read access

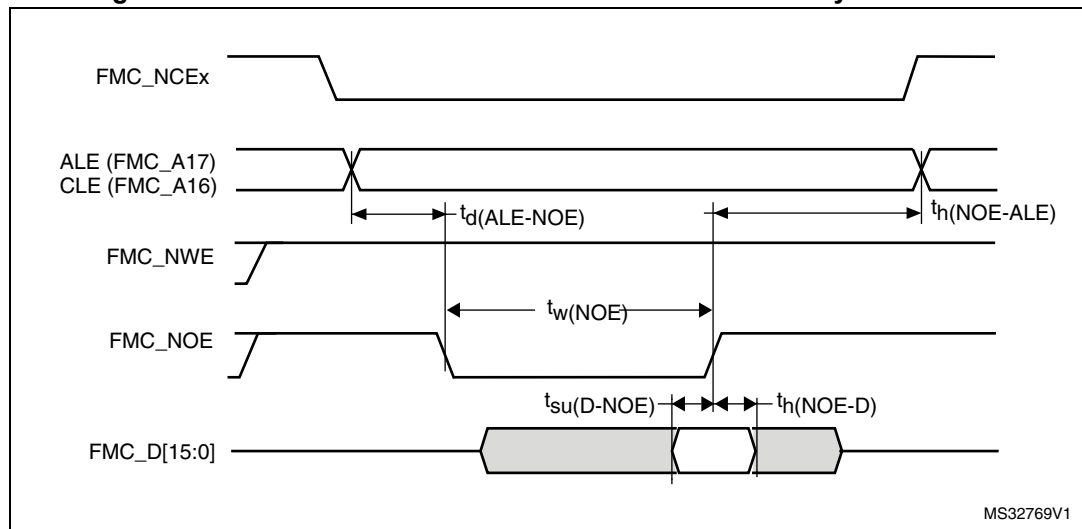
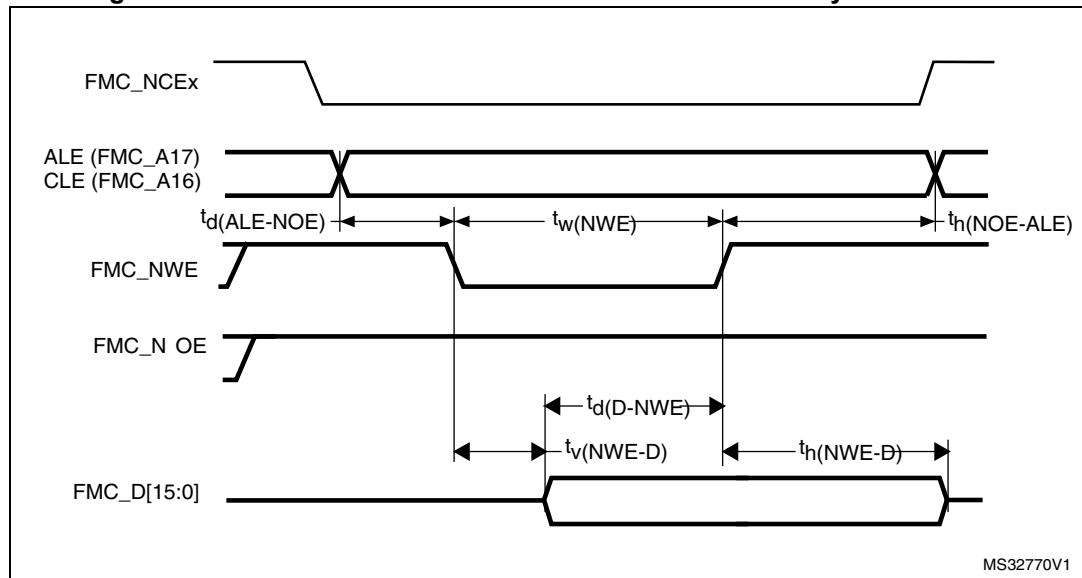


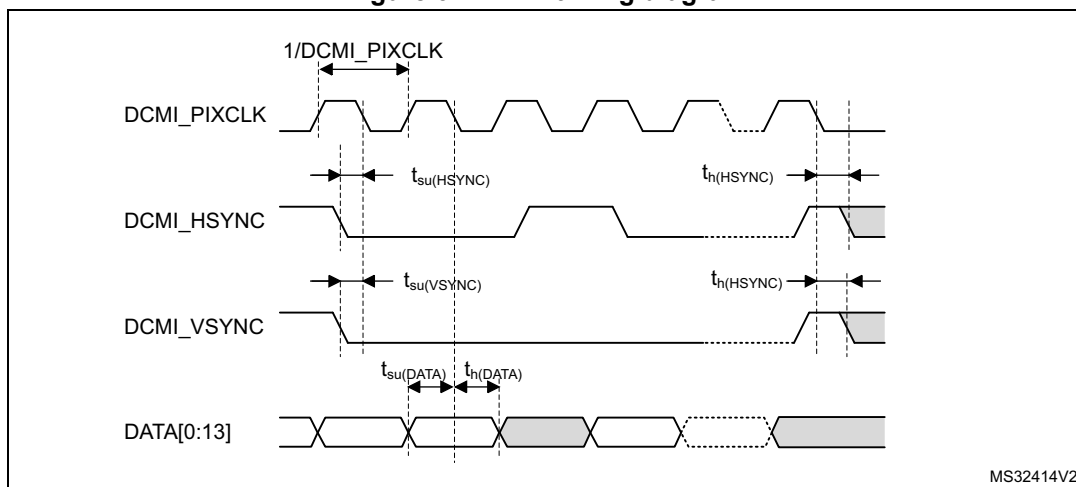
Figure 61. NAND controller waveforms for common memory write access

Table 98. Switching characteristics for NAND Flash read cycles⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FMC_NOE low width	$4T_{HCLK} - 0.5$	$4T_{HCLK} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15:0] valid data before FMC_NOE high	9	-	
$t_{h(NOE-D)}$	FMC_D[15:0] valid data after FMC_NOE high	2.5	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{HCLK} - 0.5$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK} - 2$	-	

1. $C_L = 30$ pF.

Figure 64. DCMI timing diagram



6.3.28 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 105](#) for the SDIO are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in [Table 16](#), with the following configuration:

- Output speed is set to $\text{OSPEEDRy}[1:0] = 10$
- Capacitive load $C = 30 \text{ pF}$
- Measurement points are done at CMOS levels: $0.5V_{\text{DD}}$

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

Figure 65. SDIO high-speed mode

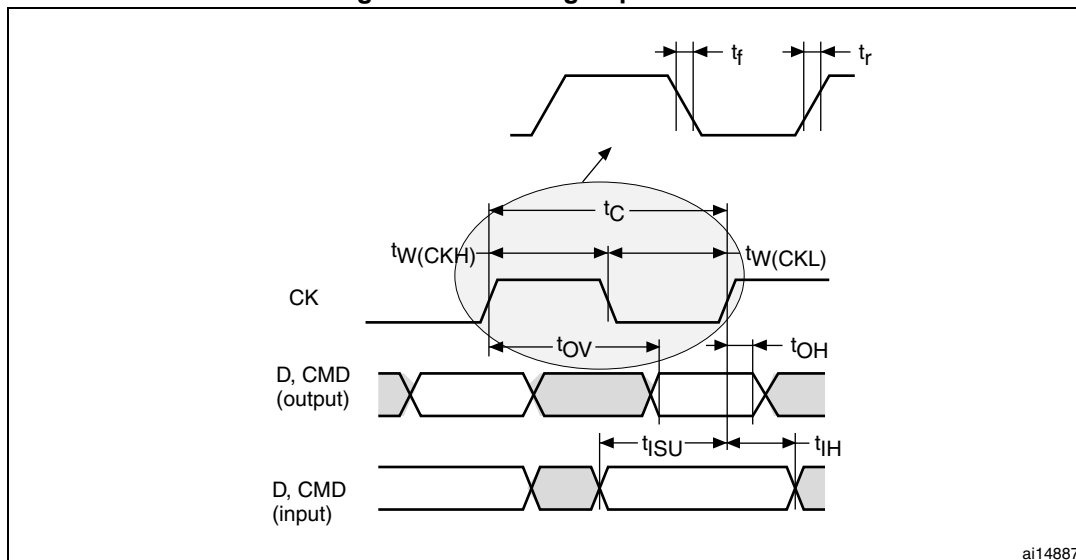
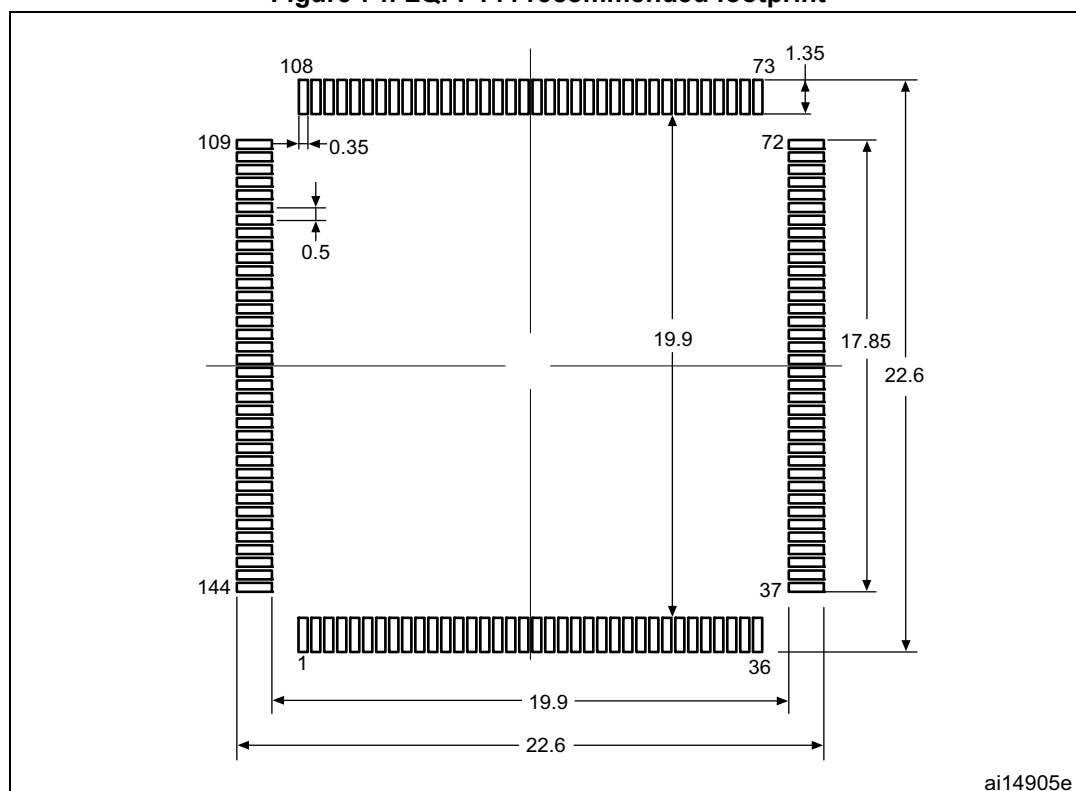


Figure 74. LQFP144 recommended footprint



1. Dimensions are expressed in millimeters.

7.4 UFBGA144 7 x 7 mm package information

Figure 76. UFBGA144 - 144-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline

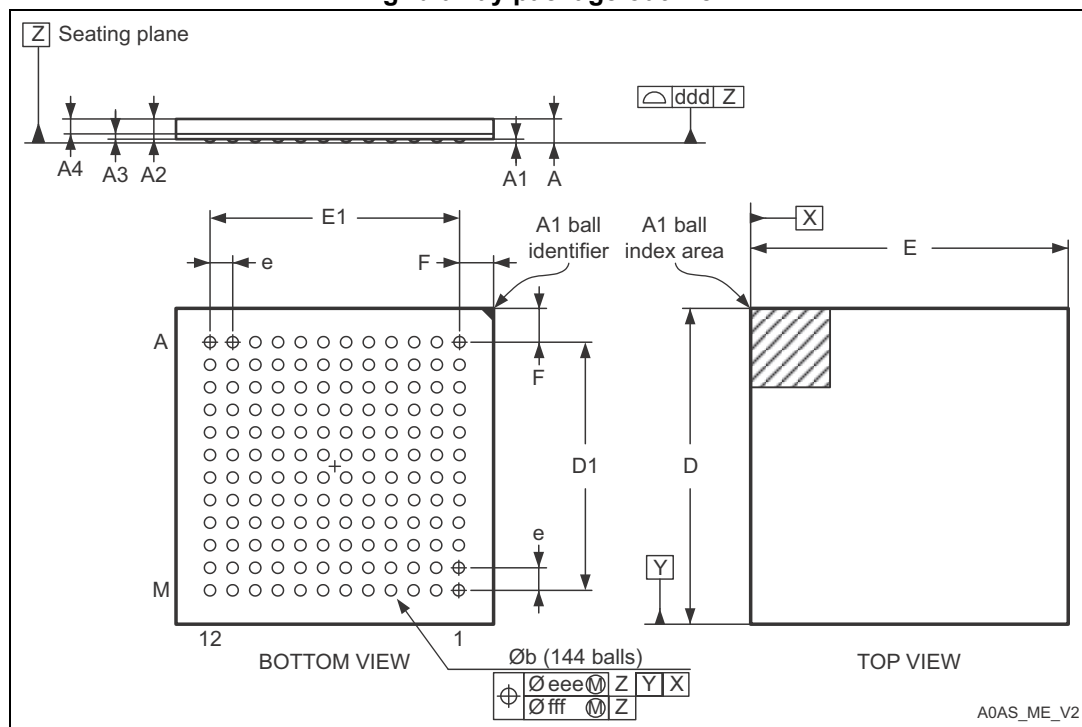


Table 111. UFBGA144 - 144-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.320	0.0091	0.0110	0.0126
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

8 Part numbering

Table 118. Ordering information scheme

Example:	STM32	F	446	V	C	T	6	xxx
Device family								
STM32 = ARM-based 32-bit microcontroller								
Product type								
F = general-purpose								
Device subfamily								
446= STM32F446xC/E,								
Pin count								
M = 81 pins								
R = 64 pins								
V = 100 pins								
Z = 144 pins								
Flash memory size								
C=256 Kbytes of Flash memory								
E=512 Kbytes of Flash memory								
Package								
H = UFBGA (7 x 7 mm)								
J = UFBGA (10 x 10 mm)								
T = LQFP								
Y = WLCSP								
Temperature range								
6 = Industrial temperature range, –40 to 85 °C.								
7 = Industrial temperature range, –40 to 105 °C.								
Options								
xxx = programmed parts								
TR = tape and reel								

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

