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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446ret7

6.1.2	Typical values	72
6.1.3	Typical curves	72
6.1.4	Loading capacitor	72
6.1.5	Pin input voltage	72
6.1.6	Power supply scheme	73
6.1.7	Current consumption measurement	74
6.2	Absolute maximum ratings	74
6.3	Operating conditions	76
6.3.1	General operating conditions	76
6.3.2	VCAP_1/VCAP_2 external capacitor	78
6.3.3	Operating conditions at power-up / power-down (regulator ON)	79
6.3.4	Operating conditions at power-up / power-down (regulator OFF)	79
6.3.5	Reset and power control block characteristics	80
6.3.6	Over-drive switching characteristics	81
6.3.7	Supply current characteristics	81
6.3.8	Wakeup time from low-power modes	101
6.3.9	External clock source characteristics	102
6.3.10	Internal clock source characteristics	107
6.3.11	PLL characteristics	108
6.3.12	PLL spread spectrum clock generation (SSCG) characteristics	110
6.3.13	Memory characteristics	112
6.3.14	EMC characteristics	114
6.3.15	Absolute maximum ratings (electrical sensitivity)	116
6.3.16	I/O current injection characteristics	117
6.3.17	I/O port characteristics	118
6.3.18	NRST pin characteristics	123
6.3.19	TIM timer characteristics	124
6.3.20	Communications interfaces	124
6.3.21	12-bit ADC characteristics	141
6.3.22	Temperature sensor characteristics	147
6.3.23	V _{BAT} monitoring characteristics	148
6.3.24	Reference voltage	148
6.3.25	DAC electrical characteristics	148
6.3.26	FMC characteristics	152
6.3.27	Camera interface (DCMI) timing specifications	172
6.3.28	SD/SDIO MMC card host interface (SDIO) characteristics	173
6.3.29	RTC characteristics	175

Figure 2. Compatible board for LQFP64 package

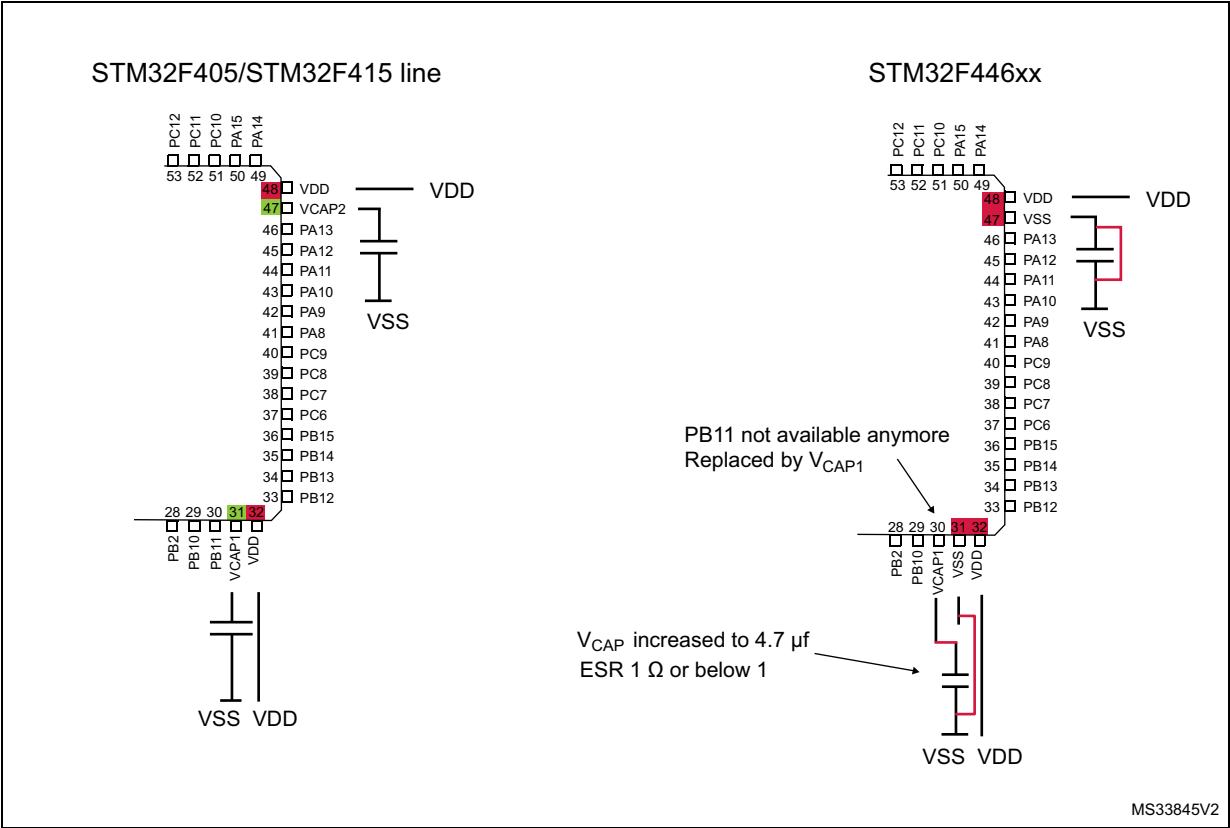


Figure 3 shows the STM32F446xx block diagram.

3.19 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

3.20 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

3.21 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

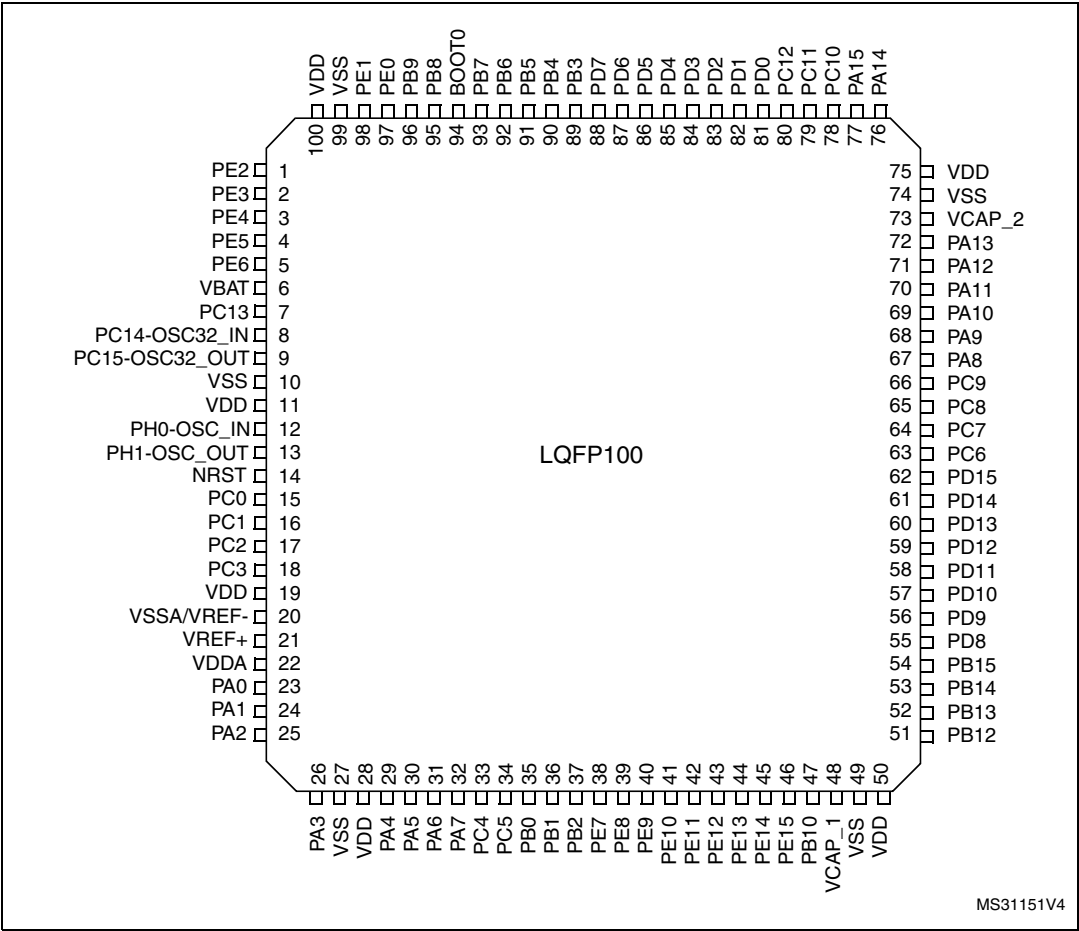
[Table 6](#) compares the features of the advanced-control, general-purpose and basic timers.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) ⁽¹⁾
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	90	180
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	90	180
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	90	180
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	45	90/180
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	45	90/180
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	45	90/180

1. The maximum timer clock is either 90 or 180 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

Figure 11. STM32F446xC/xE LQFP100 pinout



1. The above figure shows the package top view.

PA 3 37
 V_{SS} 38
 V_{DD} 39
 PA 4 40
 PA 5 41
 PA 6 42
 PA 7 43
 PC 4 44
 PC 5 45
 PB 0 46
 PB 1 47
 PB 2 48
 PF 11 49
 PF 12 50
 V_{SS} 51
 V_{DD} 52
 PF 13 53
 PF 14 54
 PF 15 55
 PG 0 56
 PG 1 57
 PE 7 58
 PE 8 59
 PE 9 60
 V_{SS} 61
 V_{DD} 62
 PE 10 63
 PE 11 64
 PE 12 65
 PE 13 66
 PE 14 67
 PE 15 68
 PB 10 69
 PB 11 70
 V_{CAP1} 71
 V_{DD} 72

144 V_{DD}
 143 PDR_ON
 142 PE 1
 141 PE 0
 140 PB 9
 139 PB 8
 138 BOOT0
 137 PB 7
 136 PB 6
 135 PB 5
 134 PB 4
 133 PB 3
 132 PG 15
 131 V_{DD}
 130 V_{SS}
 129 PG 14
 128 PG 13
 127 PG 12
 126 PG 11
 125 PG 10
 124 PG 9
 123 PD 7
 122 PD 6
 121 V_{DD}
 120 V_{SS}
 119 PD 5
 118 PD 4
 117 PD 3
 116 PD 2
 115 PD 1
 114 PD 0
 113 PC 12
 112 PC 11
 111 PC 10
 110 PA 15
 109 PA 14

108 V_{DD}
 107 V_{SS}
 106 V_{CAP2}
 105 PA 13
 104 PA 12
 103 PA 11
 102 PA 10
 101 PA 9
 100 PA 8
 99 PC 9
 98 PC 8
 97 PC 7
 96 PC 6
 95 V_{DDUSB}
 94 V_{SS}
 93 PG 8
 92 PG 7
 91 PG 6
 90 PG 5
 89 PG 4
 88 PG 3
 87 PG 2
 86 PD 15
 85 PD 14
 84 V_{DD}
 83 V_{SS}
 82 PD 13
 81 PD 12
 80 PD 11
 79 PD 10
 78 PD 9
 77 PD 8
 76 PB 15
 75 PB 14
 74 PB 13
 73 PB 12

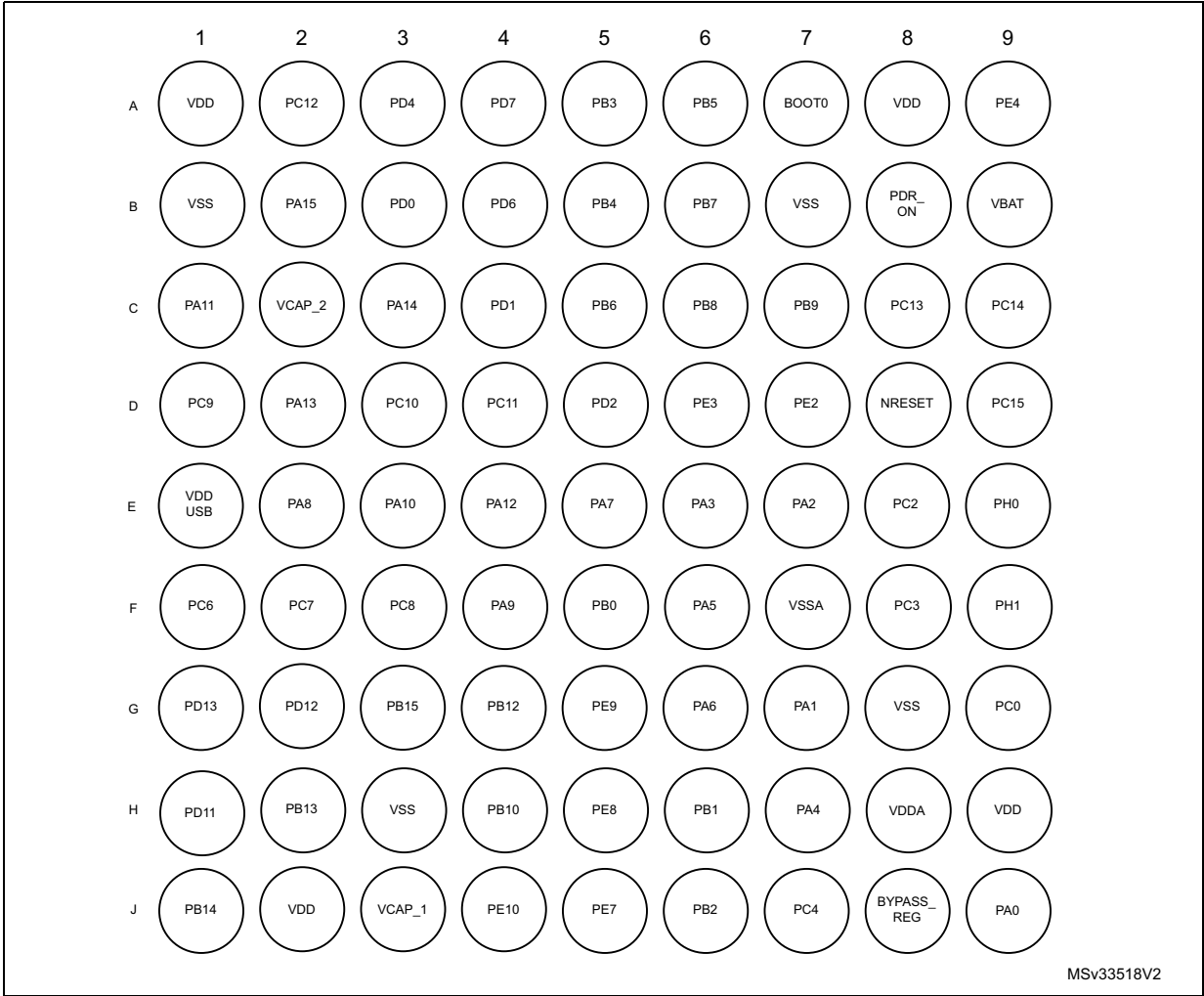
PE 2 1
 PE 3 2
 PE 4 3
 PE 5 4
 PE 6 5
 VBAT 6
 PC 13 7
 PC 14 8
 PC 15 9
 PF 0 10
 PF 1 11
 PF 2 12
 PF 3 13
 PF 4 14
 PF 5 15
 V_{SS} 16
 V_{DD} 17
 PF 6 18
 PF 7 19
 PF 8 20
 PF 9 21
 PF 10 22
 PH 0 23
 PH 1 24
 NRST 25
 PC 0 26
 PC 1 27
 PC 2 28
 PC 3 29
 V_{DD} 30
 V_{SSA} 31
 V_{REF+} 32
 V_{DDA} 33
 PA 0 34
 PA 1 35
 PA 2 36

LQFP144

ai18496c



Figure 13. STM32F446xC/xE WLCSP81 ballout



1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5V tolerant IO, I2C FM+ option
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F446xx pin and ball descriptions

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	1	D7	A3	1	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, FMC_A23, EVENTOUT	-
-	2	D6	A2	2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
-	3	A9	B2	3	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCM1_D4, EVENTOUT	-
-	4	-	B3	4	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCM1_D6, EVENTOUT	-

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
17	26	E6	M2	37	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, SAI1_FS_A, USART2_RX, OTG_HS_ULPI_D0, EVENTOUT	ADC123_IN3
18	27	-	G4	38	VSS	S	-	-	-	-
-	-	J8	H5	-	BYPASS_REG	I	FT	-	-	-
19	28	-	F4	39	VDD	S	-	-	-	-
20	29	H7	J3	40	PA4	I/O	TC	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNCR, EVENTOUT	ADC12_IN4, DAC_OUT1
21	30	F6	K3	41	PA5	I/O	TC	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, EVENTOUT	ADC12_IN5, DAC_OUT2
22	31	G6	L3	42	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, I2S2_MCK, TIM13_CH1, DCMI_PIXCLK, EVENTOUT	ADC12_IN6
23	32	E5	M3	43	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, FMC_SDNWE, EVENTOUT	ADC12_IN7
24	33	J7	J4	44	PC4	I/O	FT	-	I2S1_MCK, SPDIFRX_IN2, FMC_SDNE0, EVENTOUT	ADC12_IN14
25	34	-	K4	45	PC5	I/O	FT	-	USART3_RX, SPDIFRX_IN3, FMC_SDCKE0, EVENTOUT	ADC12_IN15

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	61	-	K11	85	PD14	I/O	FTf	-	TIM4_CH3, FMPI2C1_SCL, SAI2_SCK_A, FMC_D0, EVENTOUT	-
-	62	-	K12	86	PD15	I/O	FTf	-	TIM4_CH4, FMPI2C1_SDA, FMC_D1, EVENTOUT	-
-	-	-	J12	87	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	-	-	J11	88	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	-	-	J10	89	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	-	-	H12	90	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, DCMI_D12, EVENTOUT	-
-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, FMC_INT, DCMI_D13, EVENTOUT	-
-	-	-	G11	93	PG8	I/O	FT	-	SPDIFRX_IN2, USART6_RTS, FMC_SDCLK, EVENTOUT	-
-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	F10	-	VDD	S	-	-	-	-
-	-	E1	C11	95	VDDUSB	S	-	-	-	-
37	63	F1	G12	96	PC6	I/O	FTf	-	TIM3_CH1, TIM8_CH1, FMPI2C1_SCL, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, EVENTOUT	-
38	64	F2	F12	97	PC7	I/O	FTf	-	TIM3_CH2, TIM8_CH2, FMPI2C1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, SPDIFRX_IN1, USART6_RX, SDIO_D7, DCMI_D1, EVENTOUT	-
39	65	F3	F11	98	PC8	I/O	FT	-	TRACED0, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	6	6	CPU clock cycle
$T_{WUSLEEPFDSM}^{(1)}$	Wakeup from Sleep with Flash memory in Deep power down mode	-	33.5	50	μs
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	12.8	15	
		Main regulator is ON and Flash memory in Deep power down mode	104.9	115	
		Low power regulator is ON	20.6	28	
		Low power regulator is ON and Flash memory in Deep power down mode	112.8	120	
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	110	140	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	114.4	128	
$t_{WUSTDBY}^{(2)(3)}$	Wakeup from Standby mode	-	325	400	

1. Guaranteed based on test during characterization.

2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

3. $t_{WUSTDBY}$ maximum value is given at $-40\text{ }^{\circ}\text{C}$.

6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 56: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 23](#).

The characteristics given in [Table 37](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 16](#).

Table 48. Flash memory programming

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100 ⁽²⁾	μs
$t_{\text{ERASE16KB}}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{\text{ERASE64KB}}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{\text{ERASE128KB}}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	8	16	s
		Program/erase parallelism (PSIZE) = x 16	-	5.5	11	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed based on test during characterization.

2. The maximum programming time is measured after 100K erase operations.

Table 49. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t_{prog}	Double word programming	$T_{\text{A}} = 0 \text{ to } +40 \text{ }^{\circ}\text{C}$ $V_{\text{DD}} = 3.3 \text{ V}$ $V_{\text{PP}} = 8.5 \text{ V}$	-	16	100 ⁽²⁾	μs
$t_{\text{ERASE16KB}}$	Sector (16 KB) erase time		-	230	-	ms
$t_{\text{ERASE64KB}}$	Sector (64 KB) erase time		-	490	-	
$t_{\text{ERASE128KB}}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	3.5	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V

FMPI²C characteristics

The FMPI2C characteristics are described in [Table 62](#).

Refer also to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 62. FMPI²C characteristics⁽¹⁾

-	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
f _{FMPI2CC}	F _{FMPI2CCLK} frequency	2	-	8	-	17 16 ⁽²⁾	-	us
t _{w(SCLL)}	SCL clock low time	4.7	-	1.3	-	0.5	-	
t _{w(SCLH)}	SCL clock high time	4.0	-	0.6	-	0.26	-	
t _{su(SDA)}	SDA setup time	0.25	-	0.10	-	0.05	-	
t _{H(SDA)}	SDA data hold time	0	-	0	-	0	-	
t _{v(SDA,ACK)}	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time	-	0.100	-	0.30	-	0.12	
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time	-	0.30	-	0.30	-	0.12	
t _{h(STA)}	Start condition hold time	4	-	0.6	-	0.26	-	
t _{su(STA)}	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
t _{su(STO)}	Stop condition setup time	4	-	0.6	-	0.26	-	
t _{w(STO:STA)}	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
t _{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.09	0.05	0.09	pF
C _b	Capacitive load for each bus Line	-	400	-	400	-	550 ⁽³⁾	

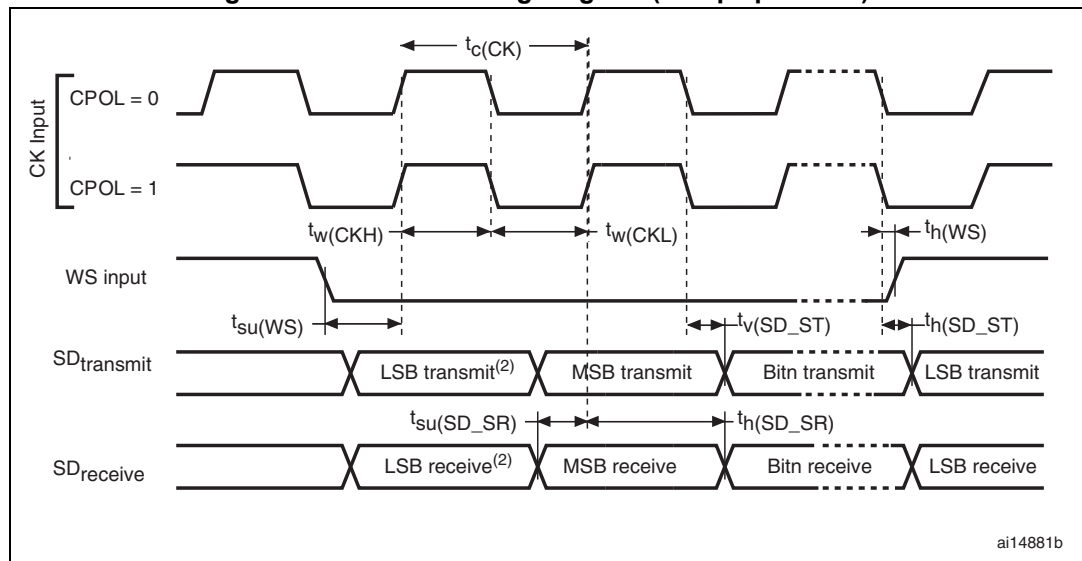
1. Guaranteed based on test during characterization.

2. When tr(SDA,SCL)≤110ns.

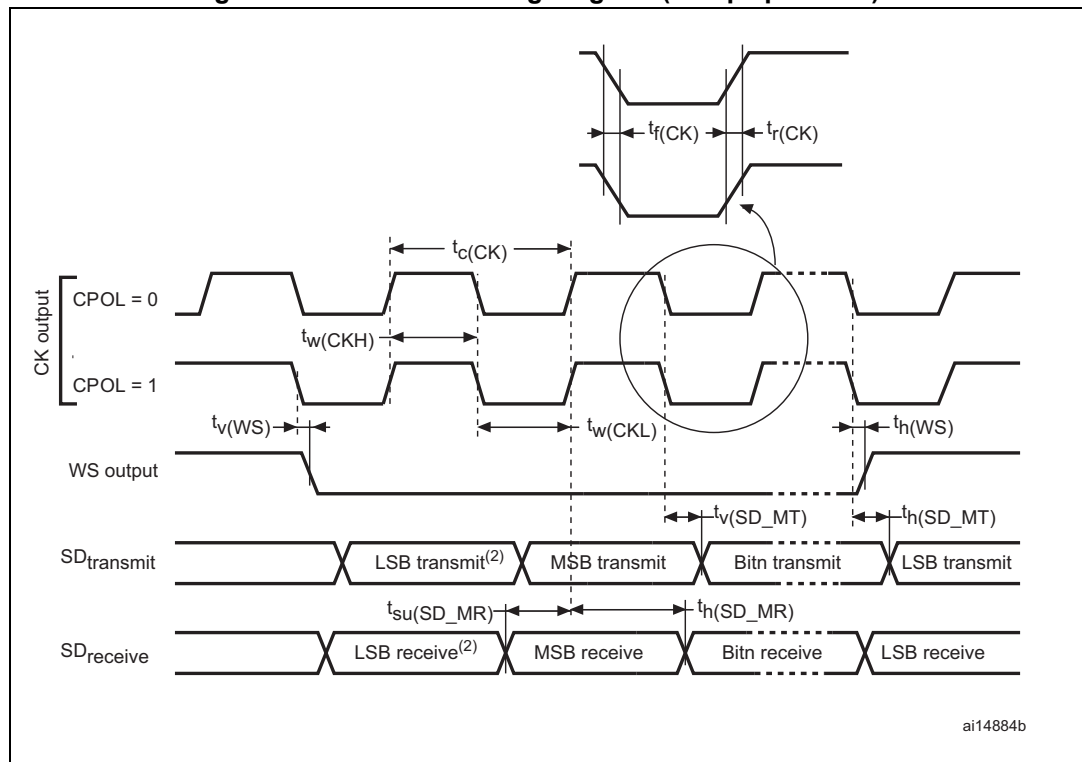
3. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:

$$t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$$

$$R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$$

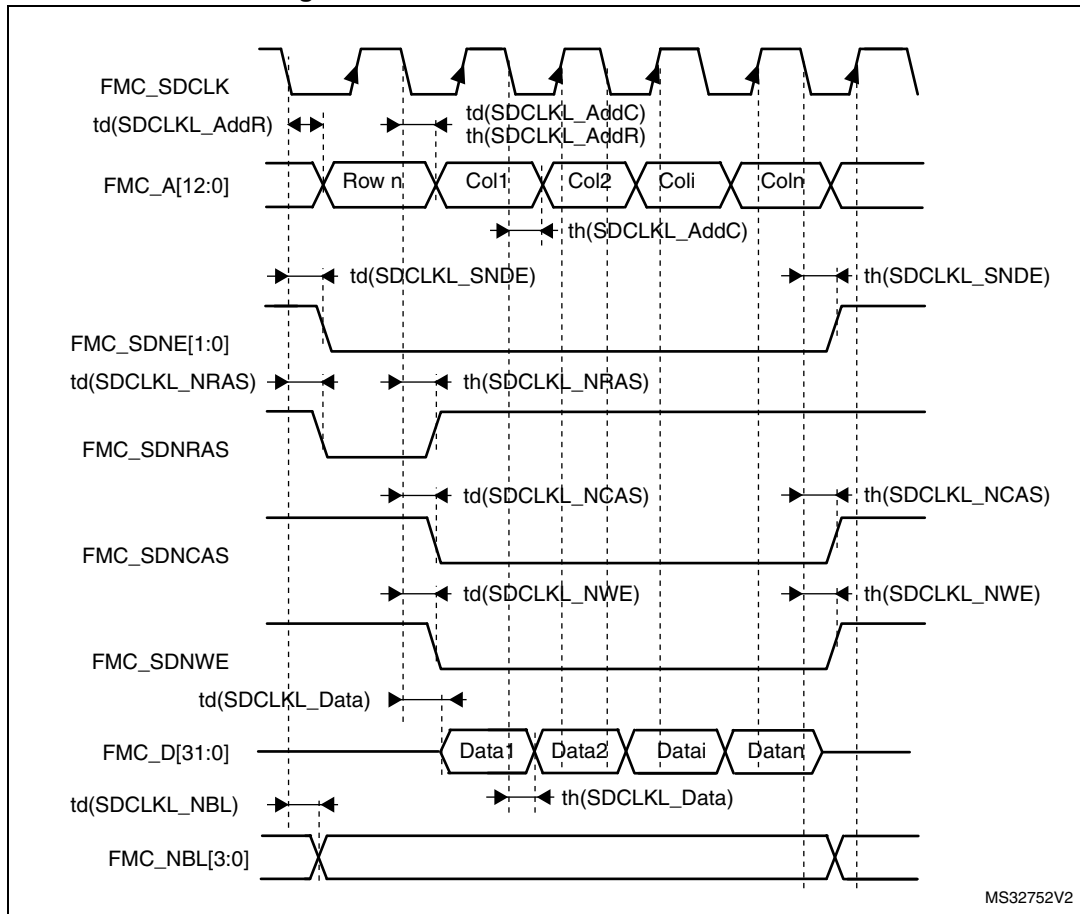
Figure 39. I²S slave timing diagram (Philips protocol)⁽¹⁾

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 40. I²S master timing diagram (Philips protocol)⁽¹⁾

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 63. SDRAM write access waveforms

Table 102. SDRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$F_{(SDCLK)}$	Frequency of operation	-	90	MHz
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	2	
$t_{h(SDCLKL_Data)}$	Data output hold time	0.5	-	
$t_{d(SDCLK_Add)}$	Address valid time	-	3	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. $C_L = 10$ pF on data and address line. $C_L = 15$ pF on FMC_SDCLK.

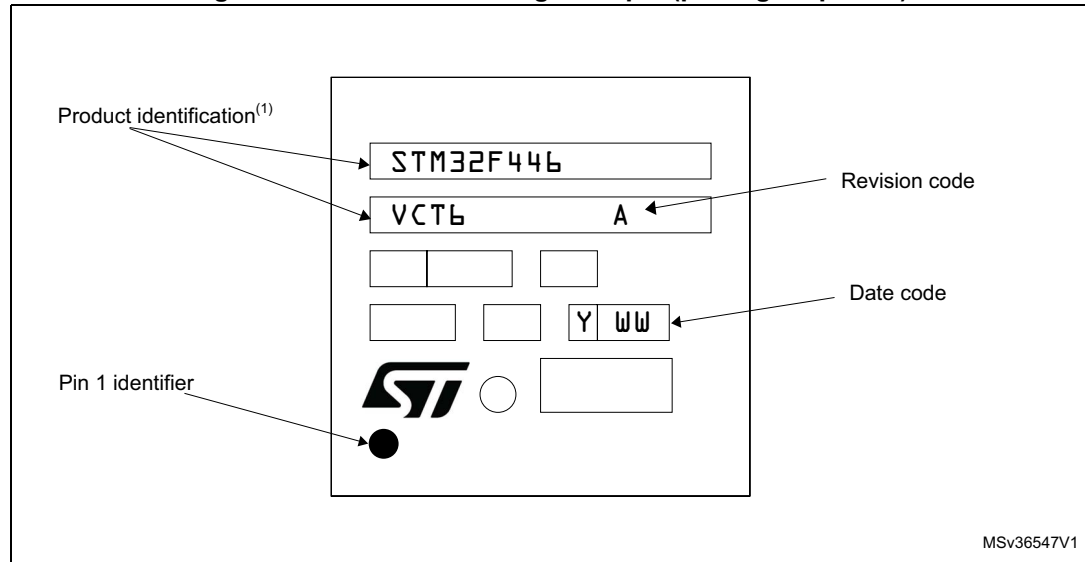
2. Guaranteed based on test during characterization.

Device marking for LQFP100 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 72. LQFP100 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 UFBGA144 7 x 7 mm package information

Figure 76. UFBGA144 - 144-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline

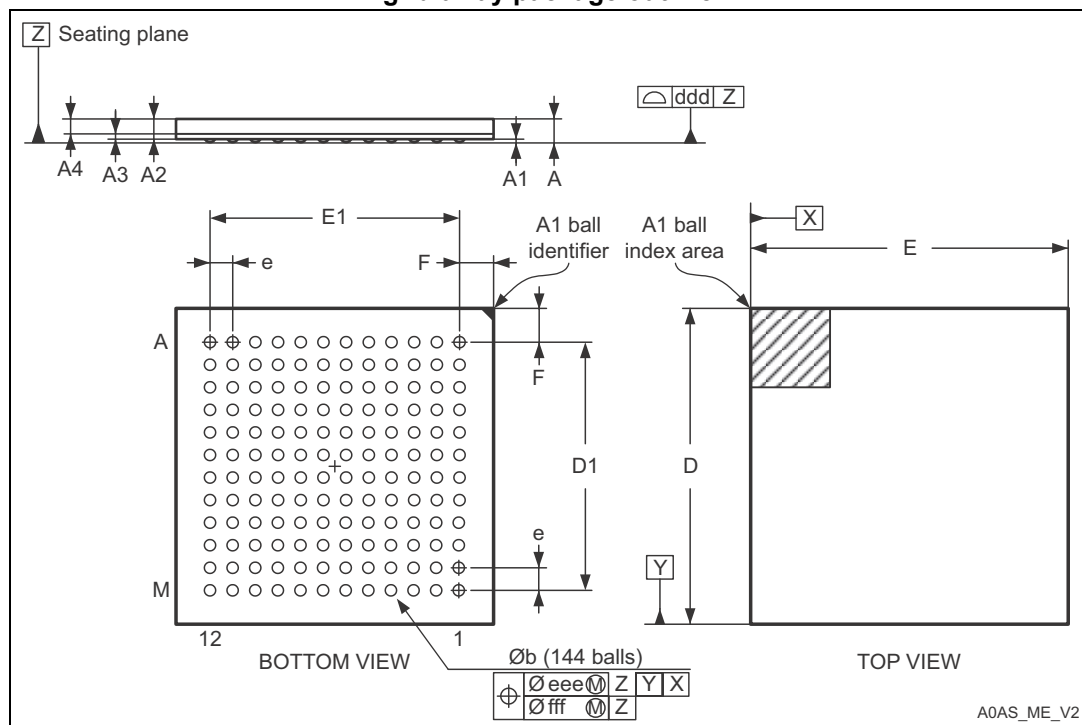


Table 111. UFBGA144 - 144-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.320	0.0091	0.0110	0.0126
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

8 Part numbering

Table 118. Ordering information scheme

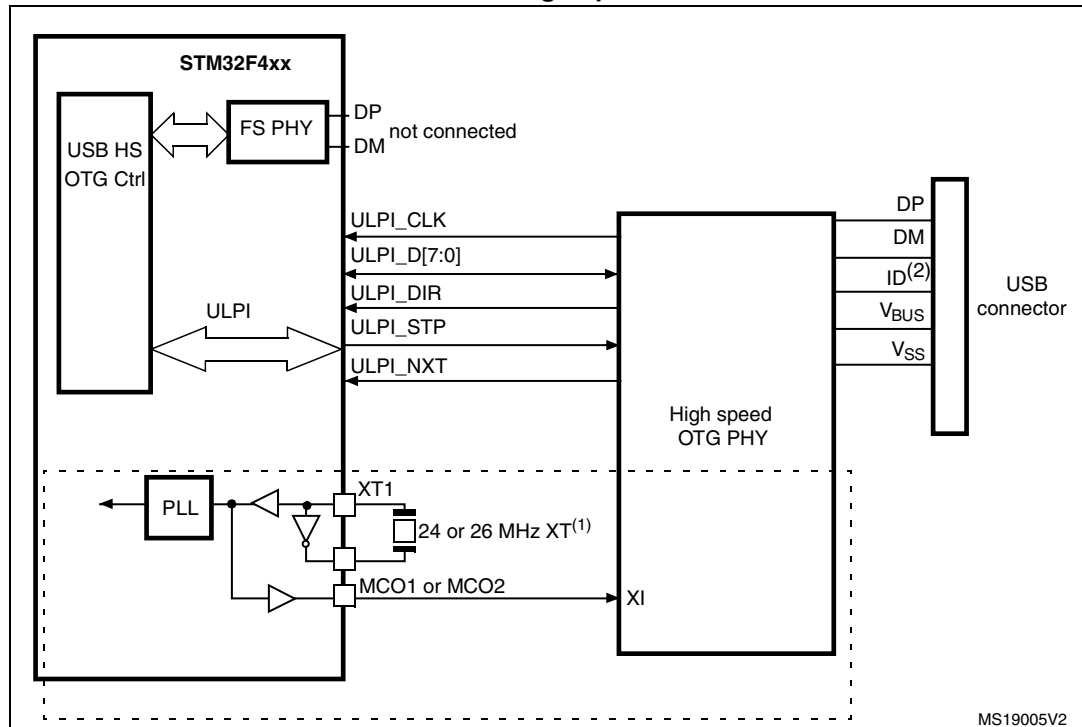
Example:	STM32	F	446	V	C	T	6	xxx
Device family								
STM32 = ARM-based 32-bit microcontroller								
Product type								
F = general-purpose								
Device subfamily								
446= STM32F446xC/E,								
Pin count								
M = 81 pins								
R = 64 pins								
V = 100 pins								
Z = 144 pins								
Flash memory size								
C=256 Kbytes of Flash memory								
E=512 Kbytes of Flash memory								
Package								
H = UFBGA (7 x 7 mm)								
J = UFBGA (10 x 10 mm)								
T = LQFP								
Y = WLCSP								
Temperature range								
6 = Industrial temperature range, –40 to 85 °C.								
7 = Industrial temperature range, –40 to 105 °C.								
Options								
xxx = programmed parts								
TR = tape and reel								

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.



A.2 USB OTG high speed (HS) interface solutions

Figure 88. USB controller configured as peripheral, host, or dual-mode and used in high speed mode



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F446xx with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.

Revision history

Table 119. Document revision history

Date	Revision	Changes
17-Feb-2015	1	Initial release.
16-Mar-2015	2	Added note 2 inside Table 2 Updated Table 11, Table 23, Table 24, Table 25, Table 26, Table 30, Table 51, Table 52, Table 53, and Table 61 Added condition inside Typical and maximum current consumption and Additional current consumption Added FMPI2C characteristics Added Table 62 and Figure 35
29-May-2015	3	Updated: – Section 6.3.15: Absolute maximum ratings (electrical sensitivity) – Section 7: Package information – Table 2: STM32F446xC/E features and peripheral counts – Table 13: STM32F446xC/xE WLCSP81 ballout – Figure 53: ESD absolute maximum ratings – Figure 54: Synchronous multiplexed NOR/PSRAM read timings Added: – Figure 78: UQFP144 7 x 7 mm marking example (package top view), – Figure 81: UQFP144 10 x 10 mm marking example (package top view), – Figure 84: WLCSP81 10 x 10 mm marking example (package top view)
10-Aug-2015	4	Updated: – Figure 14: STM32F446xC/xE UFBGA144 ballout – Table 10: STM32F446xx pin and ball descriptions – Table 18: VCAP_1/VCAP_2 operating conditions – Section 3.15: Power supply schemes – Section 6.3.2: VCAP_1/VCAP_2 external capacitor Added: – Figure 5: VDDUSB connected to an external independent power supply – Notes 3 and 4 below Figure 18: Power supply scheme