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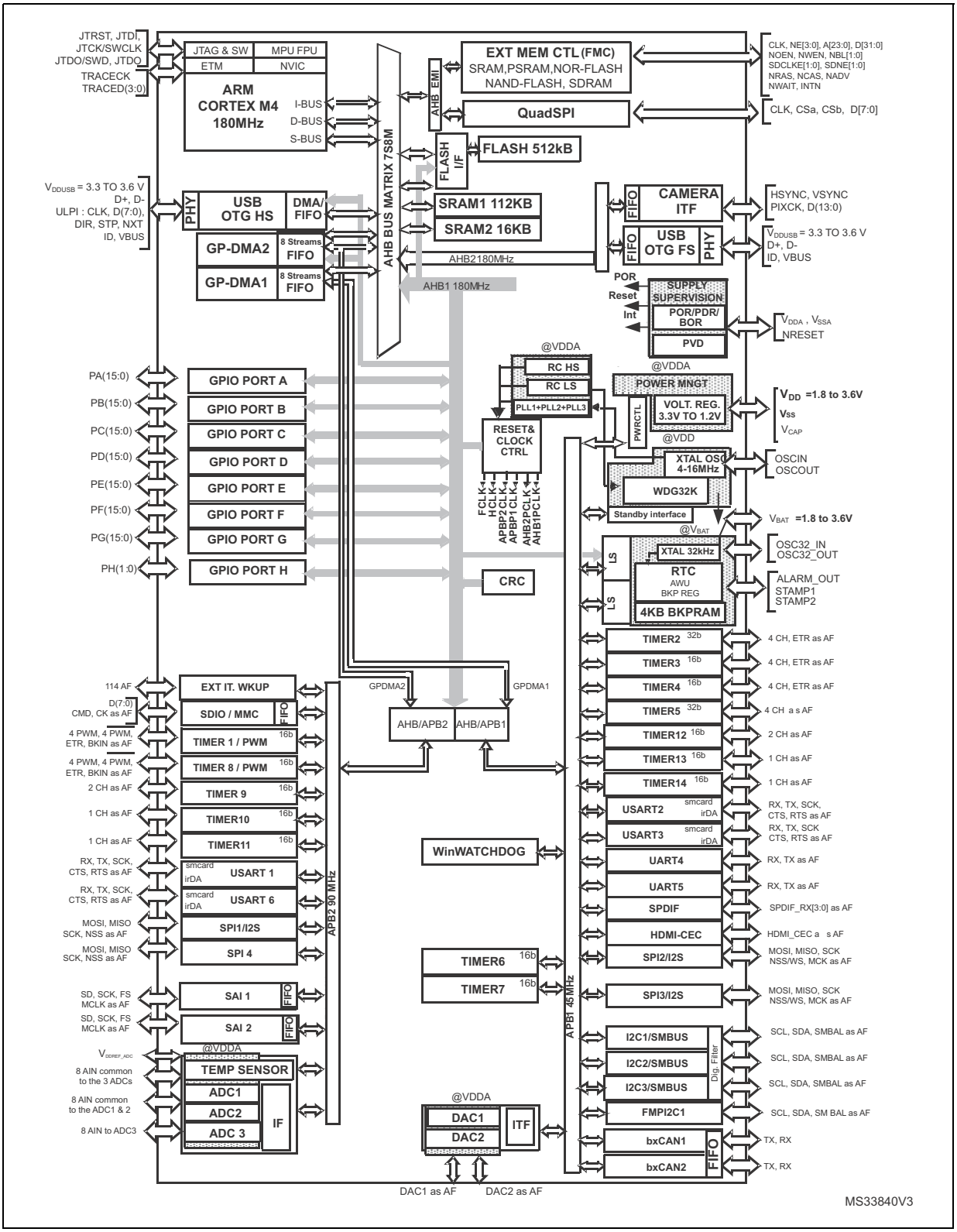
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446ret7tr

Figure 3. STM32F446xC/E block diagram



3.4 Embedded Flash memory

The devices embed a Flash memory of 512KB available for storing programs and data.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

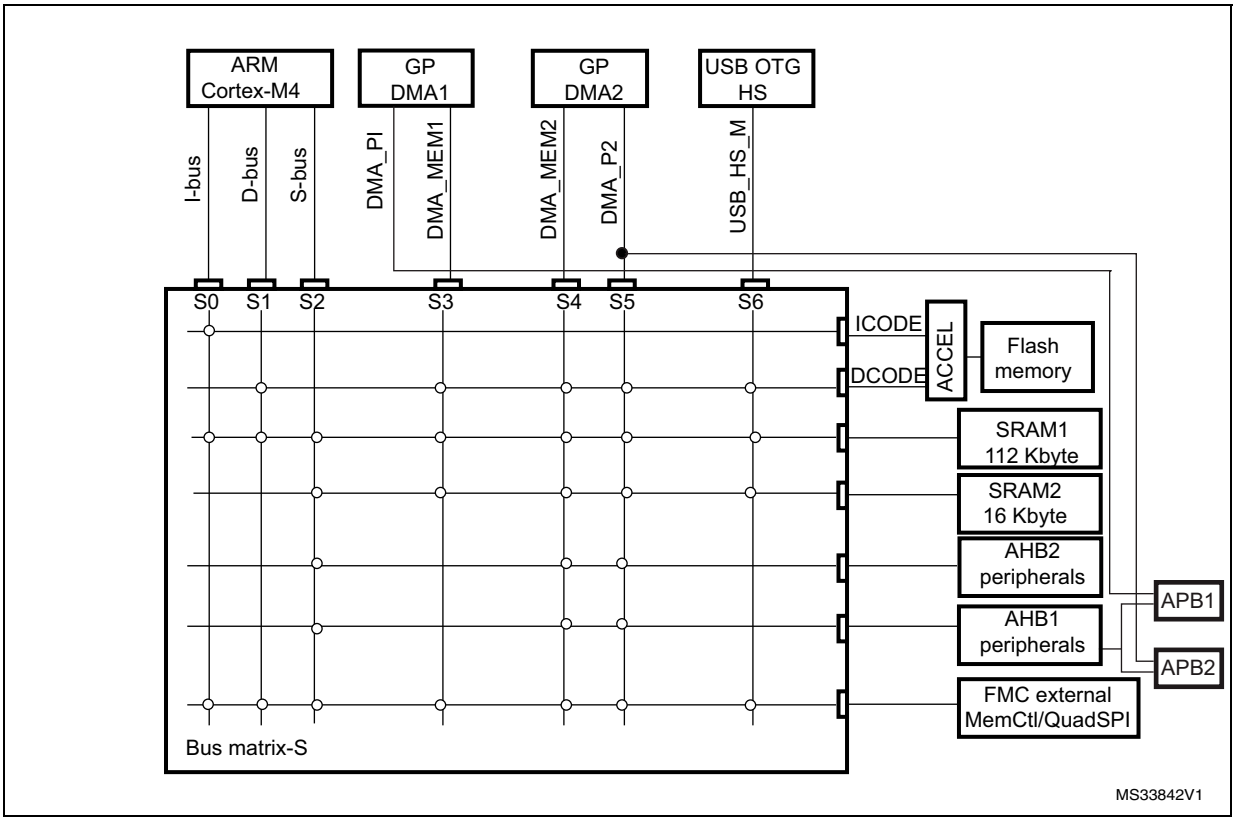
All devices embed:

- Up to 128Kbytes of system SRAM.
  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM
  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, USB HS) and the slaves Flash memory, RAM, QuadSPI, FMC, AHB and APB peripherals and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 4. STM32F446xC/E and Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

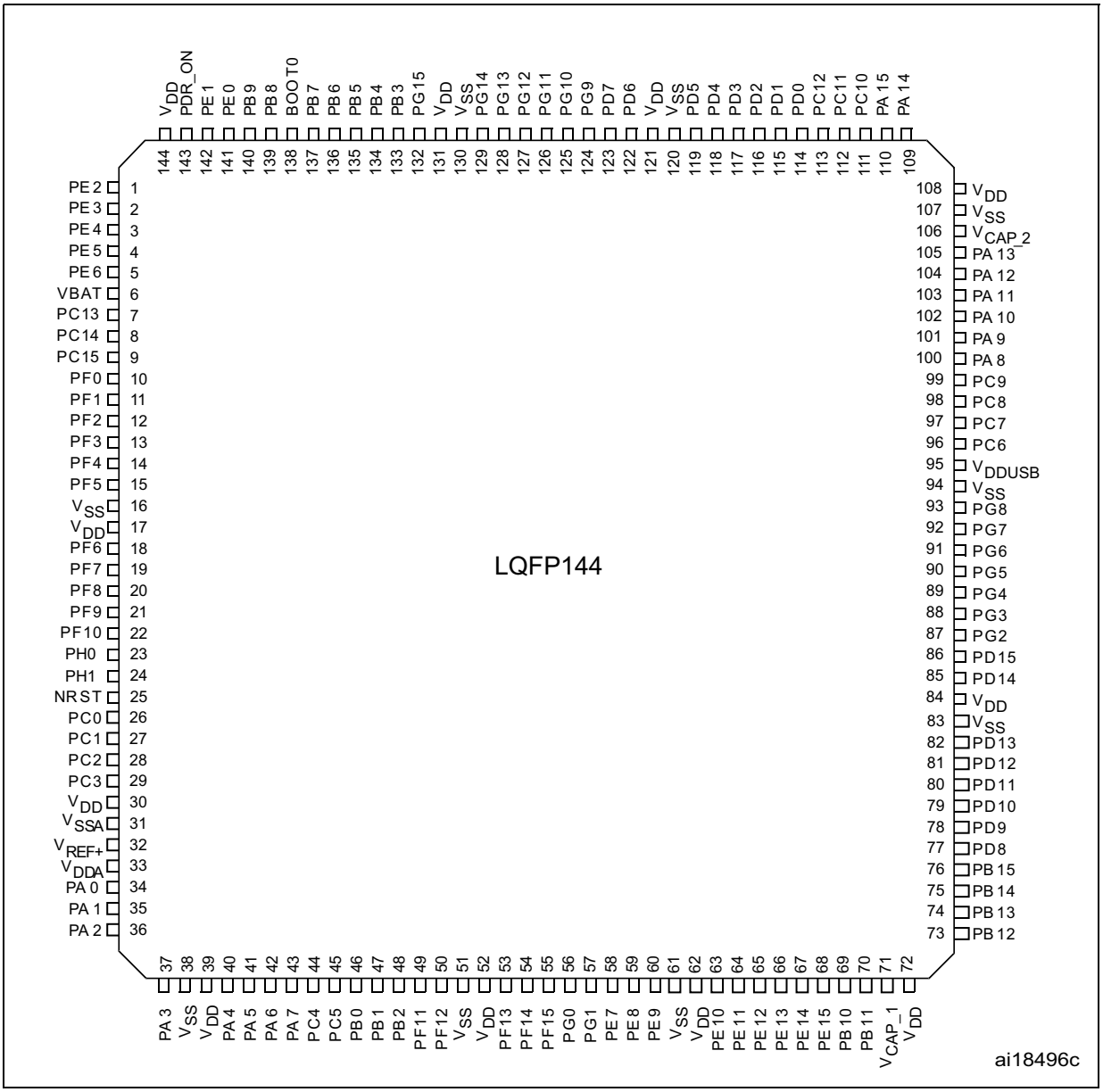
The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is not connected to V_{DD} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

Figure 12. STM32F446xC LQFP144 pinout



1. The above figure shows the package top view.

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	87	B4	A8	122	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, EVENTOUT	-
-	88	A4	A9	123	PD7	I/O	FT	-	USART2_CK, SPDIFRX_IN0, FMC_NE1, EVENTOUT	-
-	-	-	E8	124	PG9	I/O	FT	-	SPDIFRX_IN3, USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE3, DCMI_VSYNC, EVENTOUT	-
-	-	-	D8	125	PG10	I/O	FT	-	SAI2_SD_B, FMC_NE3, DCMI_D2, EVENTOUT	-
-	-	-	C8	126	PG11	I/O	FT	-	SPI4_SCK, SPDIFRX_IN0, DCMI_D3, EVENTOUT	-
-	-	-	B8	127	PG12	I/O	FT	-	SPI4_MISO, SPDIFRX_IN1, USART6_RTS, FMC_NE4, EVENTOUT	-
-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, SPI4_MOSI, USART6_CTS, FMC_A24, EVENTOUT	-
-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, SPI4_NSS, USART6_TX, QUADSPI_BK2_IO3, FMC_A25, EVENTOUT	-
-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
55	89	A5	A7	133	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, I2C2_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, EVENTOUT	-

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4	SPI2/3/4/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI/USART6/UART4/5/SPDIFRX	CAN1/2 TIM12/13/14/QUADSPI	SAI2/QUADSPI/OTG2_HS/OTG1_FS	OTG1_FS	FMC/SDIO/OTG2_FS	DCMI	-	SYS
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	-	-	SAI2_MCLK_A	-	FMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	QUADSPI_BK1_IO2	-	-	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	SAI1_SD_B	-	-	-	-	-	FMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS	SAI1_FS_A	-	-	-	-	-	FMC_A20	DCMI_D4	-	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SAI1_SCK_A	-	-	-	-	-	FMC_A21	DCMI_D6	-	EVENTOUT
	PE6	TRACED3	-	-	TIM9_CH2	-	SPI4_MOSI	SAI1_SD_A	-	-	-	-	-	FMC_A22	DCMI_D7	-	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	-	-	UART5_RX	-	QUADSPI_BK2_IO0	-	FMC_D4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	-	UART5_TX	-	QUADSPI_BK2_IO1	-	FMC_D5	-	-	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO2	-	FMC_D6	-	-	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO3	-	FMC_D7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	-	-	-	-	SAI2_SD_B	-	FMC_D8	-	-	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	-	-	-	-	SAI2_SCK_B	-	FMC_D9	-	-	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	-	-	-	-	SAI2_FS_B	-	FMC_D10	-	-	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCLK_B	-	FMC_D11	-	-	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FMC_D12	-	-	EVENTOUT

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4	SPI2/3/4/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI/USART6/UART4/5/SPDIFRX	CAN1/2 TIM12/13/14/QUADSPI	SAI2/QUADSPI/OTG2_HS/OTG1_FS	OTG1_FS	FMC/SDIO/OTG2_FS	DCMI	-	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENT OUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENT OUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENT OUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENT OUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENT OUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENT OUT
	PF6	-	-	-	TIM10_CH1	-	-	SAI1_SD_B	-	-	QUADSPI_BK1_IO3	-	-	-	-	-	EVENT OUT
	PF7	-	-	-	TIM11_CH1	-	-	SAI1_MCLK_B	-	-	QUADSPI_BK1_IO2	-	-	-	-	-	EVENT OUT
	PF8	-	-	-	-	-	-	SAI1_SCK_B	-	-	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	-	EVENT OUT
	PF9	-	-	-	-	-	-	SAI1_FS_B	-	-	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	-	EVENT OUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	-	DCMI_D11	-	EVENT OUT
	PF11	-	-	-	-	-	-	-	-	-	-	SAI2_SD_B	-	FMC_SDNRAS	DCMI_D12	-	EVENT OUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENT OUT
	PF13	-	-	-	-	FMPI2C1_SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENT OUT
	PF14	-	-	-	-	FMPI2C1_SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENT OUT
	PF15	-	-	-	-	FMPI2C1_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENT OUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 16*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 17*.

Figure 16. Pin loading conditions

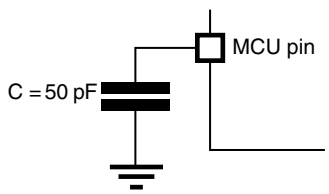


Figure 17. Pin input voltage

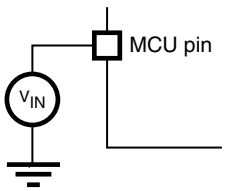


Table 23. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(2)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	External clock, PLL ON, all peripherals enabled(3)(4)	180	72	83.0(5)	100.0	110.0(5)	mA
			168	65	71.0	95.3	101.0	
			150	59	63.6	85.4	100.8	
			144(6)	54	58.4	78.8	91.2	
			120	40	44.9	62.1	73.2	
			90	30	35.3	50.7	60.0	
			60	21	25.5	39.2	46.8	
			30	12	16.2	28.1	36.0	
			25	10	14.41	26.17	32.4	
		HSI, PLL OFF, all peripherals enabled	16	6	11.4	23.1	25.2	
			8	3	9.5	20.3	22.5	
			4	2.3	8.3	18.9	21.1	
			2	1.8	7.7	18.1	20.5	
		External clock, PLL ON, all Peripherals disabled(3)	180	32	42.0(5)	59.0	75.0(5)	
			168	29	35.5	51.4	55.7	
			150	26	31.5	47.8	51.9	
			144(6)	24	29.2	44.7	48.6	
			120	18	23.3	36.8	40.4	
			90	14	19.0	31.8	35.1	
			60	10	14.7	26.9	29.9	
			30	6	10.7	22.1	24.9	
			25	5	9.96	21.24	24.02	
		HSI, PLL OFF, all peripherals disabled(3)	16	3	8.7	18.9	21.9	
			8	2	8.1	17.8	20.9	
			4	1.7	7.64	17.23	20.32	
			2	1.4	7.4	16.94	20.03	

1. Code and data processing running from SRAM1 using boot pins.
2. Guaranteed based on test during characterization.
3. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
4. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
5. Tested in production.
6. Overdrive OFF

Table 33. Typical current consumption in Sleep mode, regulator OFF(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	VDD=3.3 V		VDD=1.7 V		Unit
				I_{DD12}	I_{DD}	I_{DD12}	I_{DD}	-
I_{DD12}/I_{DD}	Supply current in Sleep mode from V_{12} and V_{DD} supply	All Peripherals enabled	180	47.605	1.2	NA	NA	mA
			168	44.35	1.0	41.53	0.8	
			150	40.58	0.9	39.96	0.8	
			144	35.68	0.9	34.60	0.7	
			120	27.30	0.9	29.11	0.7	
			90	20.69	0.8	19.78	0.6	
			60	13.88	0.7	13.36	0.6	
			30	7.66	0.7	7.85	0.6	
			25	6.49	0.7	6.66	0.5	
		All Peripherals disabled	180	8.71	1.2	NA	NA	
			168	7.00	0.9	8.42	0.8	
			150	6.88	0.9	7.61	0.8	
			144	6.29	0.9	6.99	0.7	
			120	4.87	0.9	5.95	0.7	
			90	3.78	0.8	3.96	0.6	
			60	2.66	0.7	2.80	0.6	
			30	1.65	0.7	1.74	0.6	
			25	1.45	0.7	1.52	0.5	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

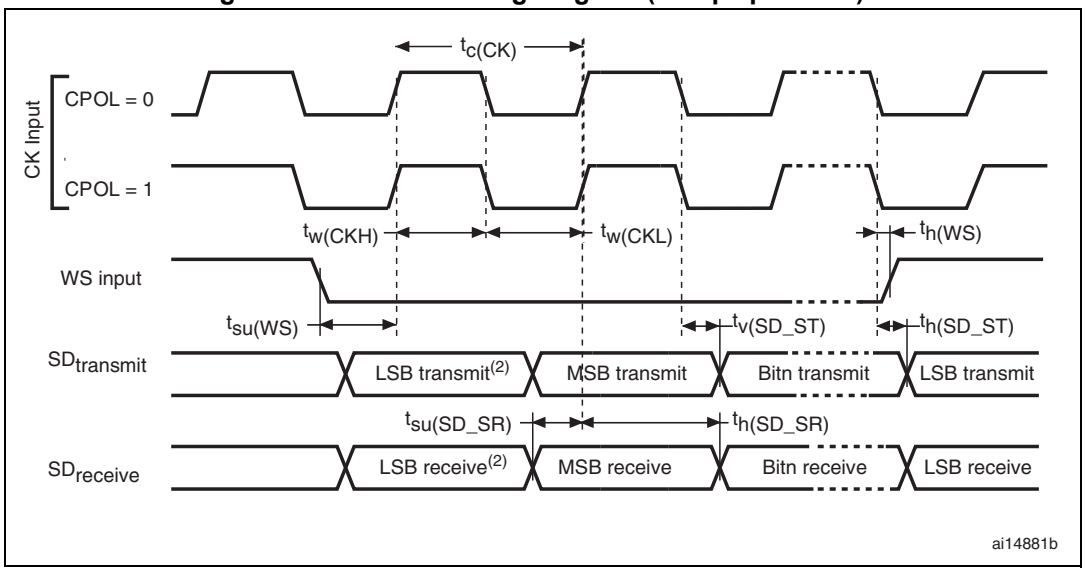
I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 56: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

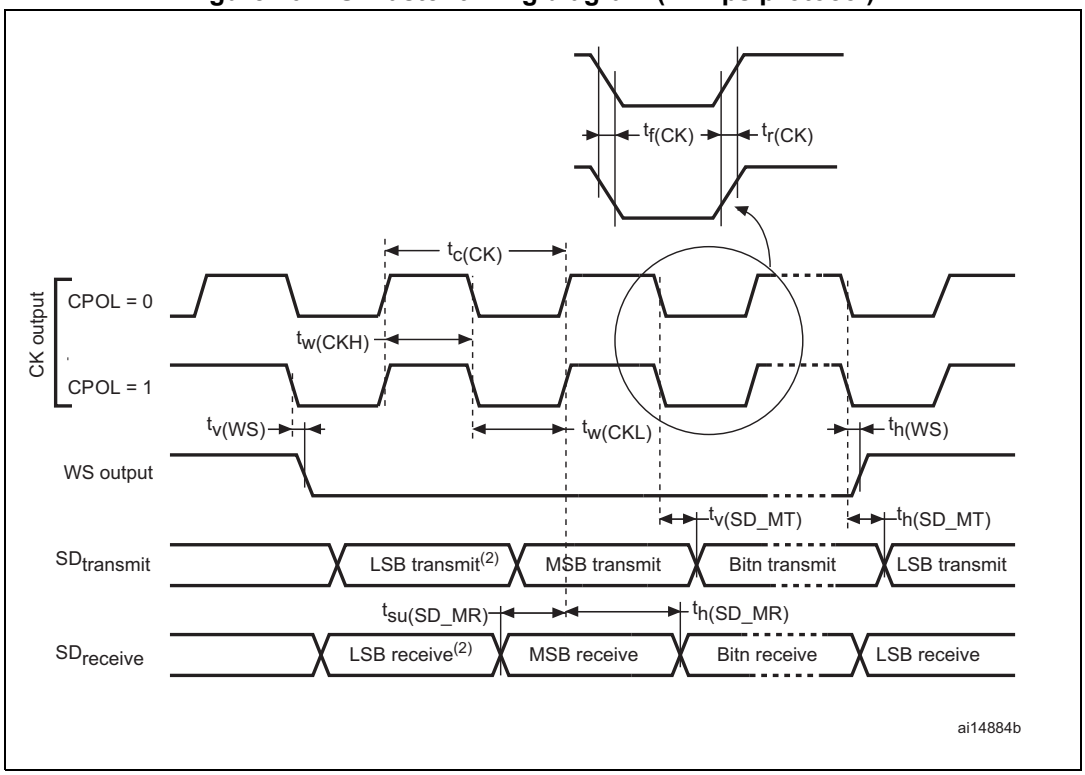
Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Figure 39. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 40. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 41. SAI master timing waveforms

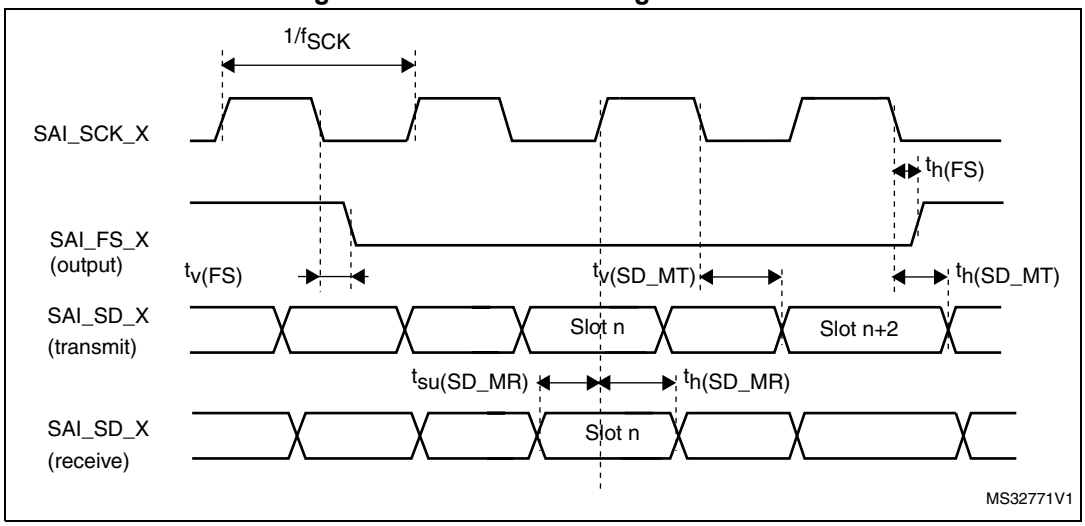
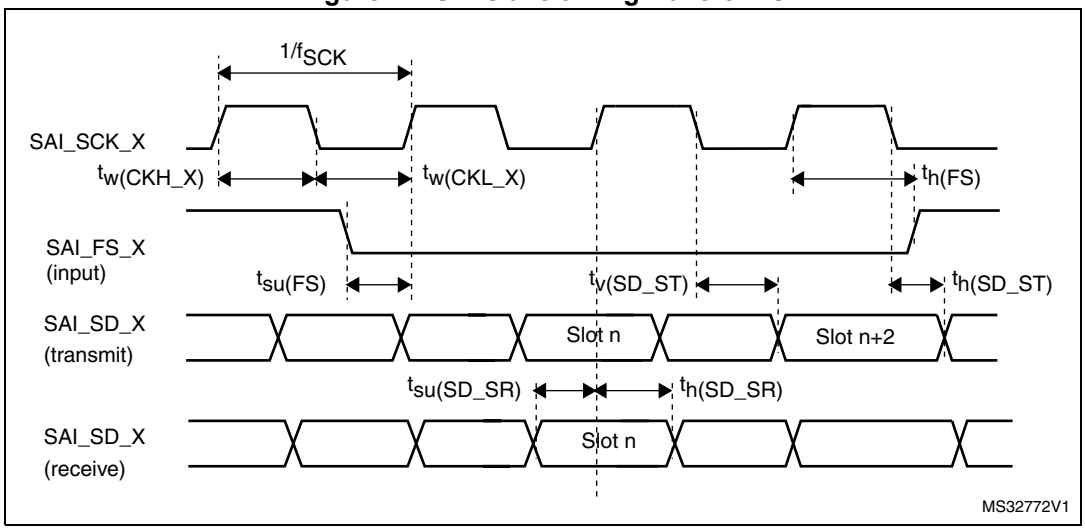


Figure 42. SAI slave timing waveforms



USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 68. USB OTG full speed startup time

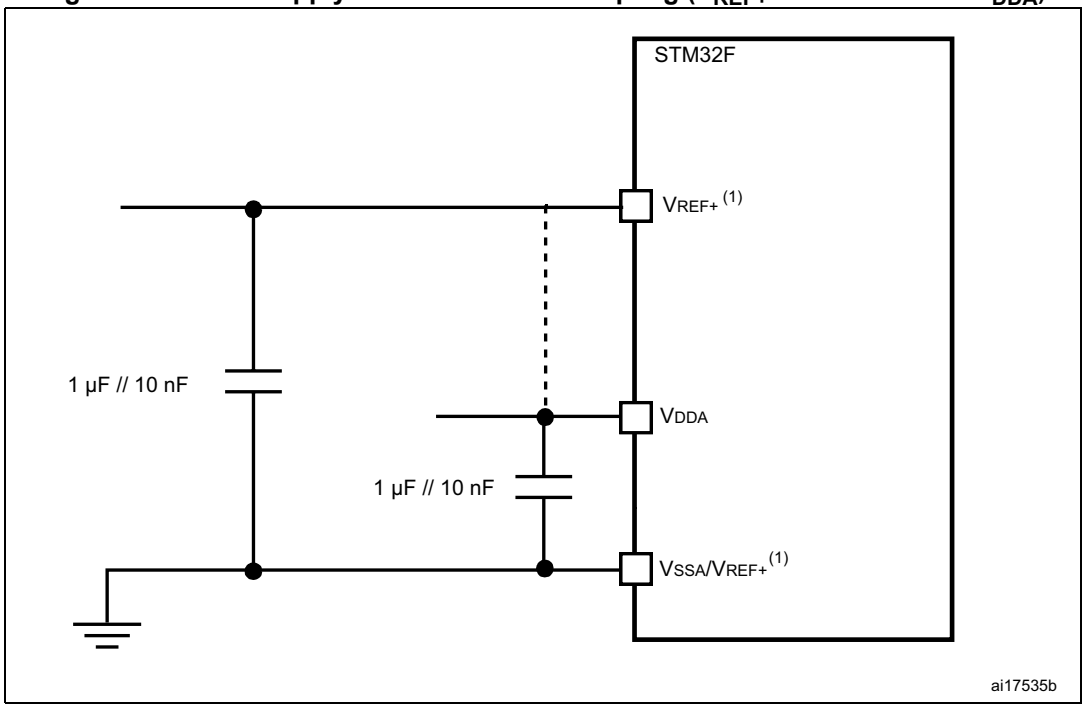
Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG full speed transceiver startup time	1	µs

1. Guaranteed by design.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 47* or *Figure 48*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 47. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA144. V_{REF+} is also available on LQFP100, LQFP144, and WLCSP81. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 94. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK} - 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK} – 0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	0.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. C_L = 30 pF.
2. Guaranteed based on test during characterization.

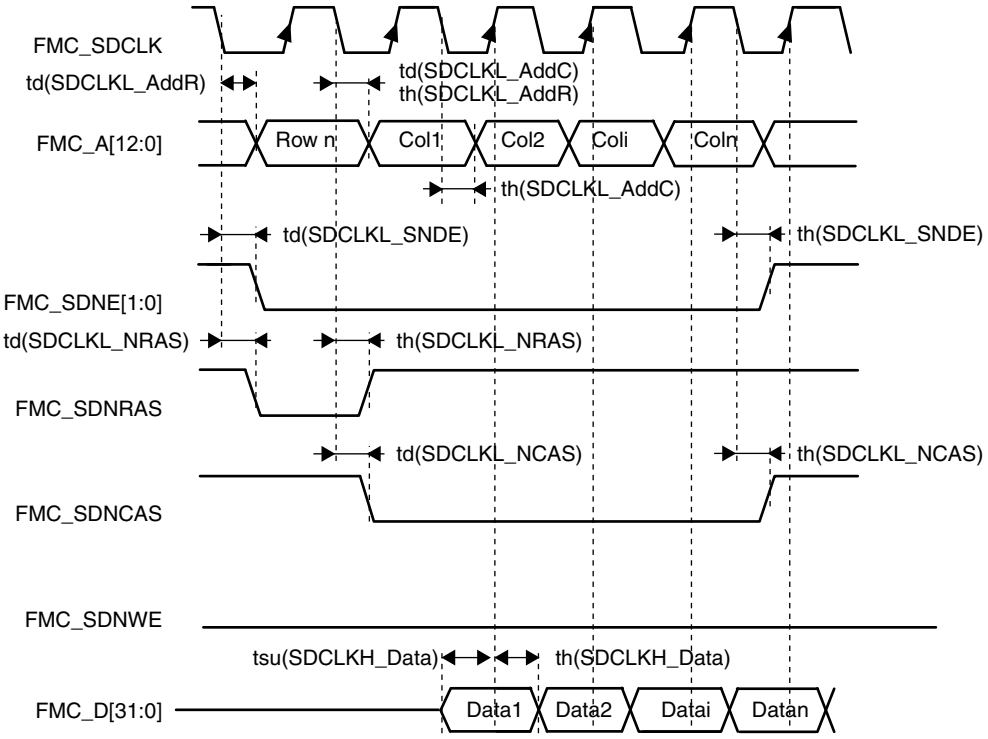
Table 99. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{HCLK}$ - 2	$4T_{HCLK}$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	ns
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$3T_{HCLK}$ – 1	-	ns
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$ – 3	-	ns
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{HCLK}$ - 0.5	ns
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK}$ – 2	-	ns

1. C_L = 30 pF.

SDRAM waveforms and timings

Figure 62. SDRAM read access waveforms (CL = 1)

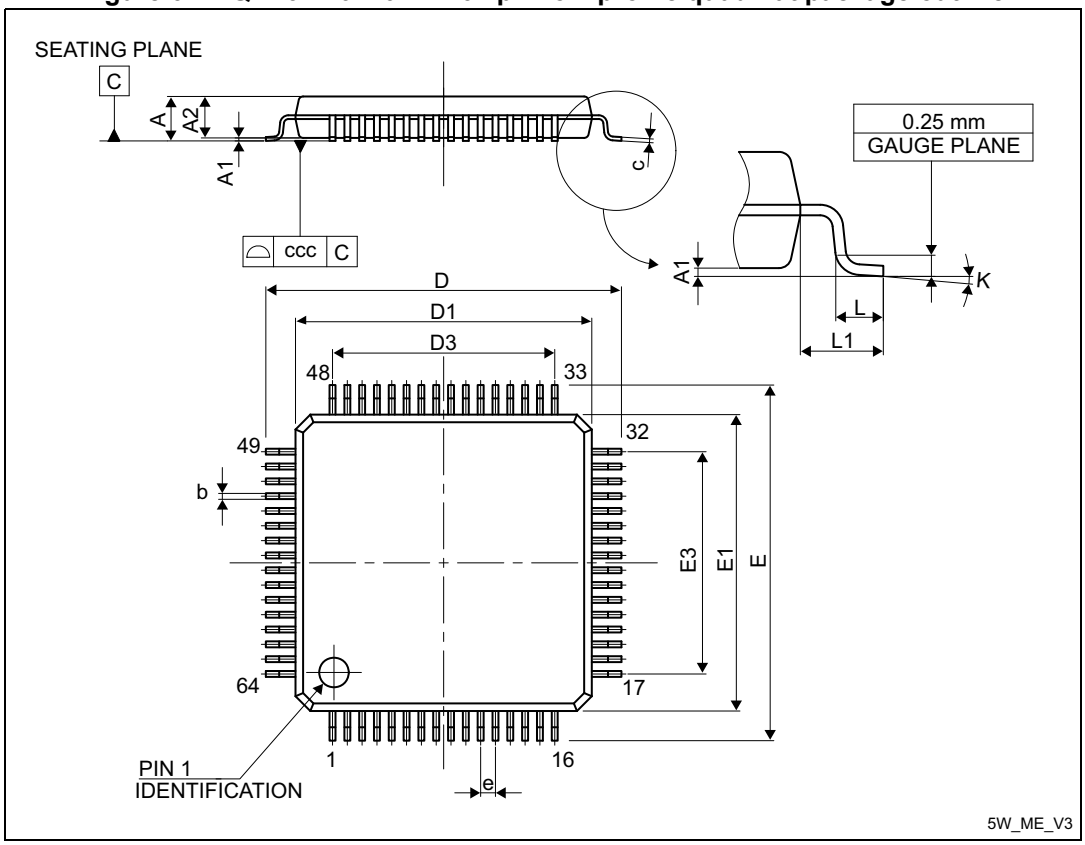


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 67. LQFP64-10x10 mm 64 pin low-profile quad flat package outline



1. Drawing is not to scale

Table 108. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data

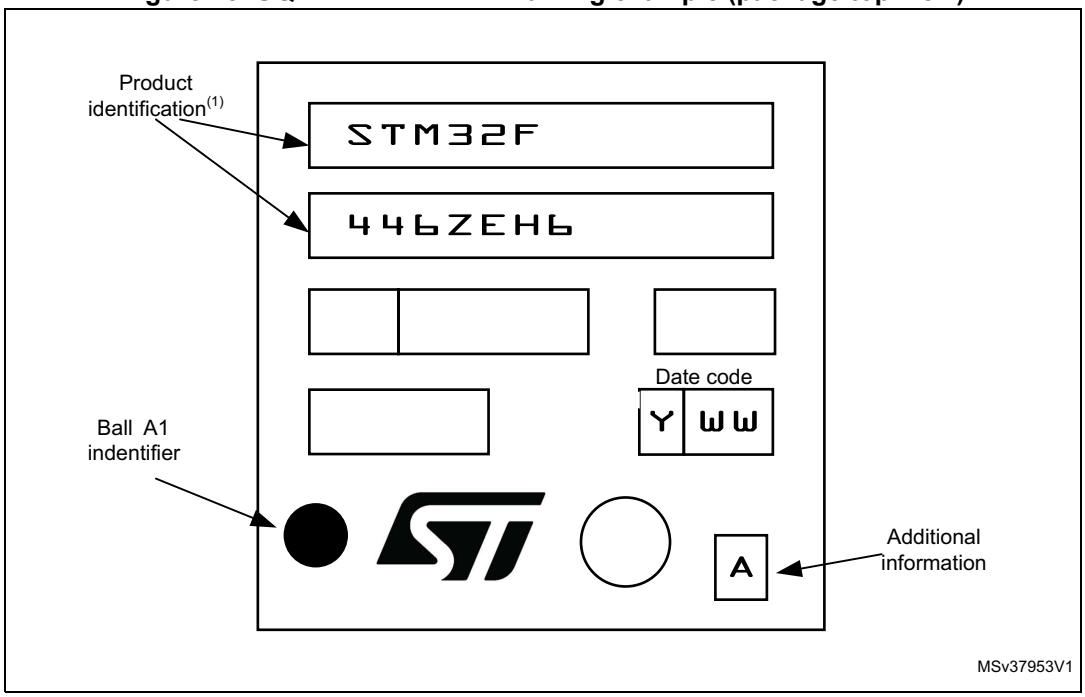
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079

Device marking for UFBGA144 7 x 7 mm package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 78. UQFP144 7 x 7 mm marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

8 Part numbering

Table 118. Ordering information scheme

Example: STM32 F 446 V C T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

446= STM32F446xC/E,

Pin count

M = 81 pins

R = 64 pins

V = 100 pins

Z = 144 pins

Flash memory size

C=256 Kbytes of Flash memory

E=512 Kbytes of Flash memory

Package

H = UFBGA (7 x 7 mm)

J = UFBGA (10 x 10 mm)

T = LQFP

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts

TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.