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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446vct7

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2 Description

The STM32F446xC/E devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F446xC/E devices incorporate high-speed embedded memories (Flash memory up to 512 Kbyte, up to 128 Kbyte of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers.

They also feature standard and advanced communication interfaces.

- Up to four I^2Cs;
- Four SPIs, three I^2Ss full simplex. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization;
- Four USARTs plus two UARTs;
- An USB OTG full-speed and an USB OTG high-speed with full-speed capability (with the ULPI), both with dedicated power rails allowing to use them throughout the entire power range;
- Two CANs;
- Two SAIs serial audio interfaces. To achieve audio class accuracy, the SAIs can be clocked via a dedicated internal audio PLL;
- An SDIO/MMC interface;
- Camera interface;
- HDMI-CEC;
- SPDIF Receiver (SPDIFRx);
- QuadSPI.

Advanced peripherals include an SDIO, a flexible memory control (FMC) interface, a camera interface for CMOS sensors. Refer to *Table 2: STM32F446xC/E features and peripheral counts* for the list of peripherals available on each part number.

The STM32F446xC/E devices operates in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 3.16.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F446xC/E devices offer devices in 6 packages ranging from 64 pins to 144 pins. The set of included peripherals changes with the device chosen.

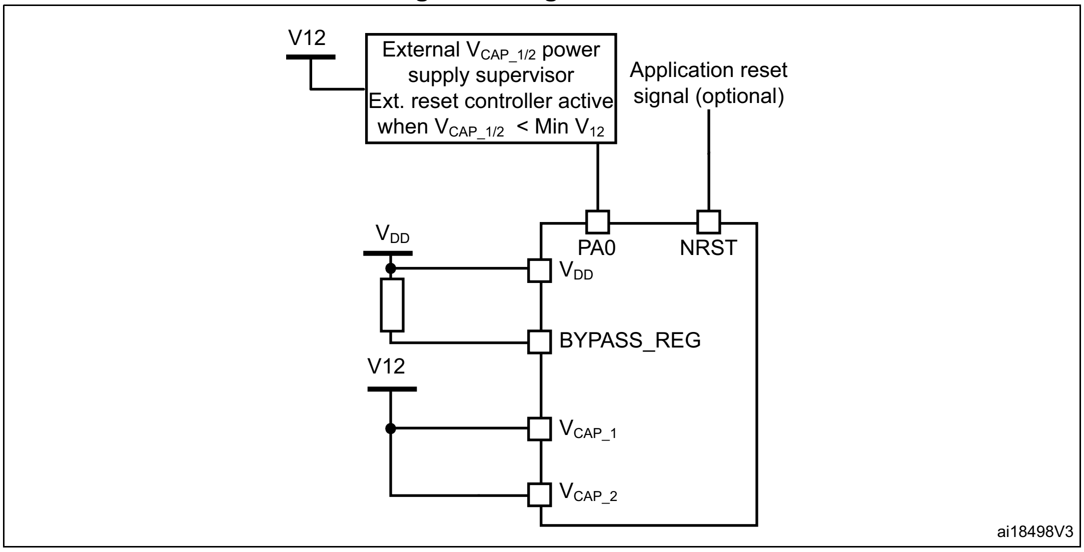
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.

Figure 7. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 8*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 9*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

3.23 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. USART feature comparison(1)

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	X	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	X	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)

1. X = feature supported.

3.24 Serial peripheral interface (SPI)

The devices feature up to four SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, and SPI4 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

3.32 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

3.33 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The USB has dedicated power rails allowing its use throughout the entire power range. The major features are:

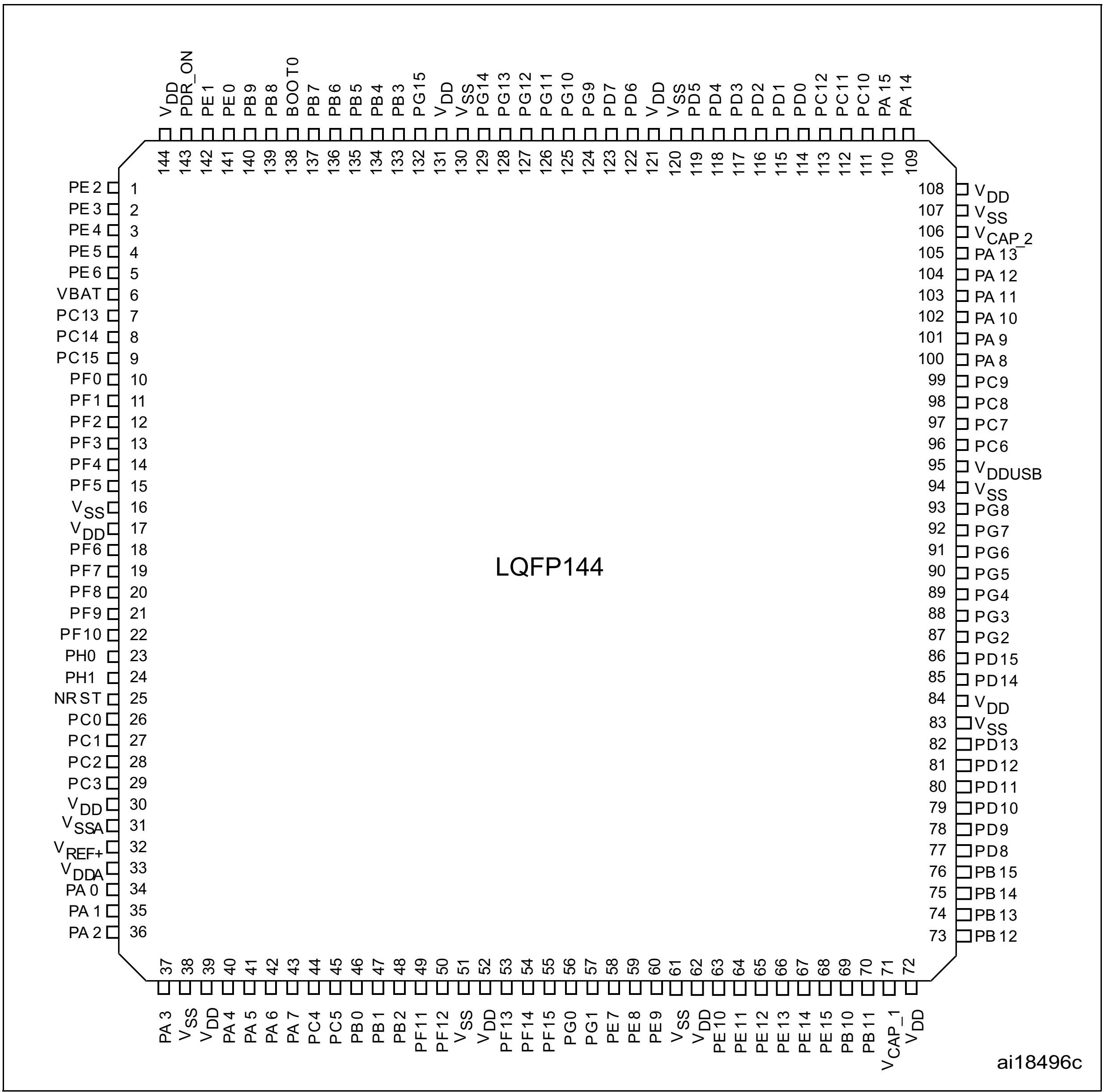
- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.34 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The USB has dedicated power rails allowing its use throughout the entire power range.

Figure 12. STM32F446xC LQFP144 pinout

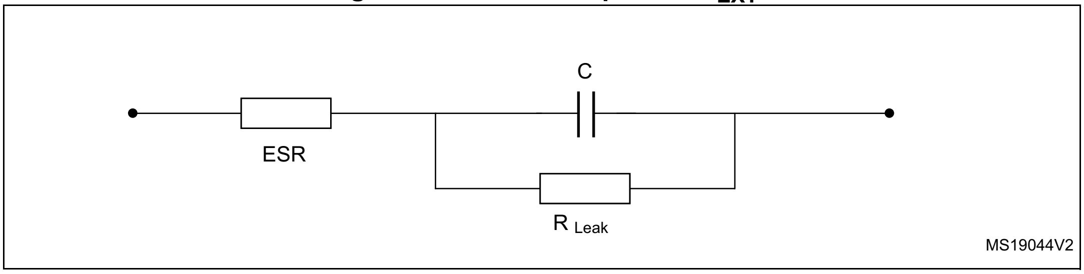


1. The above figure shows the package top view.

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
51	78	D3	B11	111	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDIO_D2, DCMI_D8, EVENTOUT	-
52	79	D4	B10	112	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDIO_D3, DCMI_D4, EVENTOUT	-
53	80	A2	C10	113	PC12	I/O	FT	-	I2C2_SDA, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDIO_CK, DCMI_D9, EVENTOUT	-
-	81	B3	E10	114	PD0	I/O	FT	-	SPI4_MISO, SPI3_MOSI/I2S3_SD, CAN1_RX, FMC_D2, EVENTOUT	-
-	82	C4	D10	115	PD1	I/O	FT	-	SPI2_NSS/I2S2_WS, CAN1_TX, FMC_D3, EVENTOUT	-
54	83	D5	E9	116	PD2	I/O	FT	-	TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
-	84	-	D9	117	PD3	I/O	FT	-	TRACED1, SPI2_SCK/I2S2_CK, USART2_CTS, QUADSPI_CLK, FMC_CLK, DCMI_D5, EVENTOUT	-
-	85	A3	C9	118	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
-	86	-	B9	119	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	-	-	E7	120	VSS	S	-	-	-	-
-	-	-	F7	121	VDD	S	-	-	-	-

Figure 20. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 18. VCAP_1/VCAP_2 operating conditions(1)

Symbol	Parameter	Conditions
C_{EXT}	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω
C_{EXT}	Capacitance of external capacitor with a single V_{CAP} pin available	4.7 µF
ESR	ESR of external capacitor with a single V_{CAP} pin available	< 1 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 19. Operating conditions at power-up/power-down (regulator ON)

Symbol	Parameter	Min	Max
t_{VDD}	V_{DD} rise time rate	20	∞
	V_{DD} fall time rate	20	∞

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 20. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Table 46. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15}-1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(peak)$$

Table 48. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	8	16	s
		Program/erase parallelism (PSIZE) = x 16	-	5.5	11	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed based on test during characterization.
2. The maximum programming time is measured after 100K erase operations.

Table 49. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	ms
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	ms
t_{ME}	Mass erase time		-	3.5	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V

6.3.17 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 56: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 16*. All I/Os are CMOS and TTL compliant.

Table 56. I/O static characteristics

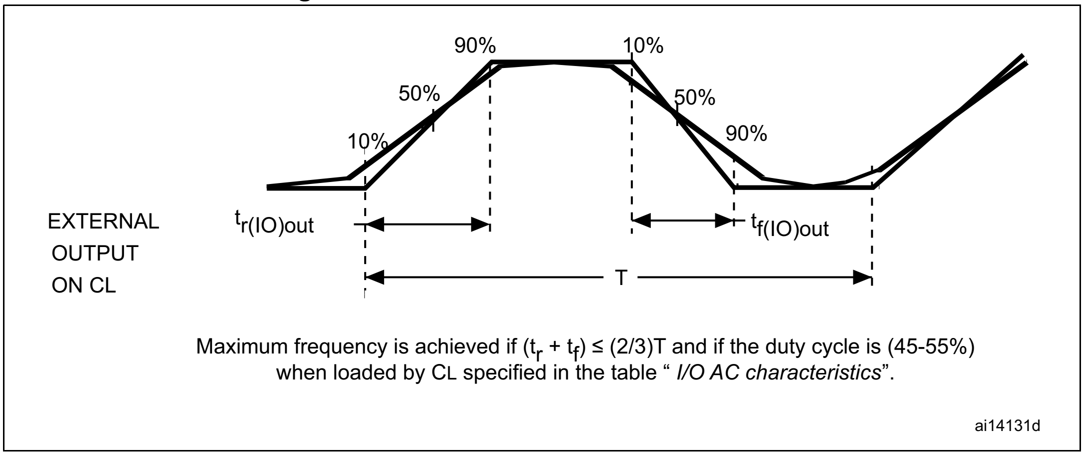
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, FTf, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}-0.04$(1)	V
					$0.3V_{DD}$(2)	
	BOOT0 I/O input low level voltage	1.75 V ≤ V_{DD} ≤ 3.6 V, – 40 °C≤ T_A ≤ 105 °C	-	-	$0.1V_{DD}+0.1$(1)	
		1.7 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤105 °C	-	-		
V_{IH}	FT, FTf, TTa and NRST I/O input high level voltage(4)	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3$(1)	-	-	V
			$0.7V_{DD}$(2)			
	BOOT0 I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, – 40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7$(1)	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
V_{HYS}	FT, FTf, TTa and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	-	10%V_{DD}	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	-	100m	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	-		-	
I_{lkg}	I/O input leakage current (3)	V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (4)	V_{IN} = 5 V	-	-	3	

Table 58. I/O AC characteristics(1)(2) (continued)

OSPEEDRy[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD}≥ 2.7 V	-	-	25	MHz
			C_L = 50 pF, V_{DD}≥ 1.8 V	-	-	12.5	
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	50	
			C_L = 10 pF, V_{DD}≥ 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	12.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	10	ns
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	6	
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	20	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} ≥ 2.7 V	-	-	50(4)	MHz
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	25	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} ≥2.7 V	-	-	6	ns
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	4	
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	6	
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
			C_L = 10 pF, V_{DD}≥ 2.7 V	-	-	180(4)	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	100	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	72.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥1.8 V	-	-	6	
			C_L = 30 pF, V_{DD} ≥1.7 V	-	-	7	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	2.5	
			C_L = 10 pF, V_{DD} ≥1.8 V	-	-	3.5	
			C_L = 10 pF, V_{DD} ≥1.7 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 32*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 32. I/O AC characteristics definition



6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 56: I/O static characteristics*).

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 59. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FMC_CLK = 90 MHz).

Figure 54. Synchronous multiplexed NOR/PSRAM read timings

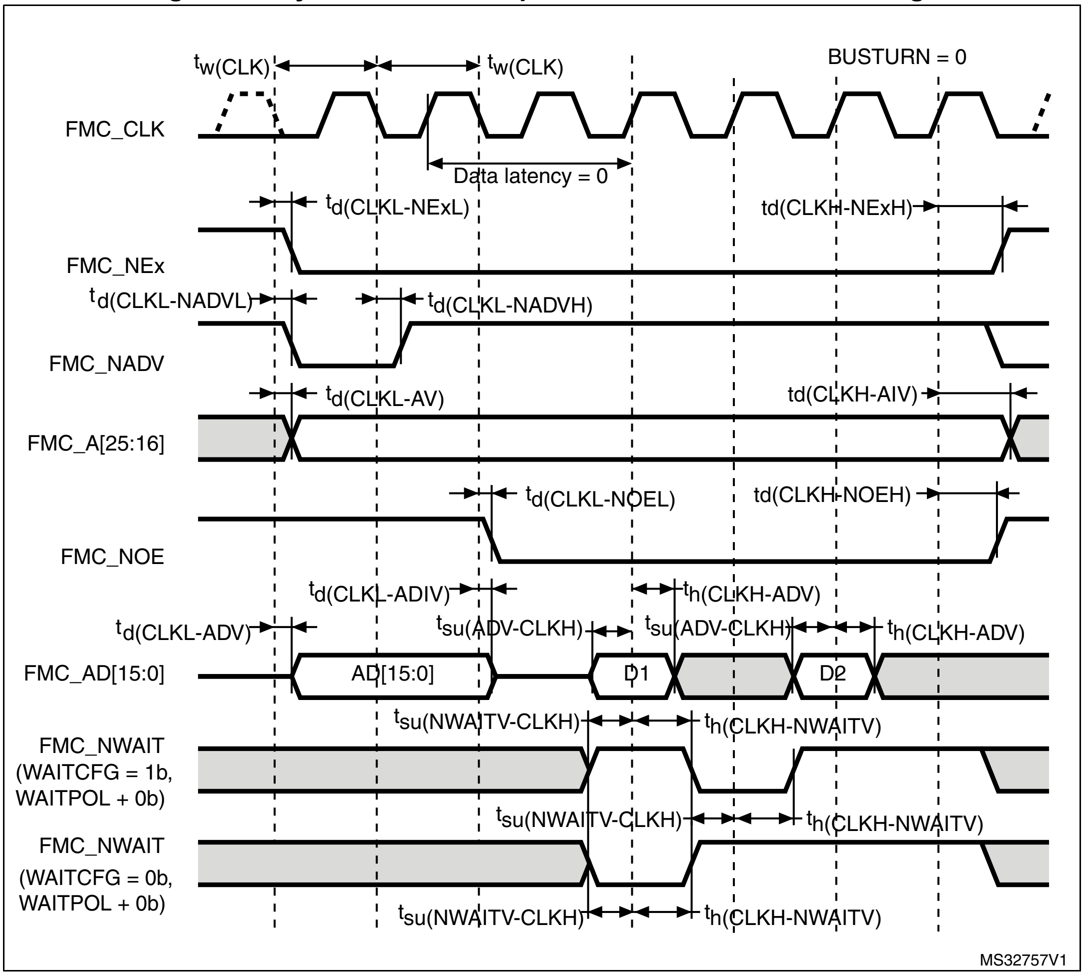


Figure 55. Synchronous multiplexed PSRAM write timings

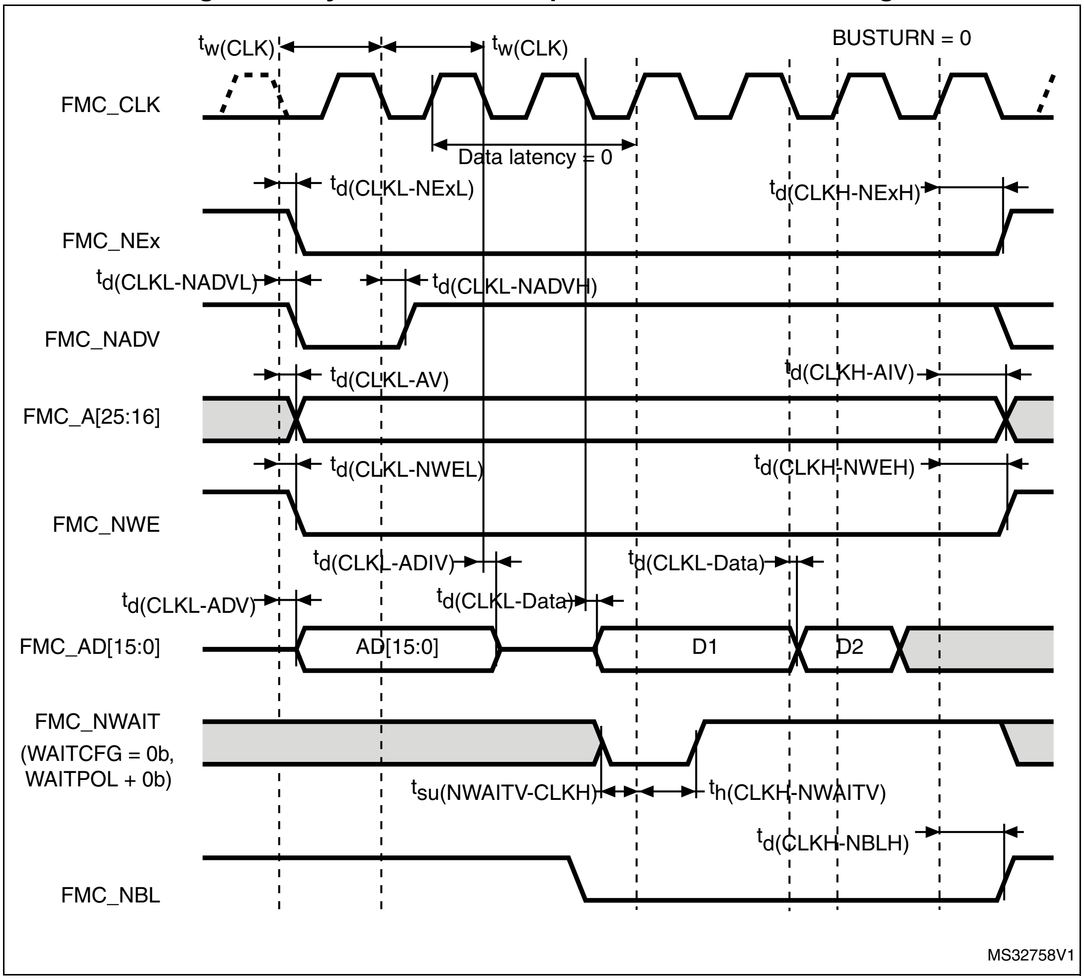


Figure 60. NAND controller waveforms for common memory read access

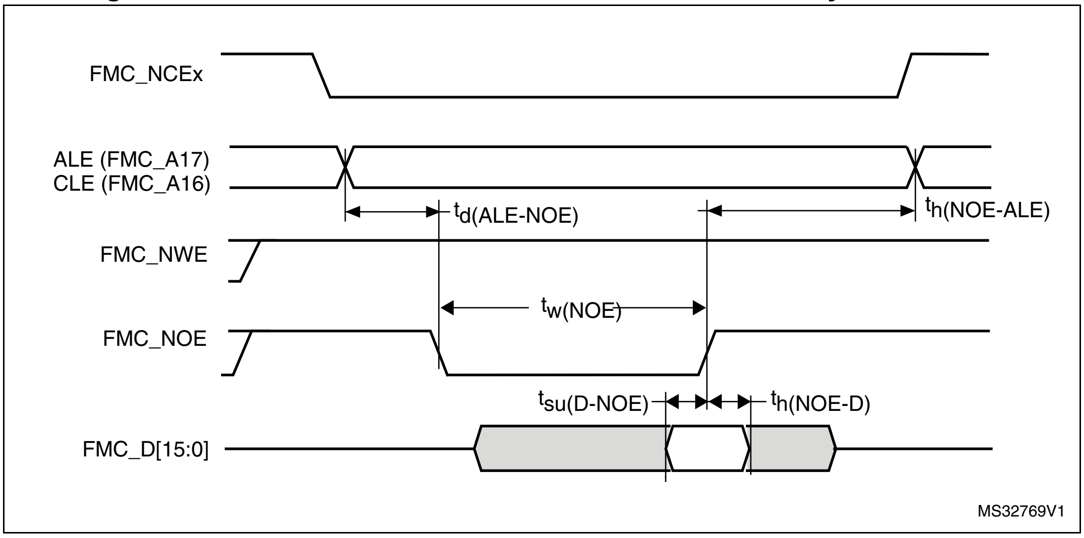


Figure 61. NAND controller waveforms for common memory write access

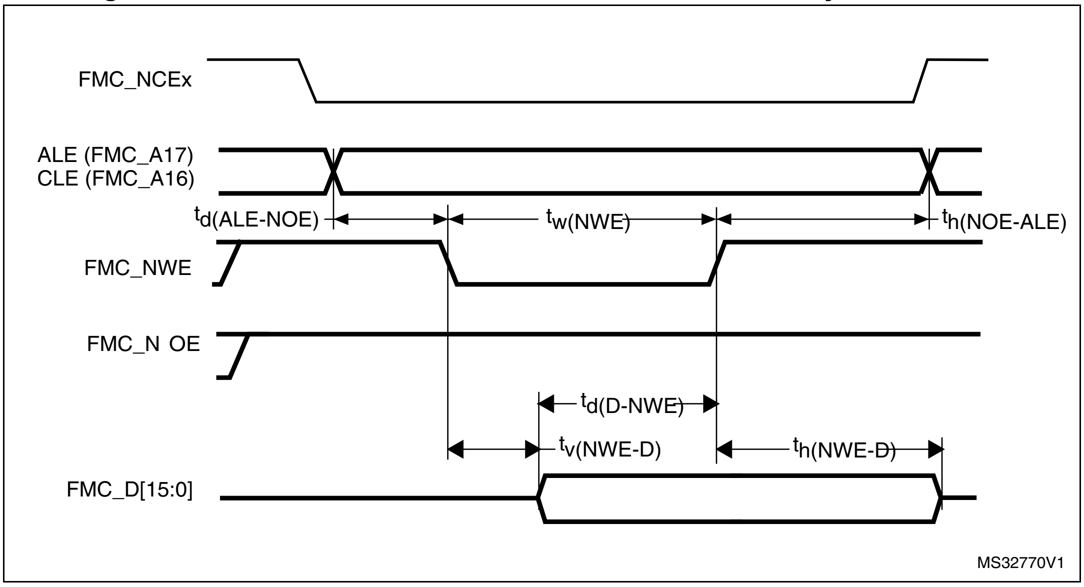


Table 98. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK} - 0.5$	$4T_{HCLK} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	9	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	2.5	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{HCLK}$ - 0.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK} - 2$	-	

1. C_L = 30 pF.

Figure 63. SDRAM write access waveforms

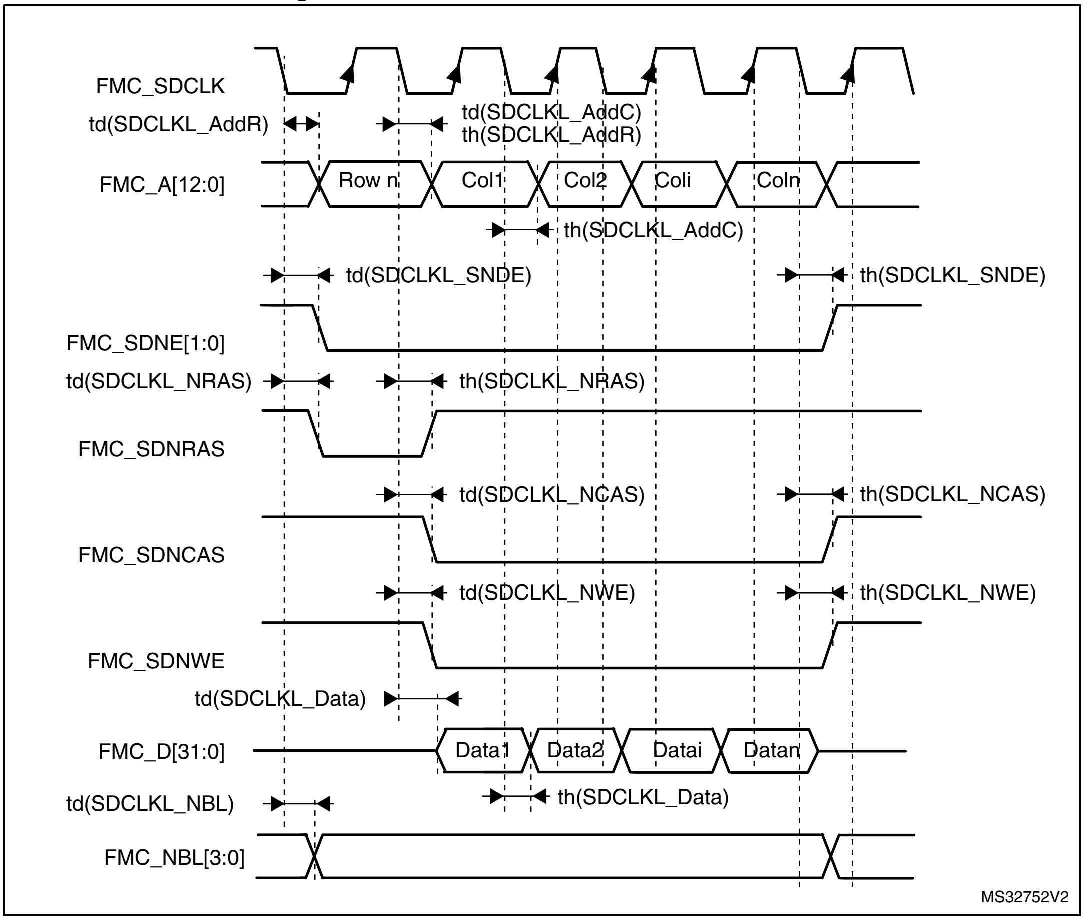


Table 102. SDRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$F_{(SDCLK)}$	Frequency of operation	-	90	MHz
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}$ - 0.5	$2T_{HCLK}$ + 0.5	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	2	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0.5	-	
$t_{d(SDCLK\_Add)}$	Address valid time	-	3	
$t_{d(SDCLKL\_SDNWE))}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL\_SDNWE))}$	SDNWE hold time	0	-	
$t_{d(SDCLKL\_SDNE))}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valie time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

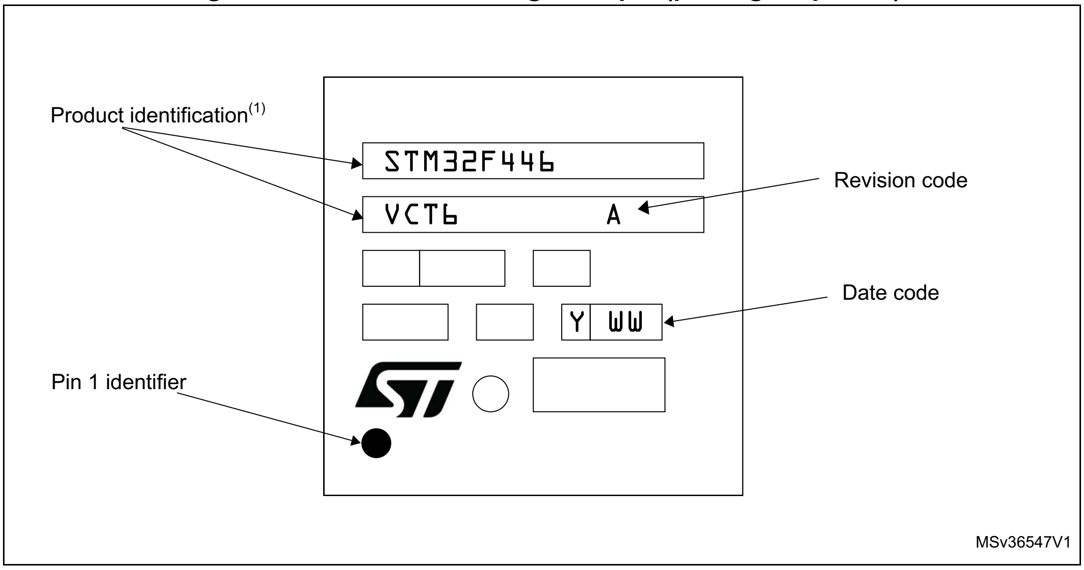
1. C_L = 10 pF on data and address line. C_L=15 pF on FMC_SDCLK.
2. Guaranteed based on test during characterization.

Device marking for LQFP100 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 72. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 113. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.550	0.600	0.650	0.0177	0.0197	0.0217
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 80. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package recommended footprint

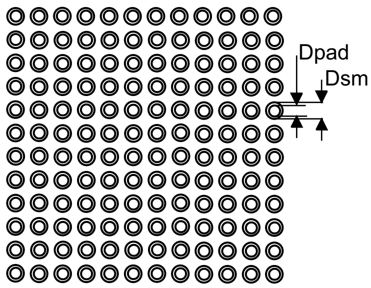
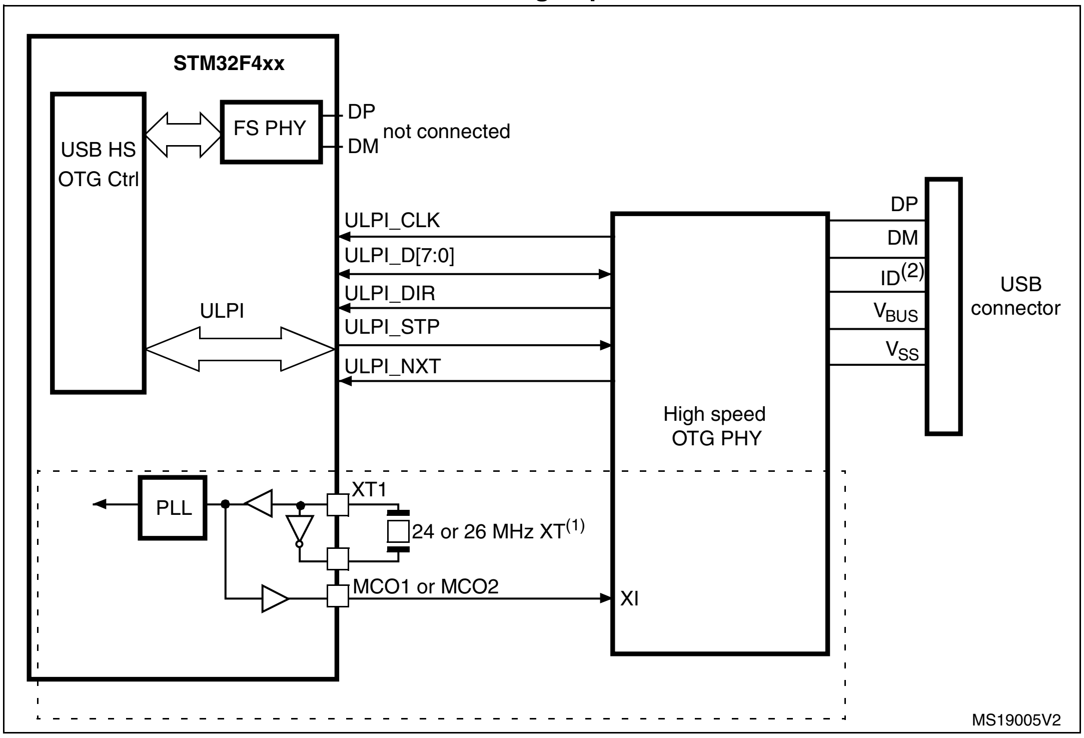


Table 114. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)

Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

A.2 USB OTG high speed (HS) interface solutions

Figure 88. USB controller configured as peripheral, host, or dual-mode and used in high speed mode



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F446xx with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.