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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 180MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 81 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446vet6 |

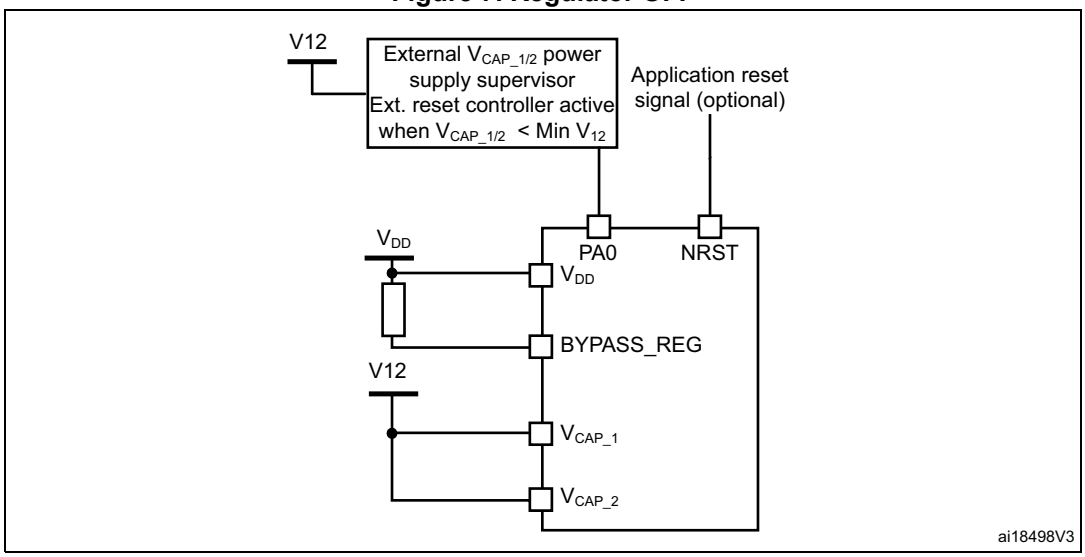
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on $V_{12}$. An external power supply supervisor should be used to monitor the $V_{12}$ of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on $V_{12}$ power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the $V_{12}$ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.

**Figure 7. Regulator OFF**




The following conditions must be respected:

- $V_{DD}$ should always be higher than $V_{CAP\_1}$ and $V_{CAP\_2}$ to avoid current injection between power domains.
- If the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach $V_{12}$ minimum value is faster than the time for $V_{DD}$ to reach 1.7 V, then PA0 should be kept low to cover both conditions: until $V_{CAP\_1}$ and $V_{CAP\_2}$ reach $V_{12}$ minimum value and until $V_{DD}$ reaches 1.7 V (see *Figure 8*).
- Otherwise, if the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach $V_{12}$ minimum value is slower than the time for $V_{DD}$ to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 9*).
- If $V_{CAP\_1}$ and $V_{CAP\_2}$ go below $V_{12}$ minimum value and $V_{DD}$ is higher than 1.7 V, then a reset must be asserted on PA0 pin.

*Note: The minimum value of $V_{12}$ depends on the maximum frequency targeted in the application.*

**Table 4. Regulator ON/OFF and internal reset ON/OFF availability**

| Package | Regulator ON | Regulator OFF | Internal reset ON | Internal reset OFF |
|---|---|---|---|---|
| LQFP144 | Yes | No | Yes<br>PDR_ON<br>set to $V_{DD}$ | Yes<br>PDR_ON<br>set to VSS |
| UFBGA144 | Yes<br>BYPASS_REG<br>set to Vss | Yes<br>BYPASS_REG<br>set to VDD | | |
| WLCSP81 | | | | |

## 3.18 Real-time clock (RTC), backup SRAM and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The 4-Kbyte backup SRAM is an EEPROM-like memory area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled by default to minimize power consumption (see *Section 3.19: Low-power modes*). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when $V_{DD}$ power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.19: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the $V_{DD}$ supply when present or from the $V_{BAT}$ pin.

# 5 Memory mapping

The memory map is shown in *Figure 15*

**Figure 15. Memory map**

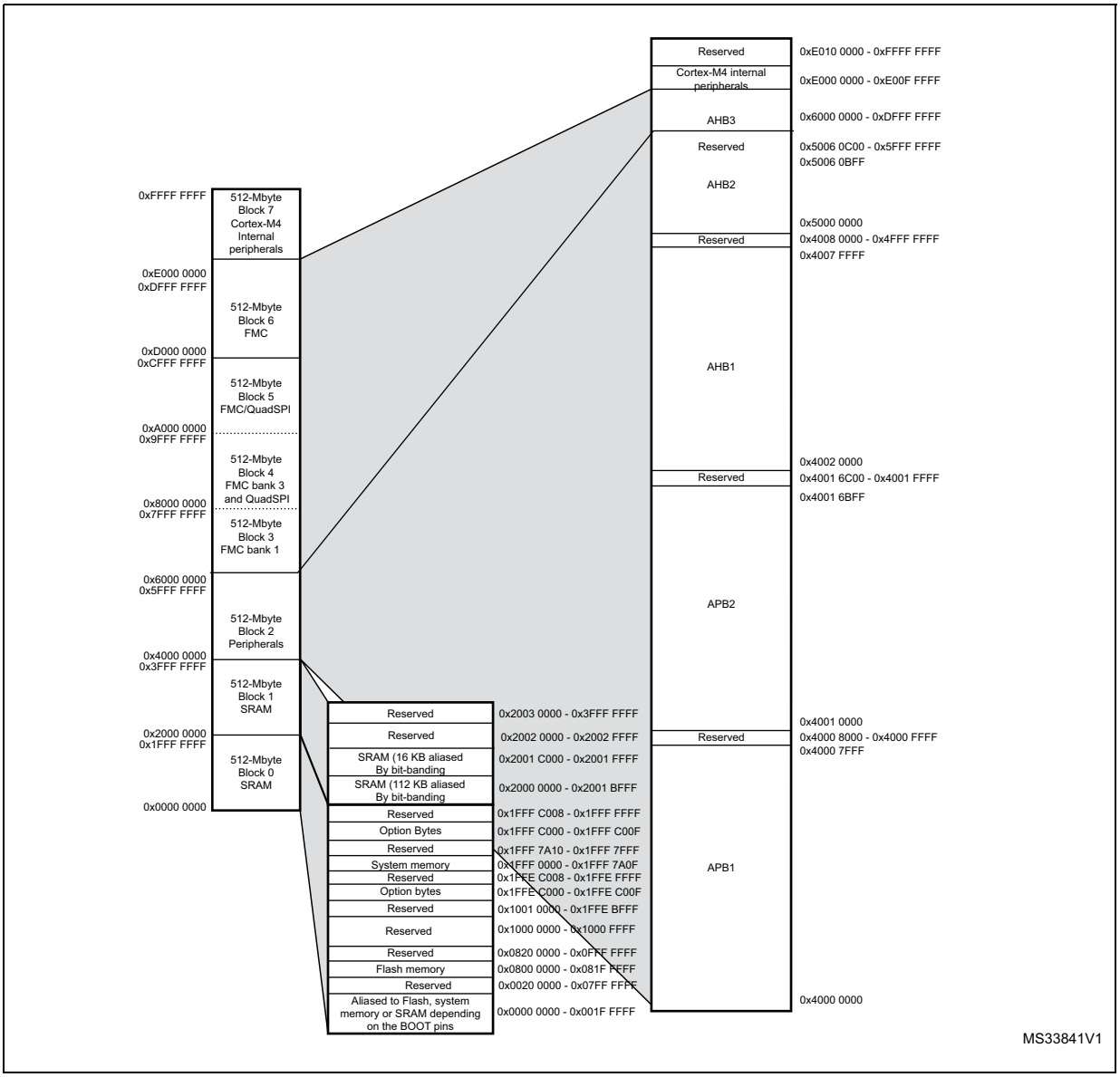


**Table 14. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into sum of all $V_{DD}$ power lines (source)(1) | 240 | mA |
| $\Sigma I_{VSS}$ | Total current out of sum of all $V_{SS}$ ground lines (sink)(1) | - 240 | |
| $\Sigma IV_{DDUSB}$ | Total current into $V_{DDUSB}$ power line (source) | 25 | |
| $I_{VDD}$ | Maximum current into each $V_{DD}$ power pin (source)(1) | 100 | |
| $I_{VSS}$ | Maximum current out of each $V_{SS}$ ground pin (sink)(1) | - 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/Os and control pin | - 25 | |
| $\Sigma I_{IO}$ | Total output current sunk by sum of all I/Os and control pins (2) | 120 | |
| | Total output current sunk by sum of all USB I/Os | 25 | |
| | Total output current sourced by sum of all I/Os and control pins(2) | -120 | |
| $I_{INJ(PIN)}$ | Injected current on FT, FTf, RST and B pins | –5/+0(3) | |
| | Injected current on TTa pins | ±5(4) | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(5) | ±25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. IINJ(PIN) must never be exceeded. Refer to *Table 13* for the maximum allowed input voltage value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 15. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | °C |

**Table 34. Switching output I/O current consumption(1) (continued)**

| Symbol | Parameter | Conditions | I/O toggling frequency (fsw) | Typ | Unit |
|---|---|---|---|---|---|
| $I_{DDIO}$ | I/O switching Current | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 10 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.18 | mA |
| | | | 8 MHz | 0.67 | |
| | | | 25 MHz | 2.09 | |
| | | | 50 MHz | 3.6 | |
| | | | 60 MHz | 4.5 | |
| | | | 84 MHz | 7.8 | |
| | | | 90 MHz | 9.8 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 22 pF<br>C = $C_{INT}$ + $C_{EXT}$ + $C_S$ | 2 MHz | 0.26 | |
| | | | 8 MHz | 1.01 | |
| | | | 25 MHz | 3.14 | |
| | | | 50 MHz | 6.39 | |
| | | | 60 MHz | 10.68 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{EXT}$ = 33 pF<br>C = $C_{INT}$ + Cext + $C_S$ | 2 MHz | 0.33 | |
| | | | 8 MHz | 1.29 | |
| | | | 25 MHz | 4.23 | |
| | | | 50 MHz | 11.02 | |

1. $C_S$ is the PCB board capacitance including the pad pin. $C_S$ = 7 pF (estimated value).
2. This test is performed by cutting the LQFP144 package pin (pad removal).

## On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{HCLK}$ = 180 MHz (Scale1 + over-drive ON), $f_{HCLK}$ = 144 MHz (Scale 2), $f_{HCLK}$ = 120 MHz (Scale 3)"
- Ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

These tests are compliant with EIA/JESD 78A IC latchup standard.

**Table 54. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 55*.

**Table 55. I/O current injection susceptibility(1)**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 pin | –0 | NA | mA |
| | Injected current on NRST pin | –0 | NA | |
| | Injected current on PE2, PE3,PE4, PE5, PE6, PC13, PC14, PF10, PH0, PH1, NRST, PC0, PC1, PC2, PC3, PG15, PB3, PB4, PB5, PB6, PB7, PB8, PB9, PE0, PE1 | –0 | NA | |
| | Injected current on any other FT and FTf pins | -5 | NA | |
| | Injected current on any other pins | –5 | +5 | |

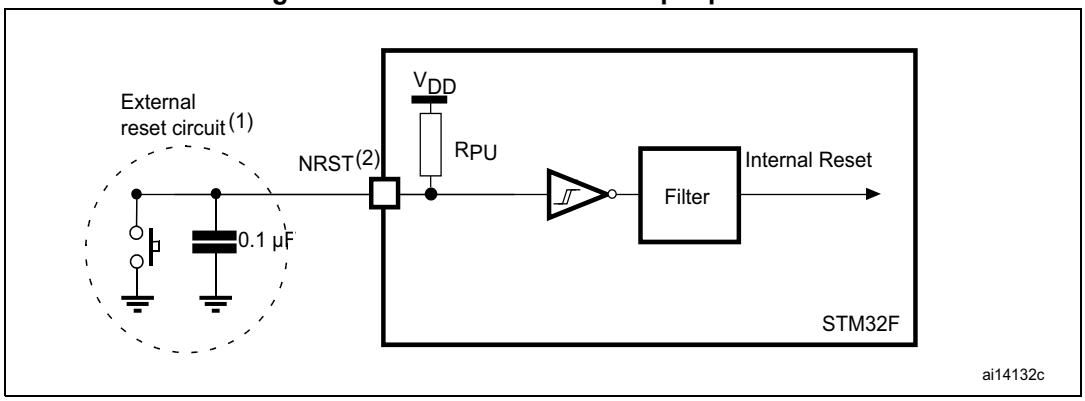
1. NA = not applicable.

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

**Table 58. I/O AC characteristics(1)(2) (continued)**

| OSPEEDRy[1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$≥ 2.7 V | - | - | 25 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$≥ 1.8 V | - | - | 12.5 | |
| | | | $C_L$ = 50 pF, $V_{DD}$≥ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.7 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.8 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.7 V | - | - | 12.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ ≥ 2.7 V | - | - | 10 | ns |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.7 V | - | - | 6 | |
| | | | $C_L$ = 50 pF, $V_{DD}$ ≥ 1.7 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 10 | |
| 10 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 40 pF, $V_{DD}$ ≥ 2.7 V | - | - | 50(4) | MHz |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.7 V | - | - | 100(4) | |
| | | | $C_L$ = 40 pF, $V_{DD}$ ≥ 1.7 V | - | - | 25 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.8 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 42.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 40 pF, $V_{DD}$ ≥2.7 V | - | - | 6 | ns |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.7 V | - | - | 4 | |
| | | | $C_L$ = 40 pF, $V_{DD}$ ≥ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 6 | |
| 11 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 30 pF, $V_{DD}$ ≥ 2.7 V | - | - | 100(4) | MHz |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥ 1.8 V | - | - | 50 | |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥ 1.7 V | - | - | 42.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 2.7 V | - | - | 180(4) | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.8 V | - | - | 100 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 72.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ ≥ 2.7 V | - | - | 4 | ns |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥1.8 V | - | - | 6 | |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥1.7 V | - | - | 7 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.7 V | - | - | 2.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥1.8 V | - | - | 3.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥1.7 V | - | - | 4 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 10 | - | - | ns |

**Figure 33. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 59*. Otherwise the reset is not taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

## 6.3.19 TIM timer characteristics

The parameters given in *Table 60* are guaranteed by design.

Refer to *Section 6.3.17: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 60. TIMx characteristics(1)(2)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 180 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 90 MHz | 1 | - | $t_{TIMxCLK}$ |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK}$ = 180 MHz | 0 | $f_{TIMxCLK}/2$ | MHz |
| $Res_{TIM}$ | Timer resolution | | - | 16/32 | bit |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |

1. TIMx is used as a general term to refer to the TIM1 to TIM12 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 180 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK = 4x PCLKx.

## 6.3.20 Communications interfaces

### $I^2C$ interface characteristics

The $I^2C$ interface meets the requirements of the standard $I^2C$ communication protocol with the following restrictions: the I/O pins SDA and SCL too are mapped as not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

**Figure 35. FMPI$^2$C timing diagram and measurement circuit**

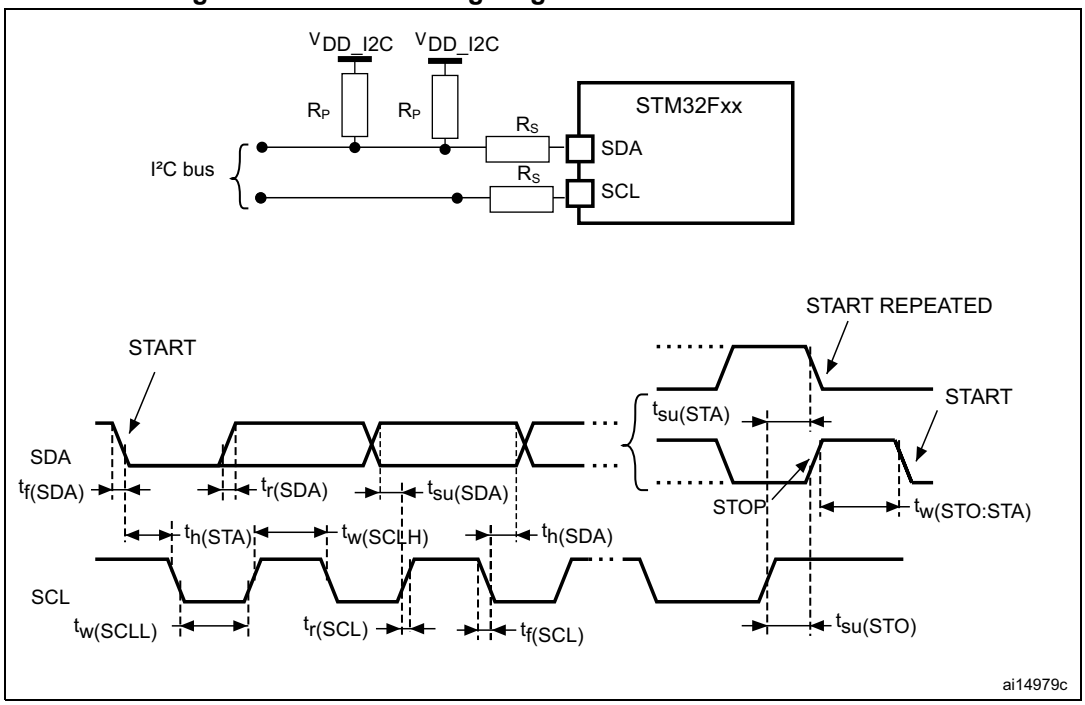


**Table 63. SPI dynamic characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(SCKH)}$ / $t_{w(SCKL)}$ | SCK high and low time | Master mode, SPI presc = 2 | $T_{PCLK}$ - 1.5 | $T_{PCLK}$ | $T_{PCLK}$ + 1.5 | ns |
| $t_{su(NSS)}$ | NSS setup time | Slave mode, SPI presc = 2 | $4T_{PCLK}$ | - | - | |
| $t_{h(NSS)}$ | NSS hold time | Slave mode, SPI presc = 2 | $2T_{PCLK}$ | | | |
| $t_{su(MI)}$ | Data input setup time | Master mode | 4 | - | - | |
| $t_{su(SI)}$ | | Slave mode | 3 | - | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 4 | - | - | |
| $t_{h(SI)}$ | | Slave mode | 2 | - | - | |
| $t_{a(SO)}$ | Data output access time | Slave mode | 7 | - | 21 | |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 5 | - | 12 | |
| $t_{v(SO)}$ | Data output valid/hold time | Slave mode (after enable edge), 2.7V ≤ $V_{DD}$ ≤ 3.6V | - | 7.5 | 22 | |
| | | Slave mode (after enable edge), 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 7.5 | 10.5 | |
| $t_{h(SO)}$ | Data output valid/hold time | Slave mode (after enable edge) | 5 | - | - | |
| $t_{v(MO)}$ | Data output valid time | Master mode (after enable edge) | - | 1.5 | 5 | |
| $t_{h(MO)}$ | Data output hold time | Master mode (after enable edge) | 0 | - | - | |

1. Guaranteed based on test during characterization.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.

**Figure 36. SPI timing diagram - slave mode and CPHA = 0**

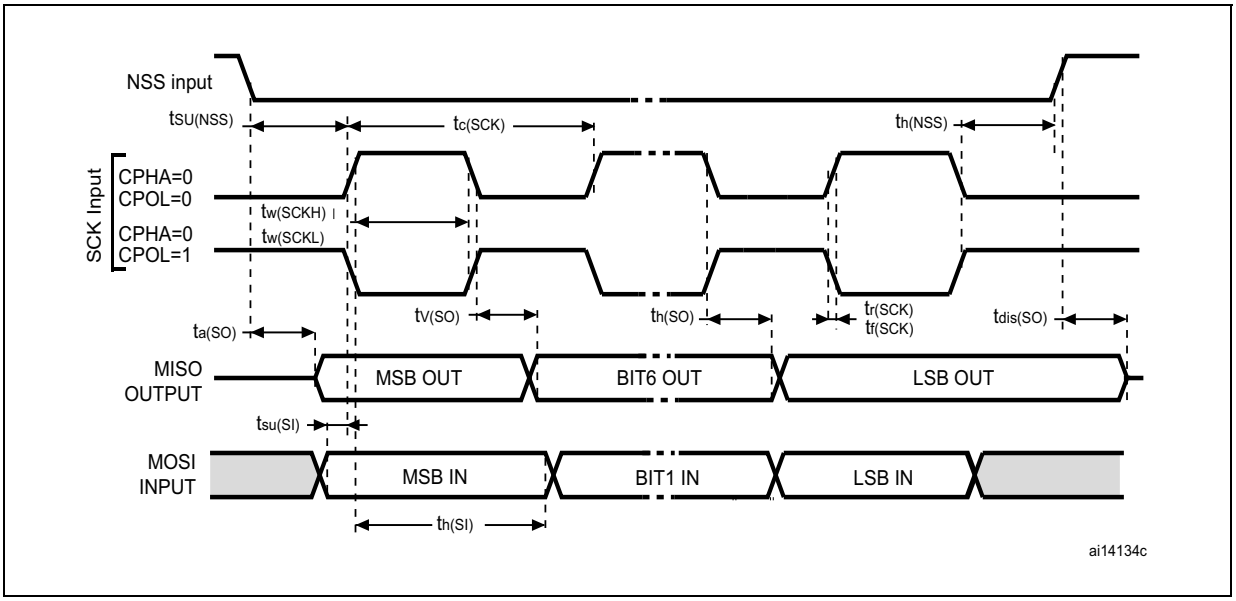


**Table 66. $I^2S$ dynamic characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{v(WS)}$ | WS valid time | Master mode | - | 5.5 | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 1 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 1 | - | |
| - | | PCM short pulse Slave mode(3) | 2 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 3 | - | |
| - | | PCM short pulse Slave mode(3) | 1.5 | - | |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 3 | - | |
| $t_{su(SD\_SR)}$ | | Slave receiver | 2.5 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 4 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 1 | - | |
| $t_{v(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 16 | |
| $t_{v(SD\_MT)}$ | | Master transmitter (after enable edge) | - | 4.5 | |
| $t_{h(SD\_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 5 | - | |
| $t_{h(SD\_MT)}$ | | Master transmitter (after enable edge) | 1 | - | |

1. Guaranteed based on test during characterization.
2. The maximum value of 256xFs is 45 MHz (APB1 maximum frequency).
3. Measurement done with respect to I2S_CK rising edge.

*Note: Refer to the I2S section of RM0390 reference manual for more details on the sampling frequency ($F_S$).*

*$f_{MCK}$, $f_{CK}$, and $D_{CK}$ values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. $D_{CK}$ depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). $F_S$ maximum value is supported for each mode/condition.*

**Figure 41. SAI master timing waveforms**

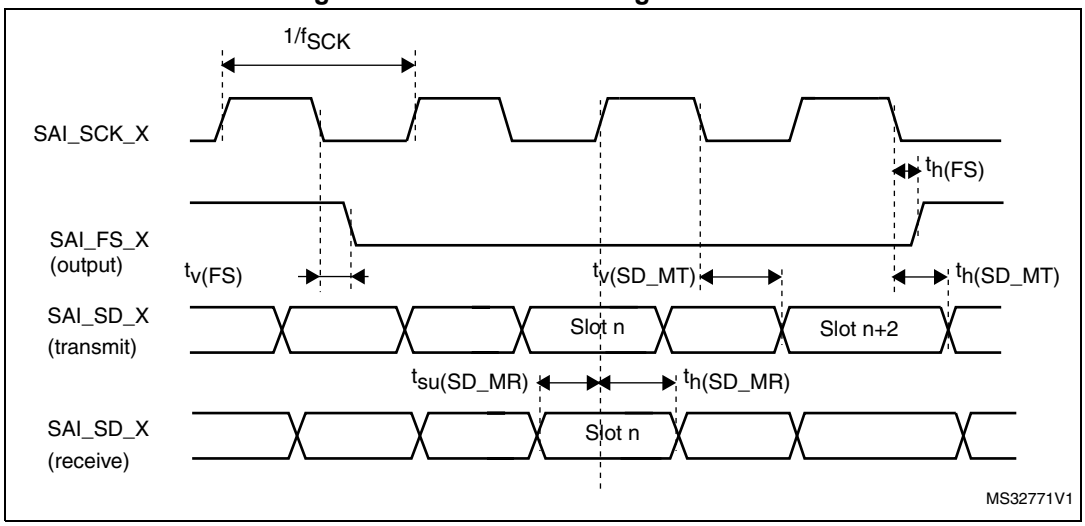
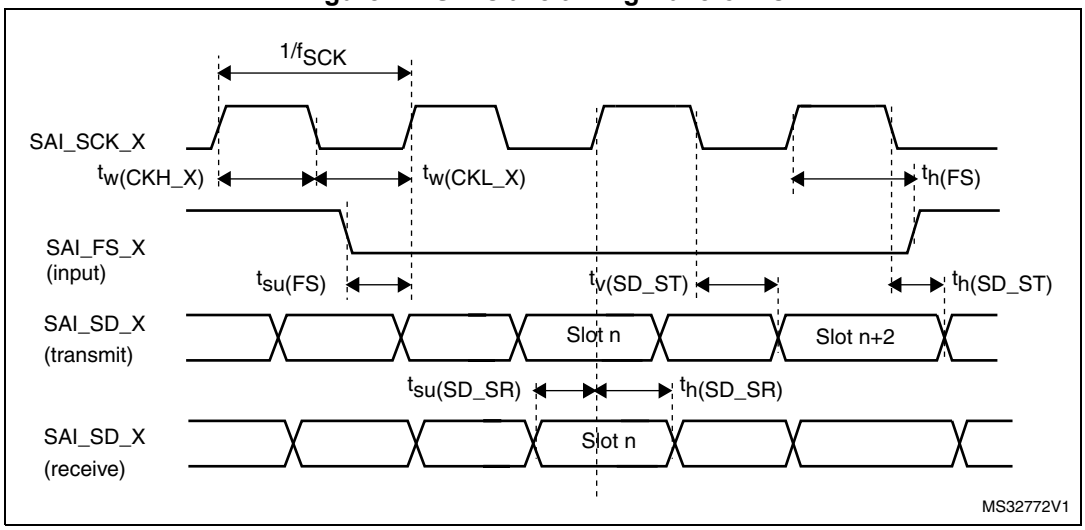



**Figure 42. SAI slave timing waveforms**




## USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

**Table 68. USB OTG full speed startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB OTG full speed transceiver startup time | 1 | µs |

1. Guaranteed by design.

**Figure 53. Asynchronous multiplexed PSRAM/NOR write waveforms**

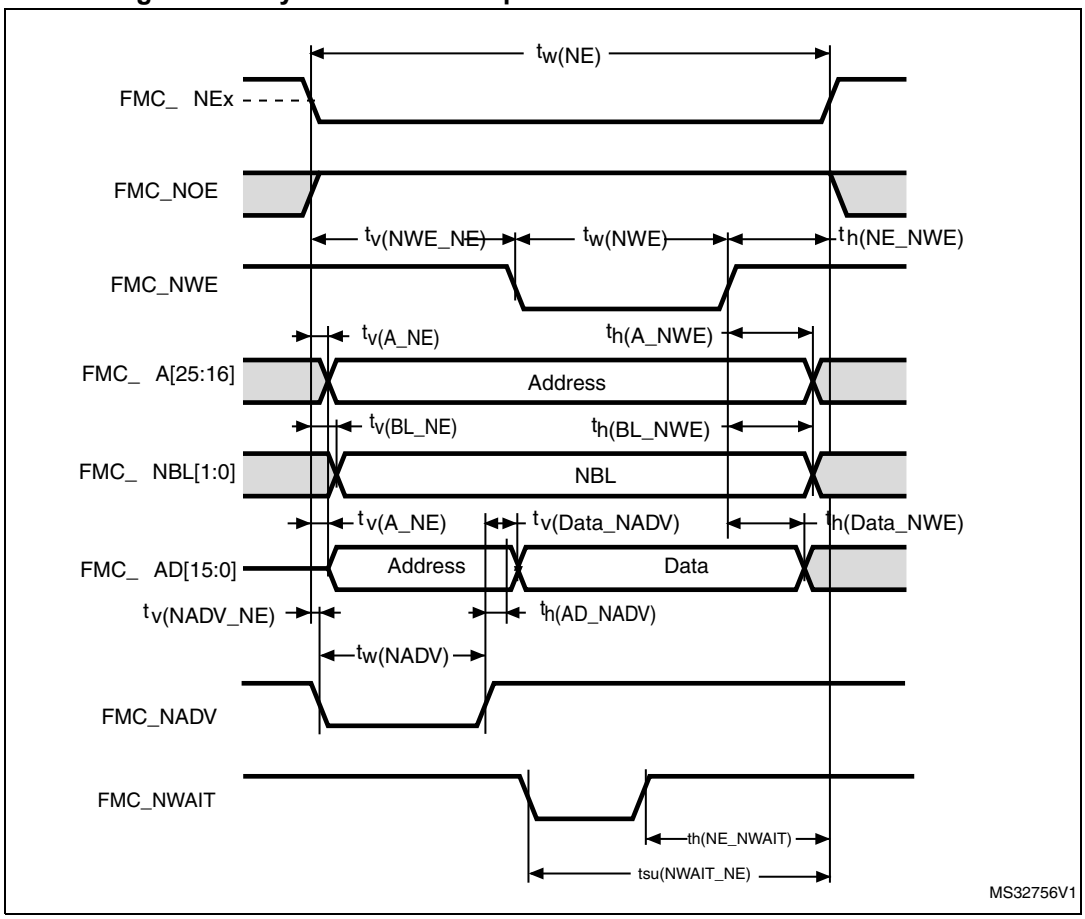


**Table 103. LPSDR SDRAM write timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $F_{(SDCLK)}$ | Frequency of operation | - | 84 | MHz |
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK}$ - 0.5 | $2T_{HCLK}$ + 0.5 | ns |
| $t_{d(SDCLKL\_Data)}$ | Data output valid time | - | 5 | |
| $t_{h(SDCLKL\_Data)}$ | Data output hold time | 0.5 | - | |
| $t_{d(SDCLK\_Add)}$ | Address valid time | - | 3 | |
| $t_{d(SDCLKL\_SDNWE))}$ | SDNWE valid time | - | 3 | |
| $t_{h(SDCLKL\_SDNWE))}$ | SDNWE hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNE))}$ | Chip select valid time | - | 2.5 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | - | 2 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | - | 2 | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. CL = 10 pF.
2. Guaranteed based on test during characterization.

## 6.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 104* for DCMI are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage summarized in *Table 16*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

**Table 104. DCMI characteristics**

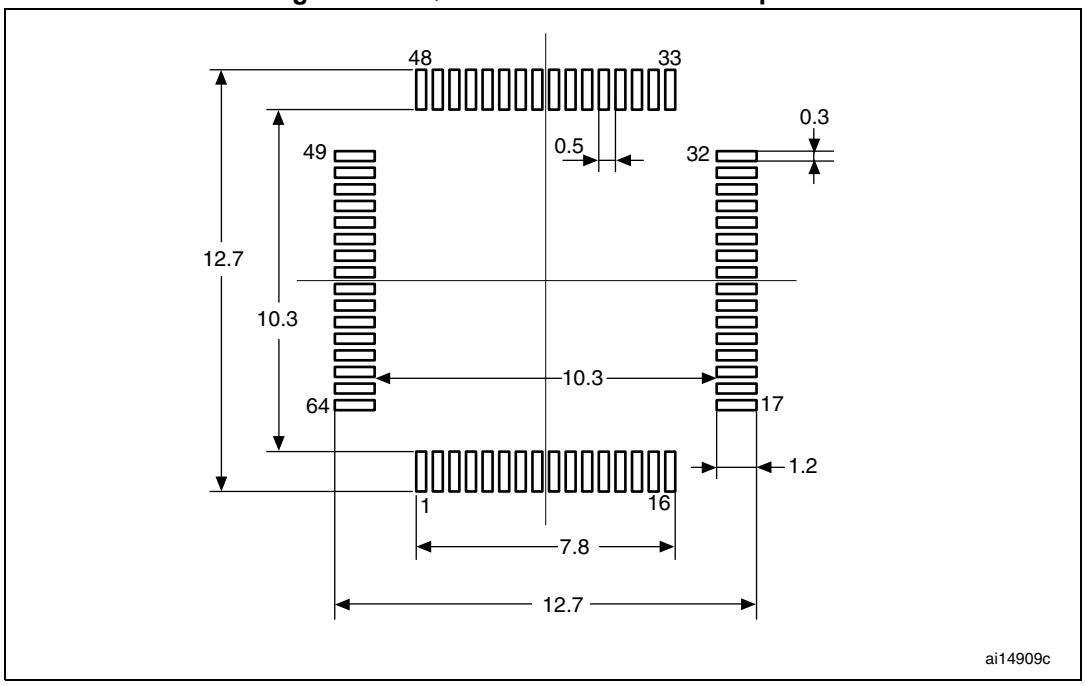
| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| - | Frequency ratio DCMI_PIXCLK/$f_{HCLK}$ | - | 0.4 | - |
| DCMI_PIXCLK | Pixel clock input | - | 54 | MHz |
| $D_{Pixel}$ | Pixel clock input duty cycle | 30 | 70 | % |
| $t_{su(DATA)}$ | Data input setup time | 1 | - | ns |
| $t_{h(DATA)}$ | Data input hold time | 3.5 | - | |
| $t_{su(HSYNC)}$ $t_{su(VSYNC)}$ | DCMI_HSYNC/DCMI_VSYNC input setup time | 2 | - | |
| $t_{h(HSYNC)}$ $t_{h(VSYNC)}$ | DCMI_HSYNC/DCMI_VSYNC input hold time | 0 | - | |

**Table 108. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| D | 11.800 | 12.000 | 12.200 | 0.4646 | 0.4724 | 0.4803 |
| D1 | 9.800 | 10.000 | 10.200 | 0.3858 | 0.3937 | 0.4016 |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | 11.800 | 12.000 | 12.200 | 0.4646 | 0.4724 | 0.4803 |
| E1 | 9.800 | 10.000 | 10.200 | 0.3858 | 0.3937 | 0.4016 |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 68. LQFP64 Recommended footprint**



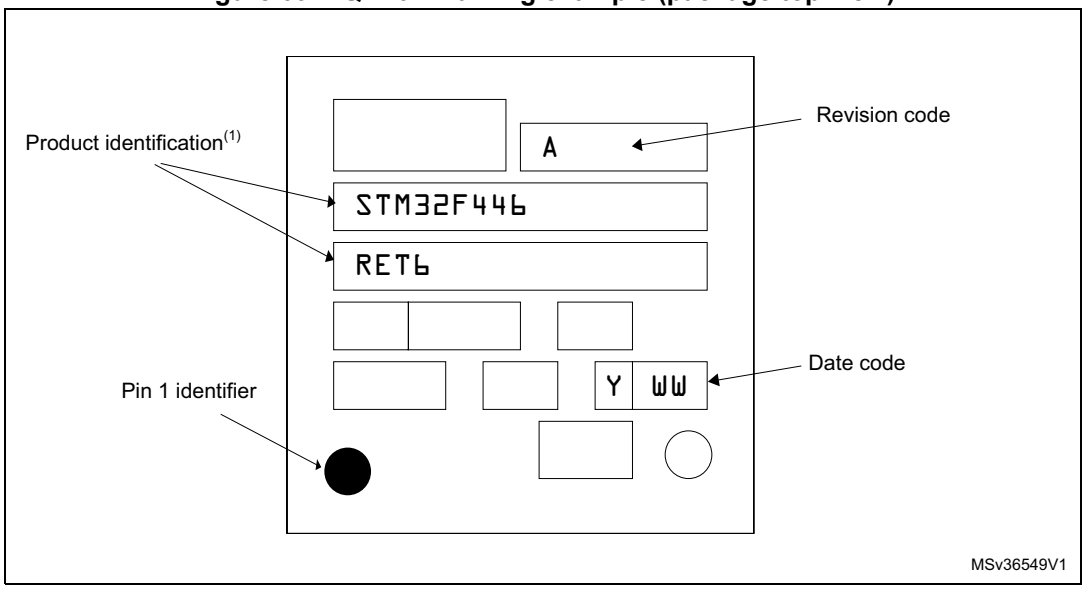

1. Drawing is not to scale.
2. Dimensions are in millimeters.

### Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

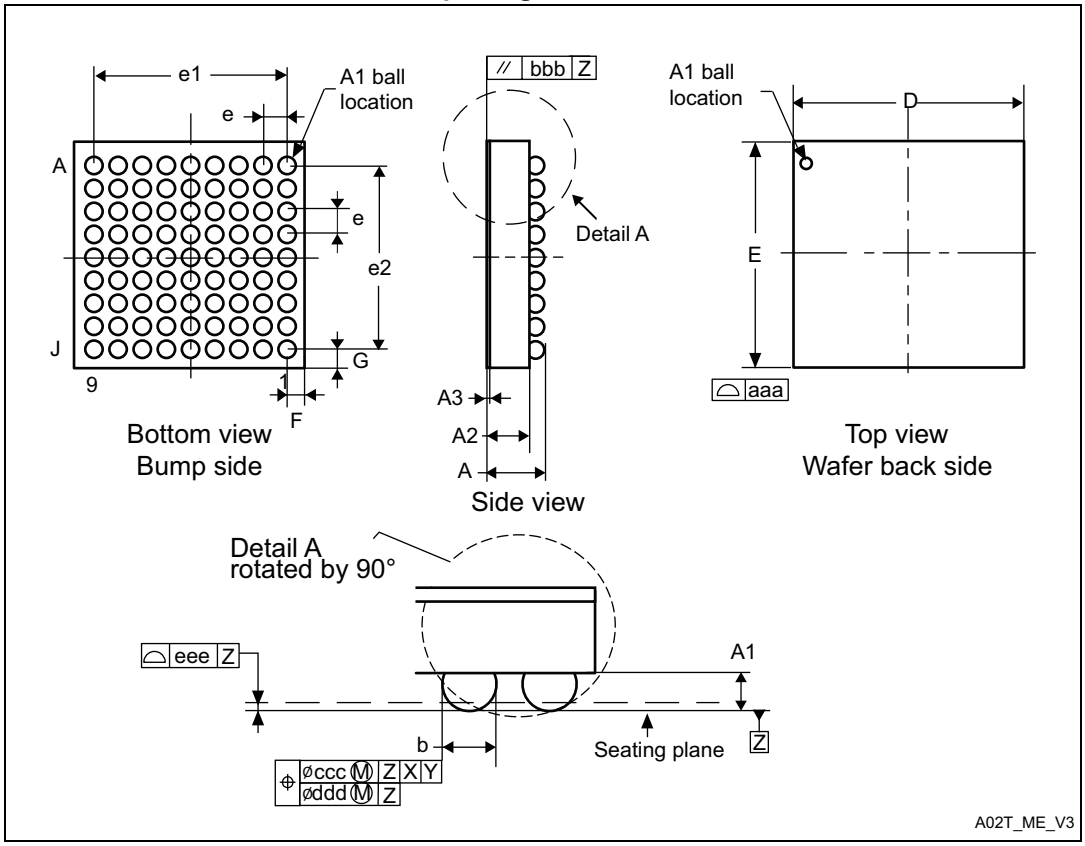
**Figure 69. LQFP64 marking example (package top view)**




1. Parts marked as “ES”, "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.6 WLCSP81 package information

**Figure 82. WLCSP81 - 81-pin, 3.693 x 3.815 mm, 0.4 mm pitch wafer level chip scale package outline**




1. Drawing is not to scale.

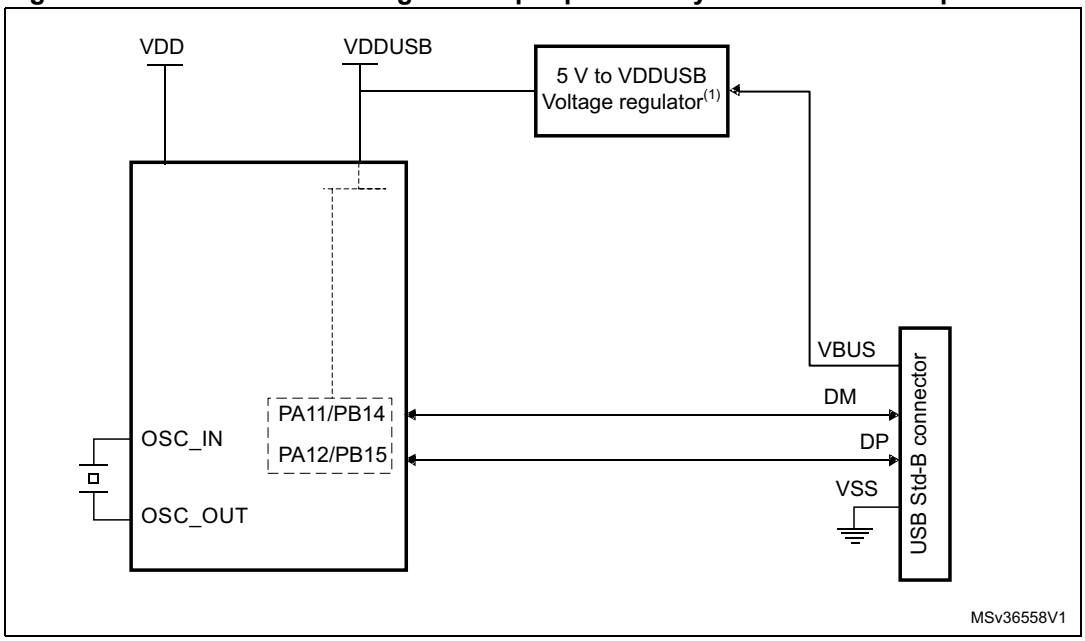
**Table 115. WLCSP81- 81-pin, 3.693 x 3.815 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 0.600 | - | - | 0.0236 |
| A1 | - | 0.170 | - | - | 0.0067 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| b[3] | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 3.658 | 3.693 | 3.728 | 0.1440 | 0.1454 | 0.1468 |
| E | 3.780 | 3.815 | 3.850 | 0.1488 | 0.1502 | 0.1516 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 3.200 | - | - | 0.1260 | - |
| e2 | - | 3.200 | - | - | 0.1260 | - |

# Appendix A Application block diagrams

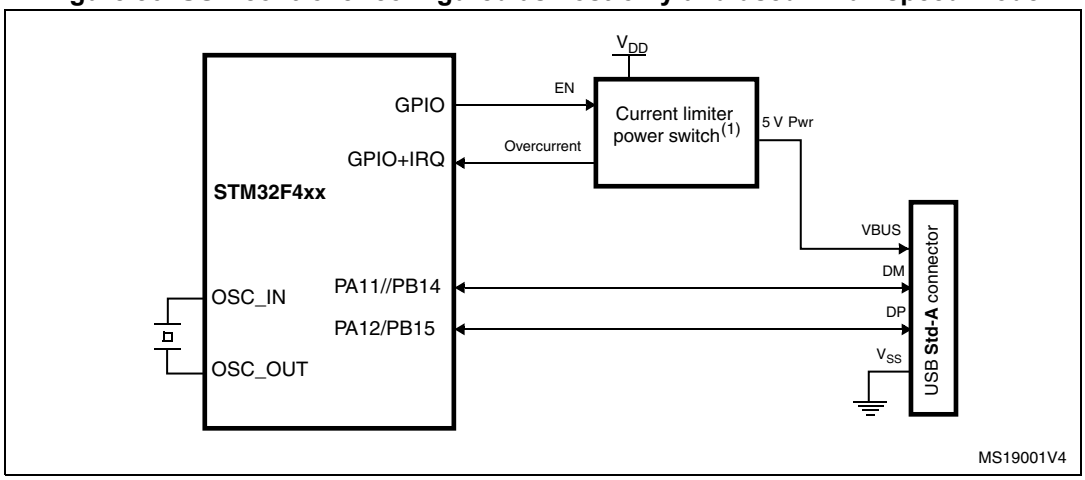
## A.1 USB OTG full speed (FS) interface solutions

**Figure 85. USB controller configured as peripheral-only and used in Full speed mode**




1. External voltage regulator only needed when building a $V_{BUS}$ powered device.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

**Figure 86. USB controller configured as host-only and used in full speed mode**




1. The current limiter is required only if the application has to support a $V_{BUS}$ powered device. A basic power switch can be used if 5 V are available on the application board.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.