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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446zch6

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1 Introduction

This document provides the description of the STM32F446xC/E products.

The STM32F446xC/E document should be read in conjunction with the STM32F4xx reference manual.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214), available from the www.st.com.

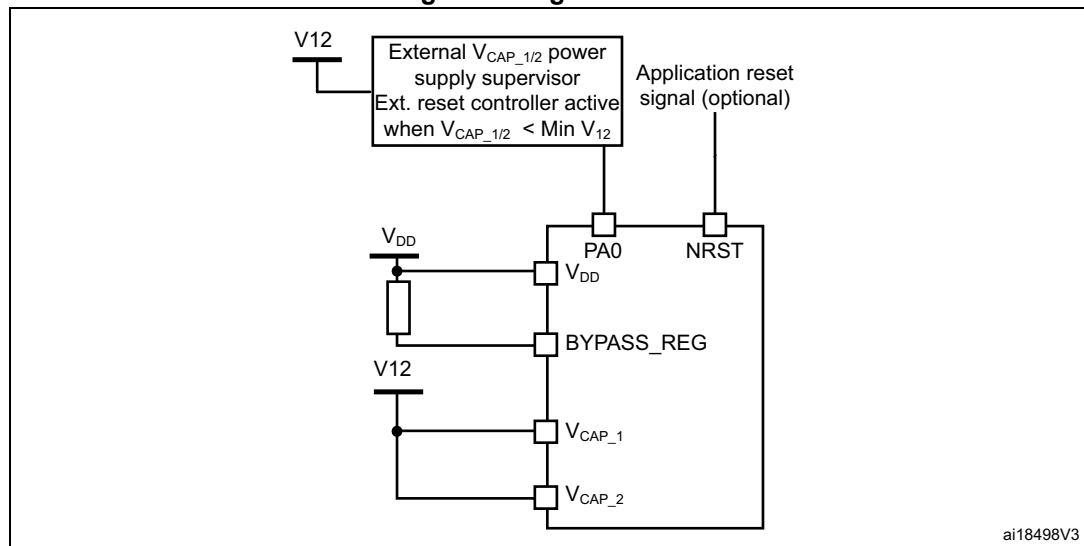
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. The two 2.2 μF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12} . An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.

Figure 7. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see [Figure 8](#)).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 9](#)).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

The SPDIF-RX also offers a signal named `spdifrx_frame_sync`, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

3.28 Serial Audio interface (SAI)

The devices feature two serial audio interfaces (SAI1 and SAI2). Each serial audio interfaces based on two independent audio sub blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub blocks can be configured in master or in slave mode. The SAIs use a PLL to achieve audio class accuracy.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 and SA2 can be served by the DMA controller.

3.29 Audio PLL (PLL^{I2S})

The devices feature an additional dedicated PLL for audio I²S and SAI applications. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I²S/SAI flow with an external PLL (or Codec output).

3.30 Serial Audio Interface PLL(PLLSAI)

An additional PLL dedicated to audio and USB is used for SAI1 and SAI2 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the 48MHz clock for USB FS and SDIO in case the system PLL is programmed with factors not multiple of 48MHz.

3.31 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.41 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F446xx through a small number of ETM pins to an external hardware trace port analyser (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

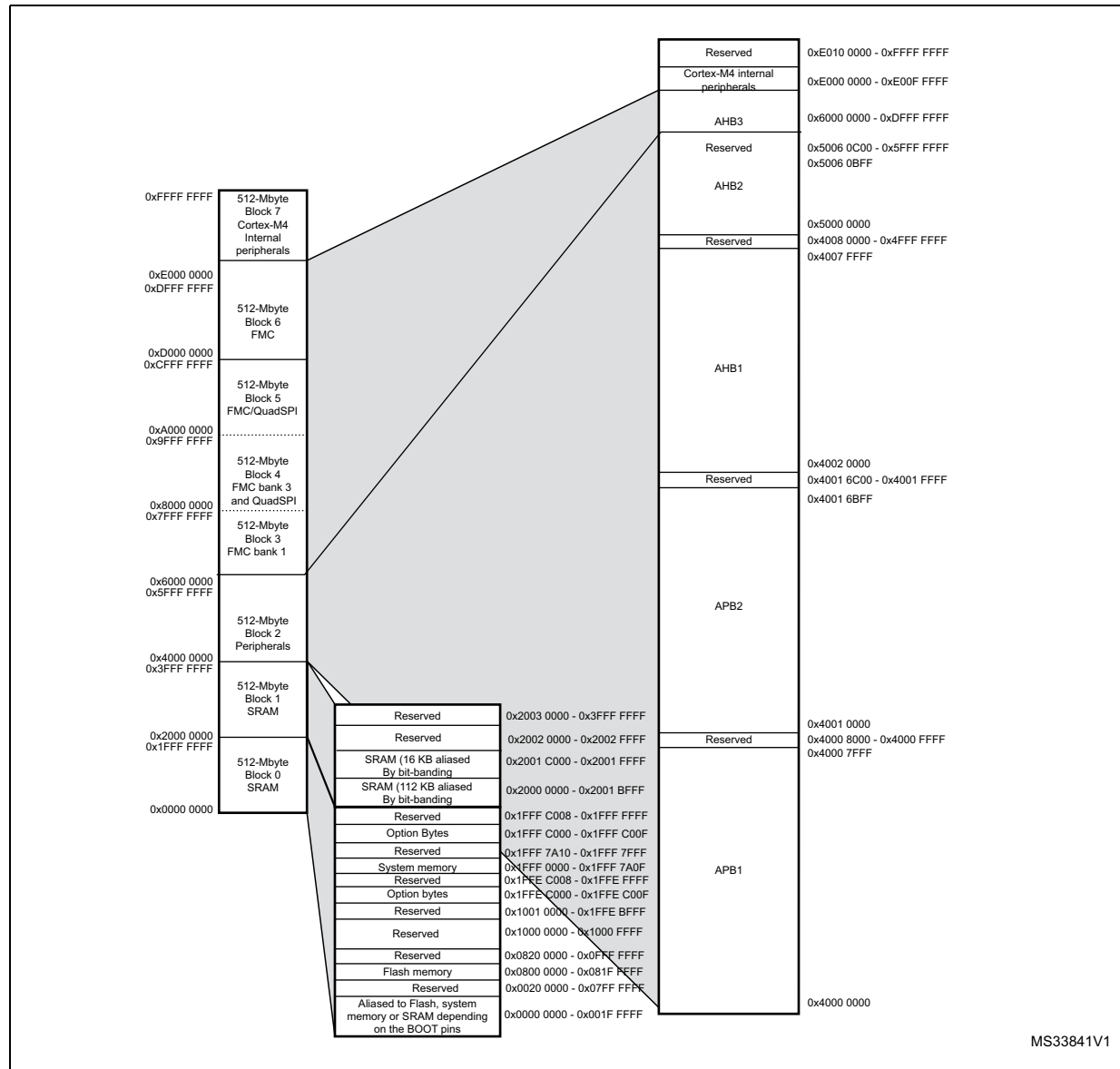
Table 11. Alternate function

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11/ CEC	I2C1/2/3 /4/CEC	SPI1/2/3/ 4	SPI2/3/4/ SAI1	SPI2/3/ USART1/ 2/3/UART 5/SPDIFR X	SAI/ USART6/ UART4/5/ SPDIFRX	CAN1/2 TIM12/13/ 14/ QUADSPI	SAI2/ QUADSPI/ OTG2_HS/ OTG1_FS	OTG1_FS	FMC/ SDIO/ OTG2_FS	DCMI	-	SYS
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_ CTS	UART4_ TX	-	-	-	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_ RTS	UART4_ RX	QUADSPI_ BK1_IO3	SAI2_ MCLK_B	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_ TX	SAI2_ SCK_B	-	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	SAI1_ FS_A	USART2_ RX	-	-	OTG_HS_ ULPI_D0	-	-	-	-	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	USART2_ CK	-	-	-	-	OTG_HS_ SOF	DCMI_ HSYNC	-	EVENT OUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	TIM8_ CH1N	-	SPI1_SCK/ I2S1_CK	-	-	-	-	OTG_HS_ ULPI_CK	-	-	-	-	EVENT OUT
	PA6	-	TIM1_ BKIN	TIM3_CH1	TIM8_ BKIN	-	SPI1_MISO	I2S2_ MCK	-	-	TIM13_CH1	-	-	-	DCMI_ PIXCLK	-	EVENT OUT
	PA7	-	TIM1_ CH1N	TIM3_CH2	TIM8_ CH1N	-	SPI1_MOSI/ I2S1_SD	-	-	-	TIM14_CH1	-	-	FMC_ SDNWE	-	-	EVENT OUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_ SCL	-	-	USART1_ CK	-	-	OTG_FS_ SOF	-	-	-	-	EVENT OUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	SPI2_SCK/ I2S2_CK	SAI1_ SD_B	USART1_ TX	-	-	-	-	-	DCMI_D0	-	EVENT OUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_ RX	-	-	OTG_FS_ ID	-	-	DCMI_D1	-	EVENT OUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_ CTS	-	CAN1_RX	OTG_FS_ DM	-	-	-	-	EVENT OUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_ RTS	SAI2_ FS_B	CAN1_TX	OTG_FS_ DP	-	-	-	-	EVENT OUT
	PA13	JTMS- SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK- SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-	HDMI_ CEC	SPI1_NSS/ I2S1_WS	SPI3_ NSS/ I2S3_WS	-	UART4_RT S	-	-	-	-	-	-	EVENT OUT

5 Memory mapping

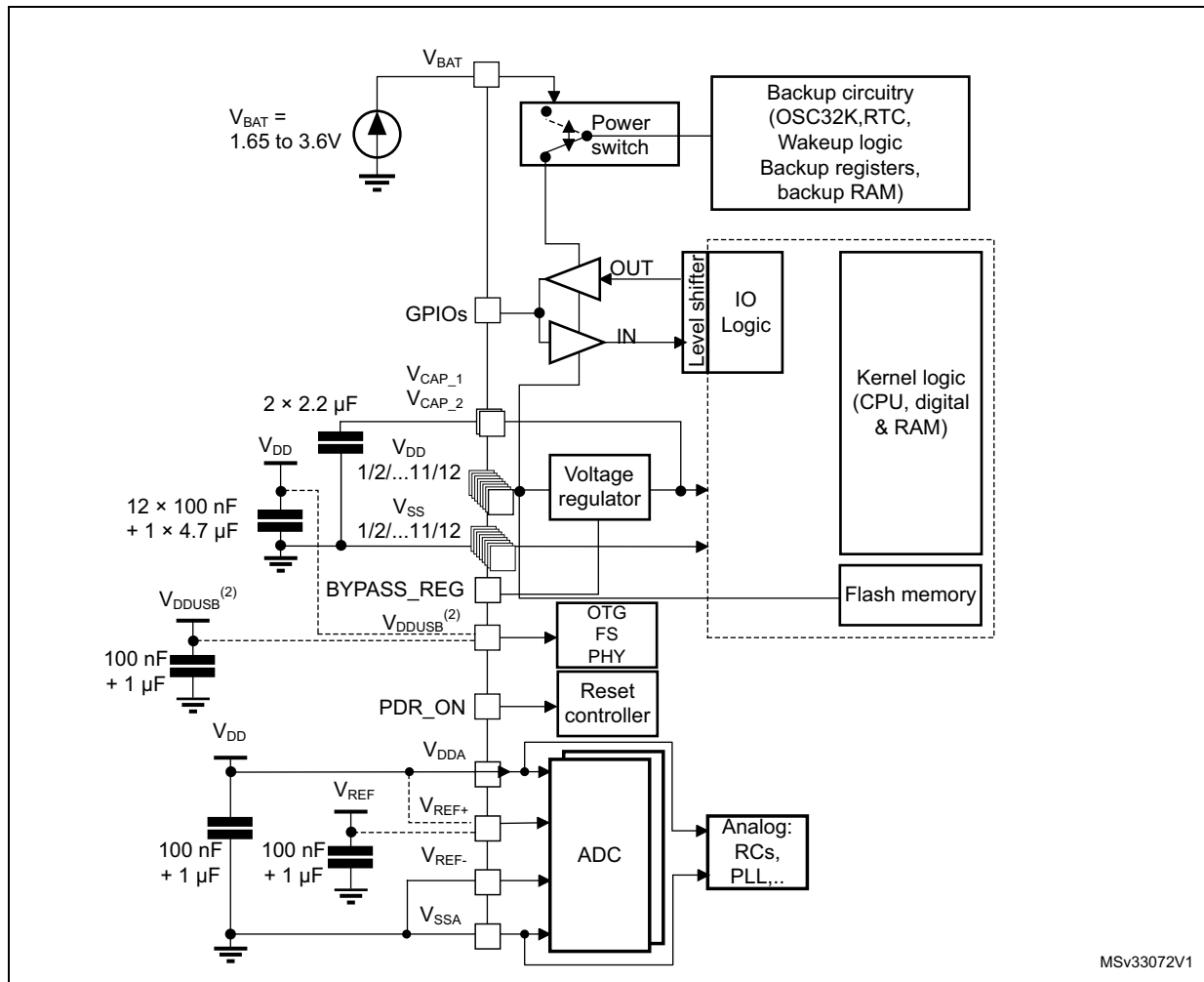
The memory map is shown in *Figure 15*

Figure 15. Memory map



6.1.6 Power supply scheme

Figure 18. Power supply scheme



1. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
2. V_{DDUSB} is a dedicated independent USB power supply for the on-chip full-speed OTG PHY module and associated DP/DM GPIOs. Its value is independent from the V_{DD} and V_{DDA} values, but must be the last supply to be provided and the first to disappear. If V_{DD} is different from V_{DDUSB} and only one on-chip OTG PHY is used, the second OTG PHY GPIOs (DP/DM) are still supplied at V_{DDUSB} (3.3V).
3. V_{DDUSB} is available only on WLCSP81, UFBGA144 and LQFP144 packages. For packages where V_{DDUSB} pin is not available, it is internally connected to V_{DD} .
4. V_{CAP_2} pad is not available on LQFP64.

Caution: Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

Table 33. Typical current consumption in Sleep mode, regulator OFF⁽¹⁾

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	VDD=3.3 V		VDD=1.7 V		Unit
				I _{DD12}	I _{DD}	I _{DD12}	I _{DD}	-
I _{DD12} /I _{DD}	Supply current in Sleep mode from V ₁₂ and V _{DD} supply	All Peripherals enabled	180	47.605	1.2	NA	NA	mA
			168	44.35	1.0	41.53	0.8	
			150	40.58	0.9	39.96	0.8	
			144	35.68	0.9	34.60	0.7	
			120	27.30	0.9	29.11	0.7	
			90	20.69	0.8	19.78	0.6	
			60	13.88	0.7	13.36	0.6	
			30	7.66	0.7	7.85	0.6	
			25	6.49	0.7	6.66	0.5	
		All Peripherals disabled	180	8.71	1.2	NA	NA	
			168	7.00	0.9	8.42	0.8	
			150	6.88	0.9	7.61	0.8	
			144	6.29	0.9	6.99	0.7	
			120	4.87	0.9	5.95	0.7	
			90	3.78	0.8	3.96	0.6	
			60	2.66	0.7	2.80	0.6	
			30	1.65	0.7	1.74	0.6	
			25	1.45	0.7	1.52	0.5	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 56: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	6	6	CPU clock cycle
$T_{WUSLEEPFDSM}^{(1)}$	Wakeup from Sleep with Flash memory in Deep power down mode	-	33.5	50	μs
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	12.8	15	
		Main regulator is ON and Flash memory in Deep power down mode	104.9	115	
		Low power regulator is ON	20.6	28	
		Low power regulator is ON and Flash memory in Deep power down mode	112.8	120	
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	110	140	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	114.4	128	
$t_{WUSTDBY}^{(2)(3)}$	Wakeup from Standby mode	-	325	400	

1. Guaranteed based on test during characterization.

2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

3. $t_{WUSTDBY}$ maximum value is given at $-40\text{ }^{\circ}\text{C}$.

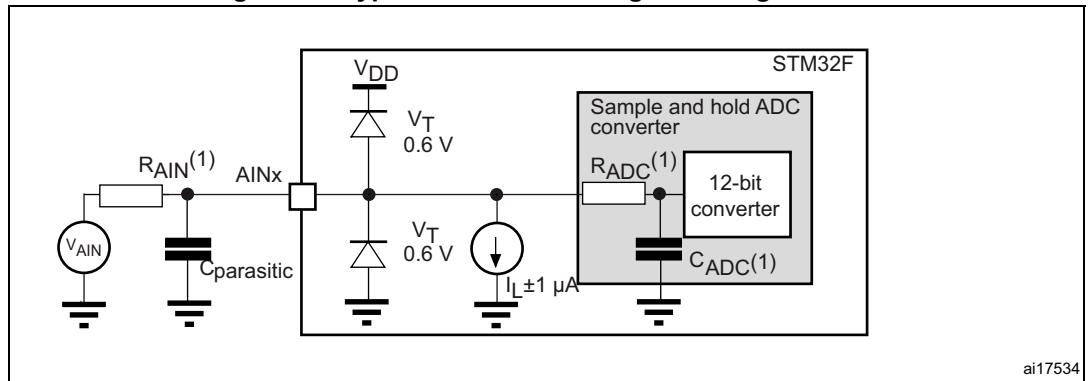
6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 56: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 23](#).

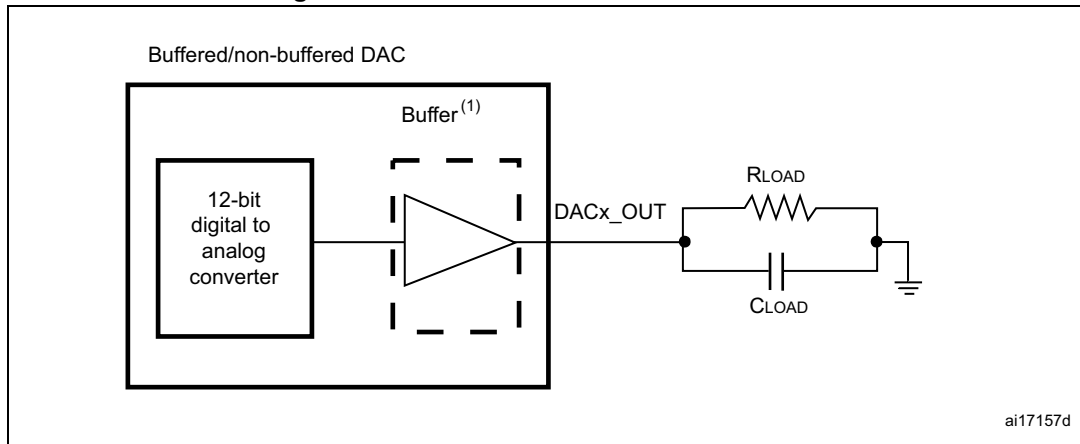
The characteristics given in [Table 37](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 16](#).

Figure 46. Typical connection diagram using the ADC



1. Refer to [Table 74](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 49. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 90. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 2$	$3T_{HCLK} + 0.5$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK} - 0.5$	$2T_{HCLK}$	
$t_{w(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK} + 0.5$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	2	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	0	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 1.5$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK} + 1$	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. $C_L = 30$ pF.
2. Guaranteed based on test during characterization.

Table 91. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK} - 1$	$8T_{HCLK} + 2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} + 1.5$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 1$	-	

1. $C_L = 30$ pF.
2. Guaranteed based on test during characterization.

Figure 53. Asynchronous multiplexed PSRAM/NOR write waveforms

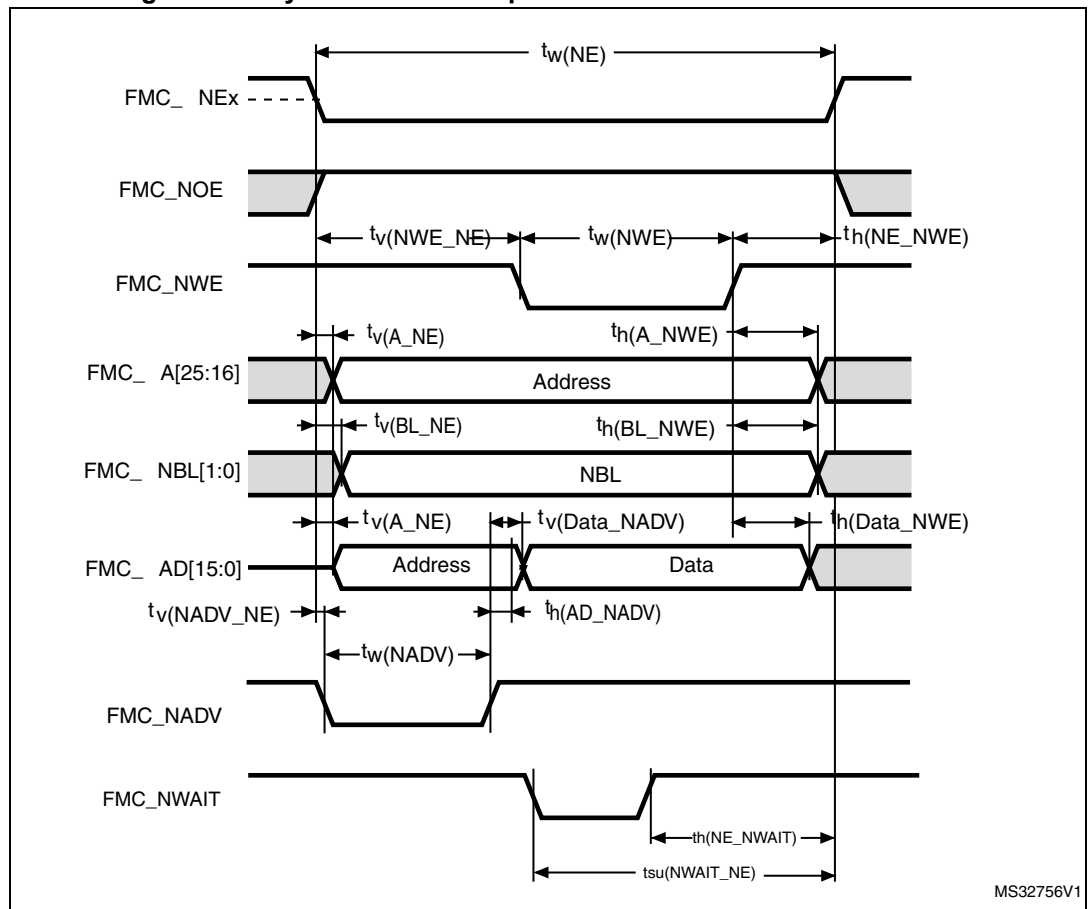


Table 92. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK} - 2$	$4T_{HCLK} + 0.5$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}	$T_{HCLK} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{HCLK} - 2$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{HCLK} + 1.5$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK} + 0.5$	-	

1. $C_L = 30$ pF.
2. Guaranteed based on test during characterization.

Table 93. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK} + 0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK} + 2$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} + 1.5$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} - 1$	-	

1. $C_L = 30$ pF.
2. Guaranteed based on test during characterization.

Synchronous waveforms and timings

[Figure 54](#) through [Figure 57](#) represent synchronous waveforms and [Table 94](#) through [Table 97](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F446 reference manual: RM0390)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Table 97. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low ($x=0..2$)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high ($x=0..2$)	$T_{HCLK} - 0.5$	-	
$t_{d(CLKL-NADV_L)}$	FMC_CLK low to FMC_NADV low	-	2	
$t_{d(CLKL-NADV_H)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid ($x=16..25$)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid ($x=16..25$)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	3	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{HCLK} + 1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	2.5	
$t_{d(CLKL-NBL_L)}$	FMC_CLK low to FMC_NBL low	3	-	
$t_{d(CLKH-NBL_H)}$	FMC_CLK high to FMC_NBL high	$T_{HCLK} + 1.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	0	-	

1. $C_L = 30$ pF.

2. Guaranteed based on test during characterization.

NAND controller waveforms and timings

[Figure 58](#) through [Figure 61](#) represent synchronous waveforms, and [Table 98](#) and [Table 99](#) provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

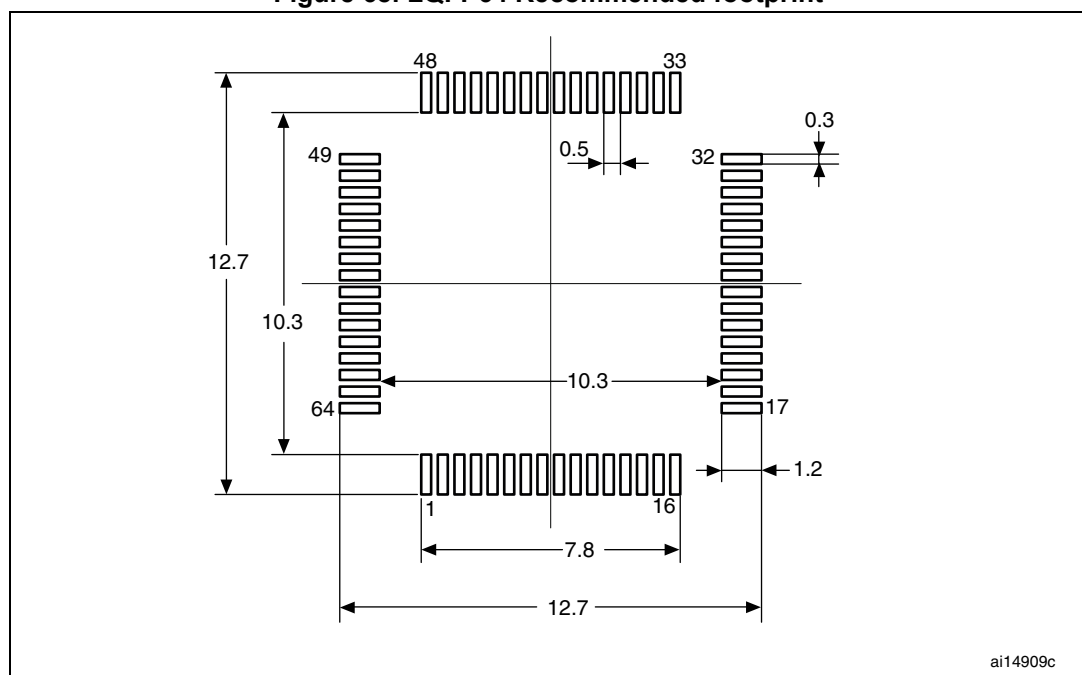
In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 108. LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D3	-	7.500	-	-	0.2953	-
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 68. LQFP64 Recommended footprint



1. Drawing is not to scale.
2. Dimensions are in millimeters.

7.7 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 117. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm	46	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	42	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	33	
	Thermal resistance junction-ambient UFBGA144 - 7 × 7 mm / 0.5 mm pitch	51	
	Thermal resistance junction-ambient UFBGA144 - 10 × 10 mm / 0.8 mm pitch	48	
	Thermal resistance junction-ambient WLCSP81	48	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Revision history

Table 119. Document revision history

Date	Revision	Changes
17-Feb-2015	1	Initial release.
16-Mar-2015	2	<p>Added note 2 inside Table 2</p> <p>Updated Table 11, Table 23, Table 24, Table 25, Table 26, Table 30, Table 51, Table 52, Table 53, and Table 61</p> <p>Added condition inside Typical and maximum current consumption and Additional current consumption</p> <p>Added FMPI2C characteristics</p> <p>Added Table 62 and Figure 35</p>
29-May-2015	3	<p>Updated:</p> <ul style="list-style-type: none"> – Section 6.3.15: Absolute maximum ratings (electrical sensitivity) – Section 7: Package information – Table 2: STM32F446xC/E features and peripheral counts – Table 13: STM32F446xC/xE WLCSP81 ballout – Figure 53: ESD absolute maximum ratings – Figure 54: Synchronous multiplexed NOR/PSRAM read timings <p>Added:</p> <ul style="list-style-type: none"> – Figure 78: UQFP144 7 x 7 mm marking example (package top view), – Figure 81: UQFP144 10 x 10 mm marking example (package top view), – Figure 84: WLCSP81 10 x 10 mm marking example (package top view)
10-Aug-2015	4	<p>Updated:</p> <ul style="list-style-type: none"> – Figure 14: STM32F446xC/xE UFBGA144 ballout – Table 10: STM32F446xx pin and ball descriptions – Table 18: VCAP_1/VCAP_2 operating conditions – Section 3.15: Power supply schemes – Section 6.3.2: VCAP_1/VCAP_2 external capacitor <p>Added:</p> <ul style="list-style-type: none"> – Figure 5: VDDUSB connected to an external independent power supply – Notes 3 and 4 below Figure 18: Power supply scheme

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