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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446zch7

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3 Functional overview

3.1 ARM[®] Cortex[®]-M4 with FPU and embedded Flash and SRAM

The ARM[®] Cortex[®]-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM[®] Cortex[®]-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F446xC/E family is compatible with all ARM tools and software.

Figure 3 shows the general block diagram of the STM32F446xC/E family.

Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the ARM[®] Cortex[®]-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP144	Yes	No	Yes PDR_ON set to V _{DD}	Yes PDR_ON set to V _{SS}
UFBGA144	Yes BYPASS_REG set to V _{ss}	Yes BYPASS_REG set to V _{DD}		
WLCSP81				

3.18 Real-time clock (RTC), backup SRAM and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The 4-Kbyte backup SRAM is an EEPROM-like memory area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled by default to minimize power consumption (see [Section 3.19: Low-power modes](#)). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see [Section 3.19: Low-power modes](#)).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.19 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

3.20 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

3.21.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.21.2 General-purpose timers (TIMx)

There are ten synchronized general-purpose timers embedded in the STM32F446xC/E devices (see [Table 6](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F446xC/E include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

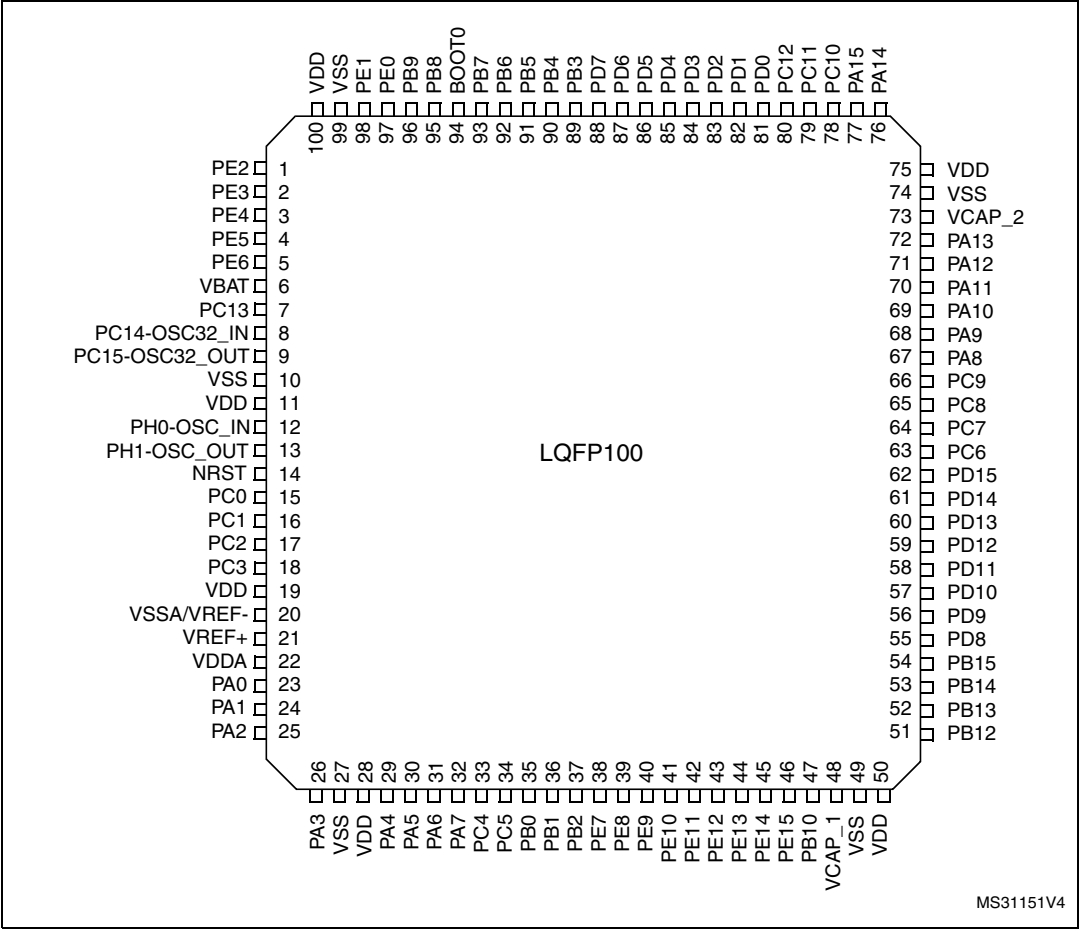
These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

3.21.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

Figure 11. STM32F446xC/xE LQFP100 pinout



1. The above figure shows the package top view.

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
6	13	F9	E1	24	PH1-OSC_OUT(PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	14	D8	F1	25	NRST	I/O	RS T	-	-	-
8	15	G9	H1	26	PC0	I/O	FT	-	SAI1_MCLK_B, OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT	ADC123_IN10
9	16	-	H2	27	PC1	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, SPI2_MOSI/I2S2_SD, EVENTOUT	ADC123_IN11
10	17	E8	H3	28	PC2	I/O	FT	-	SPI2_MISO, OTG_HS_ULPI_DIR, FMC_SDNE0, EVENTOUT	ADC123_IN12
11	18	F8	H4	29	PC3	I/O	FT	-	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, FMC_SDCKE0, EVENTOUT	ADC123_IN13
-	19	H9	-	30	VDD	S	-	-	-	-
-	-	G8	-	-	VSS	S	-	-	-	-
12	20	F7	J1	31	VSSA	S	-	-	-	-
-	-	-	K1	-	VREF-	S	-	-	-	-
-	21	-	L1	32	VREF+	S	-	-	-	-
13	22	H8	M1	33	VDDA	S	-	-	-	-
14	23	J9	J2	34	PA0-WKUP(PA0)	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, EVENTOUT	ADC123_IN0, WKUP0/TAMP_2
15	24	G7	K2	35	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, EVENTOUT	ADC123_IN1
16	25	E7	L2	36	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, EVENTOUT	ADC123_IN2

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
40	66	D1	E11	99	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDIO_D1, DCMI_D3, EVENTOUT	-
41	67	E2	E12	100	PA8	I/O	FT	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT	-
42	68	F4	D12	101	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, SAI1_SD_B, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_VBUS
43	69	E3	D11	102	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
44	70	C1	C12	103	PA11 ⁽¹⁾	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
45	71	E4	B12	104	PA12 ⁽¹⁾	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	72	D2	A12	105	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
-	73	C2	G9	106	VCAP_2	S	-	-	-	-
47	74	B1	G10	107	VSS	S	-	-	-	-
48	75	A1	F9	108	VDD	S	-	-	-	-
49	76	C3	A11	109	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
50	77	B2	A10	110	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, UART4_RTS, EVENTOUT	-

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
56	90	B5	A6	134	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, I2C3_SDA, SPI1_MISO, SPI3_MISO, SPI2_NSS/I2S2_WS, EVENTOUT	-
57	91	A6	B6	135	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, FMC_SDCKE1, DCMI_D10, EVENTOUT	-
58	92	C5	C6	136	PB6	I/O	FT	-	TIM4_CH1, HDMI_CEC, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, FMC_SDNE1, DCMI_D5, EVENTOUT	-
59	93	B6	D6	137	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, SPDIFRX_IN0, FMC_NL, DCMI_VSYNC, EVENTOUT	-
60	94	A7	D5	138	BOOT0	I	B	-	-	VPP
61	95	C6	C5	139	PB8	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, SDIO_D4, DCMI_D6, EVENTOUT	-
62	96	C7	B5	140	PB9	I/O	FT	-	TIM2_CH2, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, SAI1_FS_B, CAN1_TX, SDIO_D5, DCMI_D7, EVENTOUT	-
-	97	-	A5	141	PE0	I/O	FT	-	TIM4_ETR, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
-	98	-	A4	142	PE1	I/O	FT	-	FMC_NBL1, DCMI_D3, EVENTOUT	-

Table 11. Alternate function (continued)

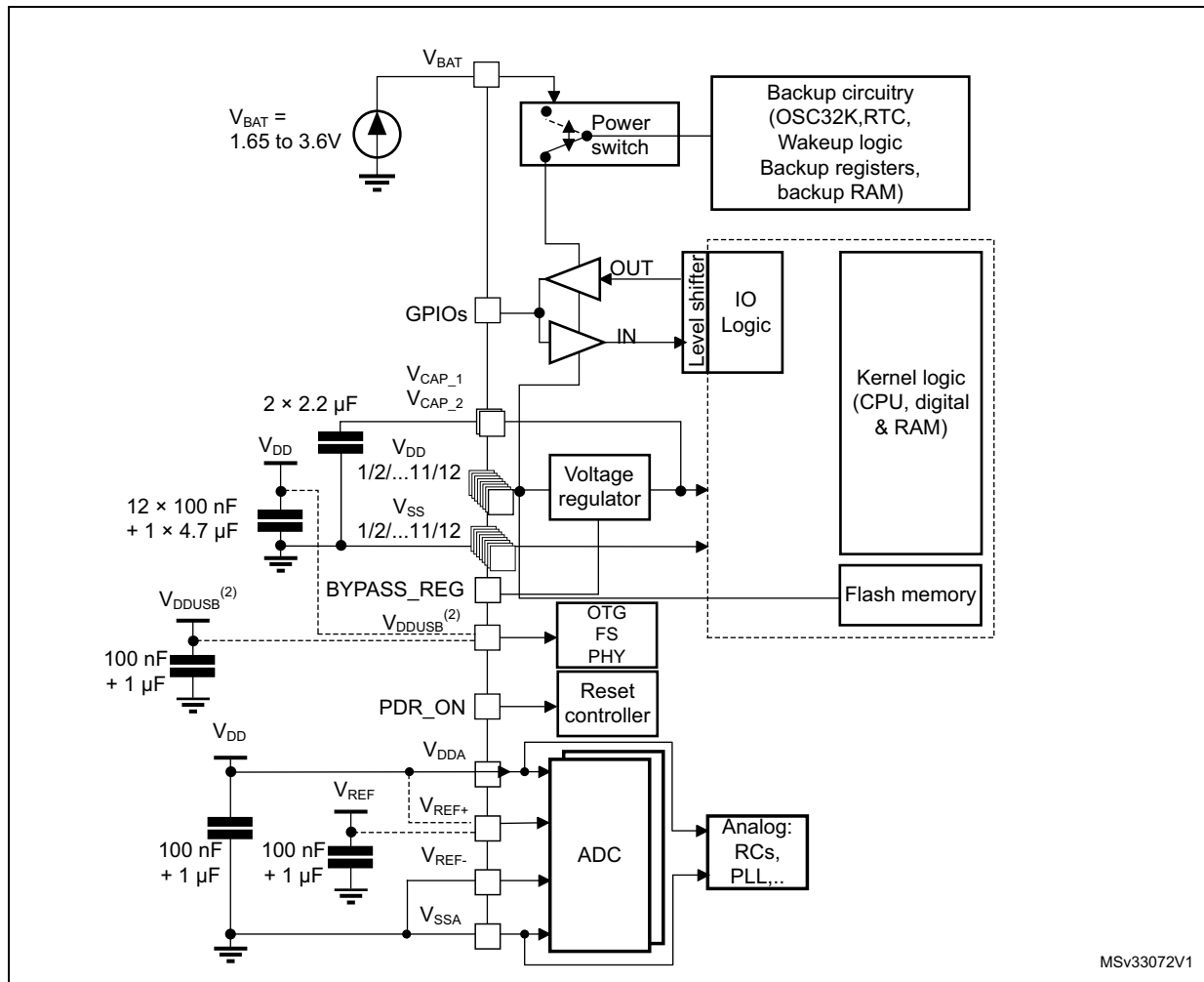
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11/ CEC	I2C1/2/3 /4/CEC	SPI1/2/3/ 4	SPI2/3/4/ SAI1	SPI2/3/ USART1/ 2/3/UART 5/SPDIFR X	SAI/ USART6/ UART4/5/ SPDIFRX	CAN1/2 TIM12/13/ 14/ QUADSPI	SAI2/ QUADSPI/ OTG2_HS/ OTG1_FS	OTG1_FS	FMC/ SDIO/ OTG2_FS	DCMI	-	SYS
Port C	PC0	-	-	-	-	-	-	SAI1_ MCLK_B	-	-	-	OTG_HS_ ULPI_STP	-	FMC_ SDNWE	-	-	EVENT OUT
	PC1	-	-	-	-	-	SPI3_MOSI /I2S3_SD	SAI1_ SD_A	SPI2_MOS I /I2S2_SD	-	-	-	-	-	-	-	EVENT OUT
	PC2	-	-	-	-	-	SPI2_MISO	-	-	-	-	OTG_HS_ ULPI_DIR	-	FMC_ SDNE0	-	-	EVENT OUT
	PC3	-	-	-	-	-	SPI2_MOSI / I2S2_SD	-	-	-	-	OTG_HS_ ULPI_NXT	-	FMC_ SDCKE0	-	-	EVENT OUT
	PC4	-	-	-	-	-	I2S1_MCK	-	-	SPDIF_ RX2	-	-	-	FMC_ SDNE0	-	-	EVENT OUT
	PC5	-	-	-	-	-	-	-	USART3_ RX	SPDIF_ RX3	-	-	-	FMC_ SDCKE0	-	-	EVENT OUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	FMPI2C1_ SCL	I2S2_MCK	-	-	USART6_T X	-	-	-	SDIO_D6	DCMI_D0	-	EVENT OUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	FMPI2C1_ SDA	SPI2_SCK/ I2S2_CK	I2S3_MCK	SPDIF_ RX1	USART6_R X	-	-	-	SDIO_D7	DCMI_D1	-	EVENT OUT
	PC8	TRACE D0	-	TIM3_CH3	TIM8_CH3	-	-	-	UART5_ RTS	USART6_C K	-	-	-	SDIO_D0	DCMI_D2	-	EVENT OUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_ SDA	I2S_CKIN	-	UART5_ CTS	-	QUADSPI_ BK1_IO0	-	-	SDIO_D1	DCMI_D3	-	EVENT OUT
	PC10	-	-	-	-	-	-	SPI3_SCK / I2S3_CK	USART3_ TX	UART4_TX	QUADSPI_ BK1_IO1	-	-	SDIO_D2	DCMI_D8	-	EVENT OUT
	PC11	-	-	-	-	-	-	SPI3_ MISO	USART3_ RX	UART4_RX	QUADSPI_ BK2_NCS	-	-	SDIO_D3	DCMI_D4	-	EVENT OUT
	PC12	-	-	-	-	I2C2_ SDA	-	SPI3_ MOSI/ I2S3_SD	USART3_ CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENT OUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 12. STM32F446xC/E register boundary addresses⁽¹⁾ (continued)

Bus	Boundary address	Peripheral
-	0x4008 0000 - 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00 - 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	
	0x4002 9400 - 0x4002 AFFF	
	0x4002 9000 - 0x4002 93FF	
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	
	0x4002 2400 - 0x4002 27FF	
	0x4002 2000 - 0x4002 23FF	
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

6.1.6 Power supply scheme

Figure 18. Power supply scheme



1. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
2. V_{DDUSB} is a dedicated independent USB power supply for the on-chip full-speed OTG PHY module and associated DP/DM GPIOs. Its value is independent from the V_{DD} and V_{DDA} values, but must be the last supply to be provided and the first to disappear. If V_{DD} is different from V_{DDUSB} and only one on-chip OTG PHY is used, the second OTG PHY GPIOs (DP/DM) are still supplied at V_{DDUSB} (3.3V).
3. V_{DDUSB} is available only on WLCSP81, UFBGA144 and LQFP144 packages. For packages where V_{DDUSB} pin is not available, it is internally connected to V_{DD} .
4. V_{CAP_2} pad is not available on LQFP64.

Caution: Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see [Table 17: Limitations depending on the operating power supply range](#)).
- Regulator ON
- The voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
 - Scale 3 for $f_{HCLK} \leq 120$ MHz
 - Scale 2 for $120 \text{ MHz} < f_{HCLK} \leq 144$ MHz
 - Scale 1 for $144 \text{ MHz} < f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 8 MHz and PLL is ON when f_{HCLK} is higher than 16 MHz.
- Flash is enabled except if explicitly mentioned as disable.
- The maximum values are obtained for $V_{DD} = 3.6$ V and a maximum ambient temperature (T_A), and the typical values for $T_A = 25$ °C and $V_{DD} = 3.3$ V unless otherwise specified.

FMPI²C characteristics

The FMPI2C characteristics are described in [Table 62](#).

Refer also to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 62. FMPI²C characteristics⁽¹⁾

-	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
f _{FMPI2CC}	F _{FMPI2CC} frequency	2	-	8	-	17 16 ⁽²⁾	-	us
t _{w(SCLL)}	SCL clock low time	4.7	-	1.3	-	0.5	-	
t _{w(SCLH)}	SCL clock high time	4.0	-	0.6	-	0.26	-	
t _{su(SDA)}	SDA setup time	0.25	-	0.10	-	0.05	-	
t _{H(SDA)}	SDA data hold time	0	-	0	-	0	-	
t _{v(SDA,ACK)}	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time	-	0.100	-	0.30	-	0.12	
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time	-	0.30	-	0.30	-	0.12	
t _{h(STA)}	Start condition hold time	4	-	0.6	-	0.26	-	
t _{su(STA)}	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
t _{su(STO)}	Stop condition setup time	4	-	0.6	-	0.26	-	
t _{w(STO:STA)}	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	pF
t _{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.09	0.05	0.09	
C _b	Capacitive load for each bus Line	-	400	-	400	-	550 ⁽³⁾	

1. Guaranteed based on test during characterization.

2. When tr(SDA,SCL)≤110ns.

3. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:

$$t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$$

$$R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$$

SAI characteristics

Unless otherwise specified, the parameters given in [Table 67](#) for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in [Table 16](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: 0.5V_{DD}

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 67. SAI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256 x 8K	256 x Fs	MHz
f_{CK}	SAI clock frequency ⁽²⁾	Master data: 32 bits	-	128 x Fs ⁽³⁾	MHz
		Slave data: 32 bits	-	128 x Fs ⁽³⁾	
$t_{V(FS)}$	FS valid time	Master mode 2.7 V ≤ V _{DD} ≤ 3.6 V	-	14	ns
		Master mode 1.71 V ≤ V _{DD} ≤ 3.6 V	-	17.5	
$t_{H(FS)}$	FS hold time	Master mode	7	-	
$t_{SU(FS)}$	FS setup time	Slave mode	1	-	
$t_{H(FS)}$	FS hold time	Slave mode	1	-	
$t_{SU(SD_A_MR)}$	Data input setup time	Master receiver	1	-	
$t_{SU(SD_B_SR)}$		Slave receiver	1	-	
$t_{H(SD_A_MR)}$	Data input hold time	Master receiver	5	-	
$t_{H(SD_B_SR)}$		Slave receiver	1	-	
$t_{V(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge 2.7 V ≤ V _{DD} ≤ 3.6 V	-	9.5	
		Slave transmitter (after enable edge 1.71 V ≤ V _{DD} ≤ 3.6 V	-	16	
$t_{H(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge	6	-	
$t_{V(SD_B_ST)}$	Data output valid time	Master transmitter (after enable edge 2.7 V ≤ V _{DD} ≤ 3.6 V	-	15	
		Master transmitter (after enable edge 1.71 V ≤ V _{DD} ≤ 3.6 V	-	18	
$t_{H(SD_B_ST)}$	Data output hold time	Master transmitter (after enable edge	7	-	

1. Guaranteed based on test during characterization.

2. 256xFs maximum corresponds to 45 MHz (APB2 xaximum frequency)

3. With Fs = 192 KHz

Table 90. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 2$	$3T_{HCLK} + 0.5$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK} - 0.5$	$2T_{HCLK}$	
$t_{w(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK} + 0.5$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	2	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	0	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 1.5$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK} + 1$	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. $C_L = 30$ pF.
2. Guaranteed based on test during characterization.

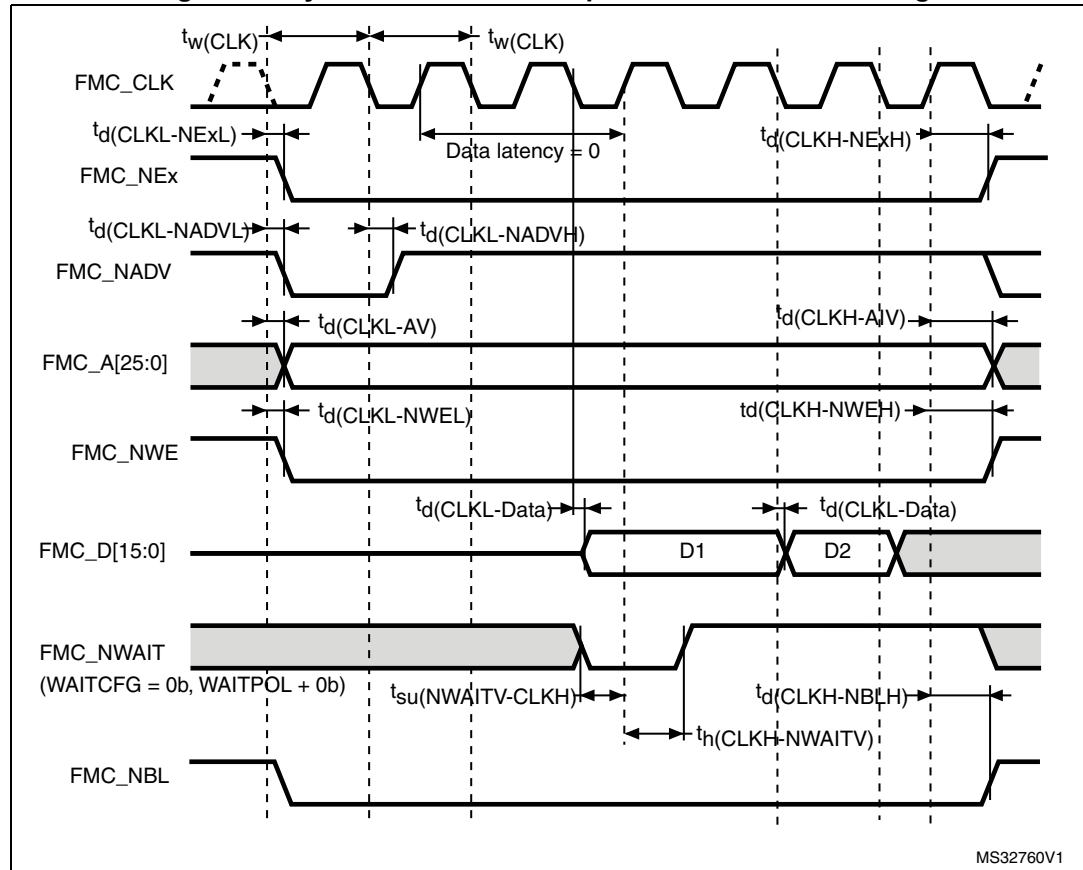
Table 91. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK} - 1$	$8T_{HCLK} + 2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} + 1.5$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 1$	-	

1. $C_L = 30$ pF.
2. Guaranteed based on test during characterization.

1. $C_L = 30 \text{ pF}$.
2. Guaranteed based on test during characterization.

Figure 57. Synchronous non-multiplexed PSRAM write timings

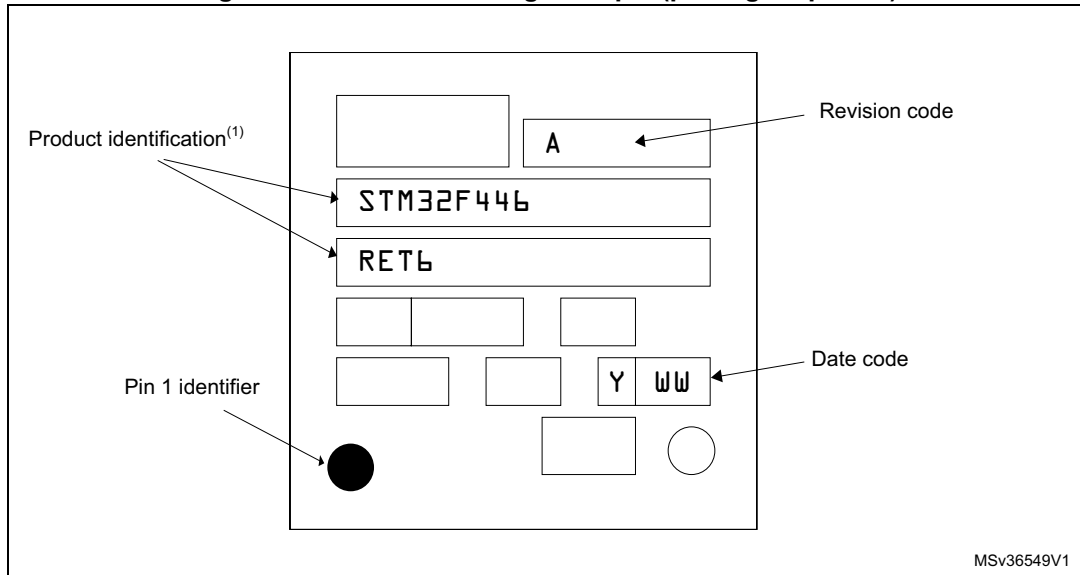


Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 69. LQFP64 marking example (package top view)

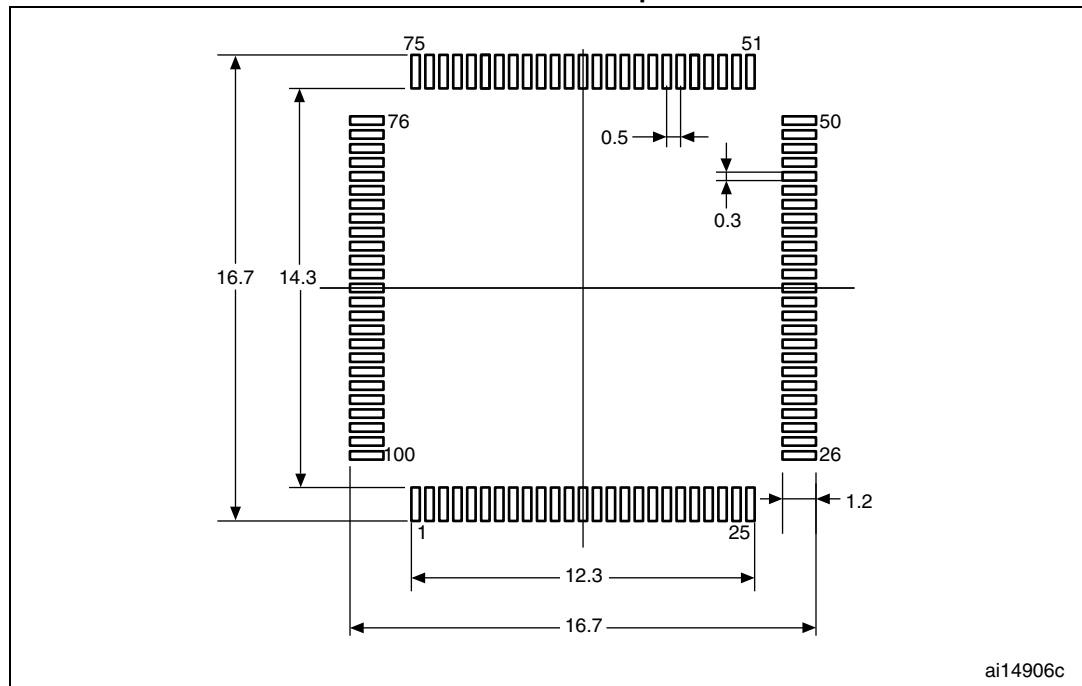


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 109. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 71. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

1. Dimensions are expressed in millimeters.

7.7 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 117. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm	46	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	42	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	33	
	Thermal resistance junction-ambient UFBGA144 - 7 × 7 mm / 0.5 mm pitch	51	
	Thermal resistance junction-ambient UFBGA144 - 10 × 10 mm / 0.8 mm pitch	48	
	Thermal resistance junction-ambient WLCSP81	48	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.