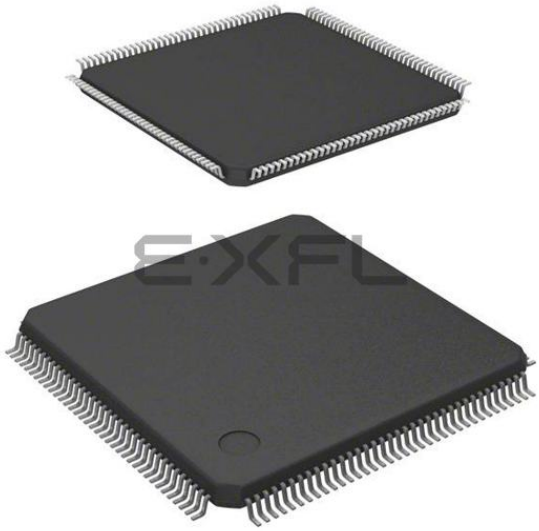

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446zct6

3.21.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.21.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.21.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.22 Inter-integrated circuit interface (I^2C)

Four I²C bus interfaces can operate in multimaster and slave modes. Three I²C can support the standard (up to 100 KHz) and fast (up to 400 KHz) modes.
One I²C can support the standard (up to 100 KHz), fast (up to 400 KHz) and fast mode plus (up to 1MHz) modes.

They (all I²C) support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave).
A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 7*).

Table 7. Comparison of I2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.25 HDMI (high-definition multimedia interface) consumer electronics control (CEC)

The devices embeds a HDMI-CEC controller that provides hardware support of consumer electronics control (CEC) (Appendix supplement 1 to the HDMI standard).
This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead.

3.26 Inter-integrated sound (I^2S)

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

3.27 SPDIF-RX Receiver Interface (SPDIFRX)

The SPDIF-RX peripheral, is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main features of the SPDIF-RX are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIF-RX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream.

The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIF-RX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.41 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F446xx through a small number of ETM pins to an external hardware trace port analyser (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	-	-	H6	61	VSS	S	-	-	-	-
-	-	-	G6	62	VDD	S	-	-	-	-
-	41	J4	J7	63	PE10	I/O	FT	-	TIM1_CH2N, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-
-	42	-	H8	64	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, SAI2_SD_B, FMC_D8, EVENTOUT	-
-	43	-	J8	65	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_D9, EVENTOUT	-
-	44	-	K8	66	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_D10, EVENTOUT	-
-	45	-	L8	67	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11, EVENTOUT	-
-	46	-	M8	68	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, EVENTOUT	-
29	47	H4	M9	69	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, SAI1_SCK_A, USART3_TX, OTG_HS_ULPI_D3, EVENTOUT	-
-	-	-	M10	70	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, USART3_RX, SAI2_SD_A, EVENTOUT	-
30	48	J3	H7	71	VCAP_1	S	-	-	-	-
31	49	H3	-	-	VSS	S	-	-	-	-
32	50	J2	G7	72	VDD	S	-	-	-	-
33	51	G4	M11	73	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SAI1_SCK_B, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, OTG_HS_ID, EVENTOUT	-

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	87	B4	A8	122	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, EVENTOUT	-
-	88	A4	A9	123	PD7	I/O	FT	-	USART2_CK, SPDIFRX_IN0, FMC_NE1, EVENTOUT	-
-	-	-	E8	124	PG9	I/O	FT	-	SPDIFRX_IN3, USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE3, DCMI_VSYNC, EVENTOUT	-
-	-	-	D8	125	PG10	I/O	FT	-	SAI2_SD_B, FMC_NE3, DCMI_D2, EVENTOUT	-
-	-	-	C8	126	PG11	I/O	FT	-	SPI4_SCK, SPDIFRX_IN0, DCMI_D3, EVENTOUT	-
-	-	-	B8	127	PG12	I/O	FT	-	SPI4_MISO, SPDIFRX_IN1, USART6_RTS, FMC_NE4, EVENTOUT	-
-	-	-	D7	128	PG13	I/O	FT	-	TRACED2, SPI4_MOSI, USART6_CTS, FMC_A24, EVENTOUT	-
-	-	-	C7	129	PG14	I/O	FT	-	TRACED3, SPI4_NSS, USART6_TX, QUADSPI_BK2_IO3, FMC_A25, EVENTOUT	-
-	-	-	-	130	VSS	S	-	-	-	-
-	-	-	F6	131	VDD	S	-	-	-	-
-	-	-	B7	132	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
55	89	A5	A7	133	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, I2C2_SDA, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, EVENTOUT	-

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
63	99	B7	E6	-	VSS	S	-	-	-	-
-	-	B8	E5	143	PDR_ON	S	-	-	-	-
64	100	A8	F5	144	VDD	S	-	-	-	-

1. PA11, PA12, PB14 and PB15 I/Os are supplied by VDDUSB

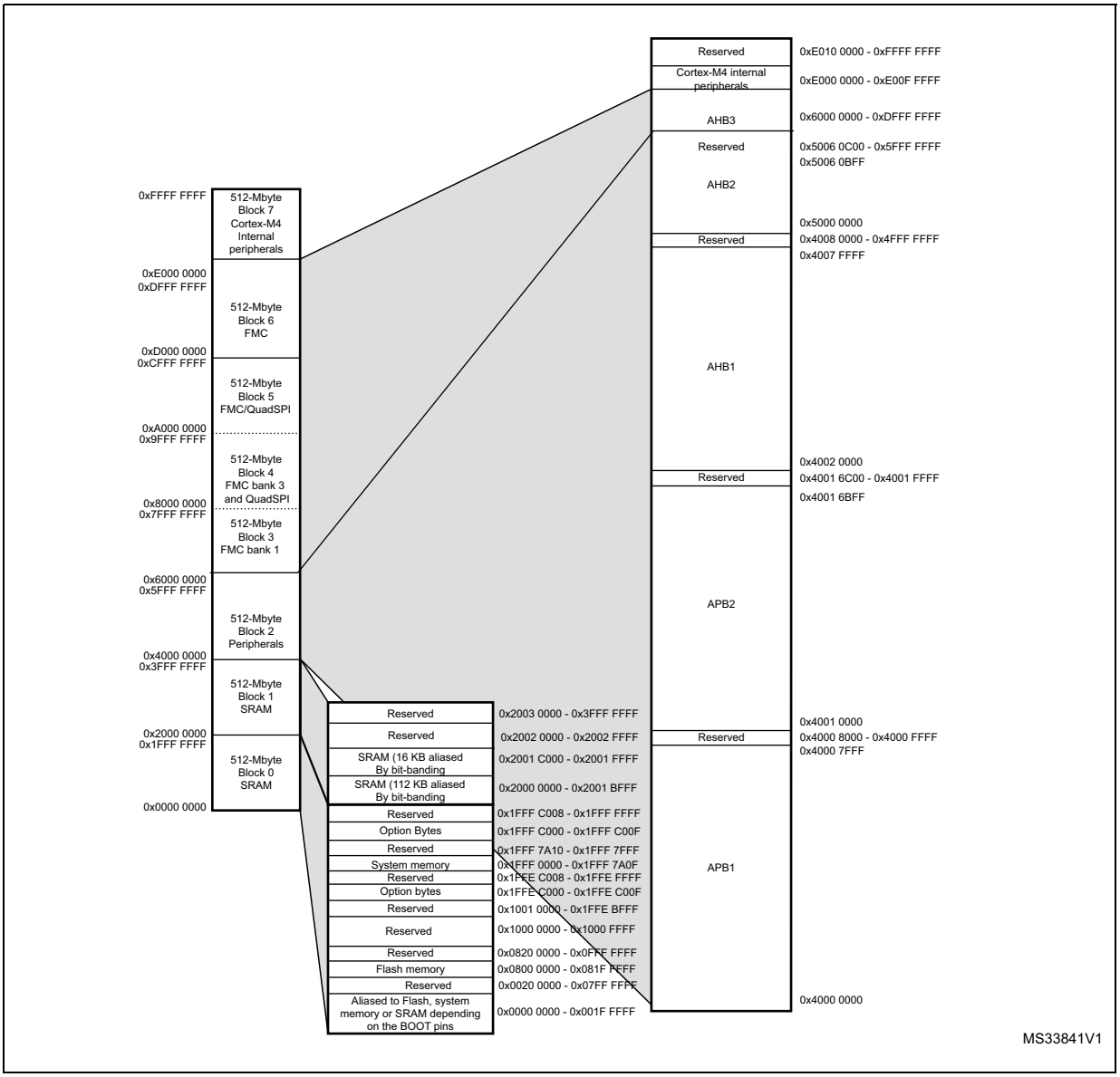
Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4	SPI2/3/4/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI/USART6/UART4/5/SPDIFRX	CAN1/2 TIM12/13/14/QUADSPI	SAI2/QUADSPI/OTG2_HS/OTG1_FS	OTG1_FS	FMC/SDIO/OTG2_FS	DCMI	-	SYS
Port D	PD0	-	-	-	-	-	SPI4_MISO	SPI3_MOSI/I2S3_SD	-	-	CAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	SPI2_NSS/I2S2_WS	-	CAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVENTOUT
	PD3	TRACED1	-	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CTS	-	QUADSPI_CLK	-	-	FMC_CLK	DCMI_D5	-	EVENTOUT
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	SPI3_MOSI/I2S3_SD	SAI1_SD_A	USART2_RX	-	-	-	-	FMC_NWAIT	DCMI_D10	-	EVENTOUT
	PD7	-	-	-	-	-	-	-	USART2_CK	SPDIF_RX0	-	-	-	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	SPDIF_RX1	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	-	EVENTOUT
	PD11	-	-	-	-	FMPI2C1_SMBA	-	-	USART3_CTS	-	QUADSPI_BK1_IO0	SAI2_SD_A	-	FMC_A16	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	-	FMPI2C1_SCL	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	SAI2_FS_A	-	FMC_A17	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	-	FMPI2C1_SDA	-	-	-	-	QUADSPI_BK1_IO3	SAI2_SCK_A	-	FMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	FMPI2C1_SCL	-	-	-	SAI2_SCK_A	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	FMPI2C1_SDA	-	-	-	-	-	-	-	FMC_D1	-	-	EVENTOUT

5 Memory mapping

The memory map is shown in *Figure 15*

Figure 15. Memory map



6.3 Operating conditions

6.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF		0	-	120	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-	144	
			Over-drive ON		-	168	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-	168	
			Over-drive ON		-	180	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		0	-	42	
		Over-drive ON		0	-	45	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		0	-	84	
		Over-drive ON		0	-	90	

Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	External clock, PLL ON, all peripherals enabled(2)(3)	180	81	89.0	110.0	120.0	mA
			168(4)	74	80.2	105.7	112.0	
			150	69	74.9	99.5	105.6	
			144(4)	63	69.3	92.4	98.1	
			120	51	56.3	76.1	81.1	
			90	40	45.32	63.19	67.63	
			60	28	33.1	48.7	52.6	
			30	16	20.8	34.0	37.4	
			25	13	18.4	31.2	34.5	
		External clock, PLL ON, all Peripherals disabled(2)(3)	16	8	13.8	25.0	28.2	
			8	5	10.8	21.1	24.2	
			4	3.0	9.1	19.0	22.0	
			2	2.1	8.1	17.9	20.9	
			180	41	47.0	69.0	79.0	
			168	38	43.2	61.9	67.1	
			150	37	41.8	60.3	65.4	
			144(4)	34	39.3	56.9	61.6	
			120	29	34.3	50.2	54.4	
		HSI, PLL OFF, all peripherals disabled(3)	90	24	28.8	43.6	47.5	
			60	17	22.0	35.6	39.2	
			30	10	14.8	27.0	30.1	
			25	8	13.51	25.36	28.47	
		HSI, PLL OFF, all Peripherals disabled(3)	16	5	11.1	21.8	24.9	
			8	3	9.5	19.4	22.5	
			4	2.3	8.35	18.12	21.17	
			2	1.8	7.78	17.42	20.51	

1. Guaranteed based on test during characterization unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. Overdrive OFF

Table 32. Typical current consumption in Sleep mode, regulator ON, V_{DD}=1.7 V(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	All Peripherals enabled Flash on	168	43.7	47.5	66.5	79.3	mA
			150	39.2	42.7	60.7	73.3	
			144	35.7	38.8	55.3	66.9	
			120	26.5	28.6	41.8	51.6	
			90	20.0	21.91	33.85	43.20	
			60	13.6	15.2	25.8	34.9	
			30	7.4	8.5	18.4	27.0	
			25	6.3	7.5	16.9	25.5	
		All Peripherals disabled, flash on	168	7.3	8.6	21.2	31.9	
			150	6.6	7.94	20.4	31.0	
			144	6.0	7.3	18.6	28.5	
			120	4.6	5.5	14.9	23.4	
			90	3.6	4.6	13.6	22.1	
			60	2.6	3.4	12.5	20.8	
			30	1.8	2.7	11.3	19.7	
			25	1.6	2.49	11.09	19.42	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ Appli)			Unit
		Scale 1 + OverDrive	Scale 2	Scale 3	
APB2	TIM1	17.51	16.28	14.43	µA/MHz
	TIM8	18.40	17.10	15.22	
	USART1	4.53	4.21	3.72	
	USART6	4.53	4.21	3.72	
	ADC1	4.69	4.35	3.85	
	ADC2	4.70	4.35	3.87	
	ADC3	4.66	4.31	3.82	
	SDIO	9.06	8.38	7.47	
	SPI1	1.97	1.89	1.67	
	SPI4	1.88	1.75	1.57	
	SYSCFG	1.51	1.40	1.23	
	TIM9	8.17	7.64	6.77	
	TIM10	5.07	4.75	4.22	
	TIM11	5.37	5.06	4.50	
	SAI1	3.89	3.64	3.17	
	SAI2	3.74	3.49	3.10	
Bus Matrix		8.15	8.10	7.13	

1. N = Number of strean enable (1..8)
2. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.

6.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 36* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 49. Flash memory programming with V_{PP} (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 50. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
-	-		Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	Kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed based on test during characterization.
2. Cycling performed over the whole temperature range.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 51*. They are based on the EMS levels and classes defined in application note AN1709.

Table 57. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+ 8mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 14*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 14* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 32* and *Table 58*, respectively.

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 58. I/O AC characteristics(1)(2)

OSPEEDRy[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	4	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns

The I^2C characteristics are described in *Table 61*. Refer also to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 61. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(4)	
$t_{v(SDA, ACK)}$	Data, ACK valid time	-	3.45	-	0.9	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.09(5)	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed based on test during characterization.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I^2C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

Table 63. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCKH)}$ / $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI presc = 2	T_{PCLK} - 1.5	T_{PCLK}	T_{PCLK} + 1.5	ns
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4T_{PCLK}$	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$			
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	
$t_{v(SO)}$	Data output valid/hold time	Slave mode (after enable edge), 2.7V ≤ V_{DD} ≤ 3.6V	-	7.5	22	
		Slave mode (after enable edge), 1.7 V ≤ V_{DD} ≤ 3.6 V	-	7.5	10.5	
$t_{h(SO)}$	Data output valid/hold time	Slave mode (after enable edge)	5	-	-	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	1.5	5	
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	0	-	-	

1. Guaranteed based on test during characterization.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.

Figure 36. SPI timing diagram - slave mode and CPHA = 0

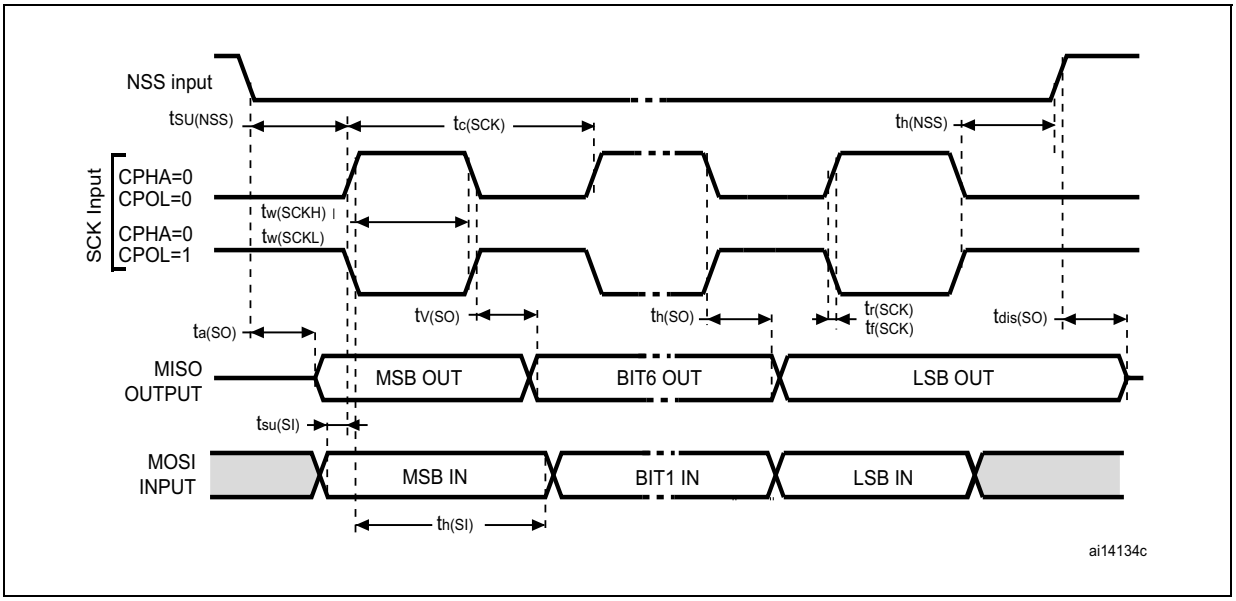


Figure 41. SAI master timing waveforms

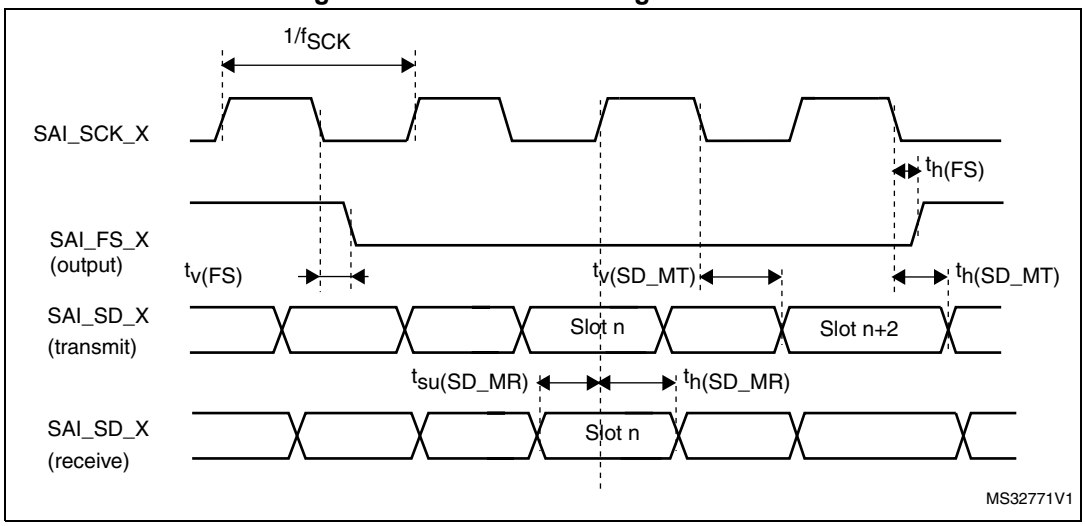
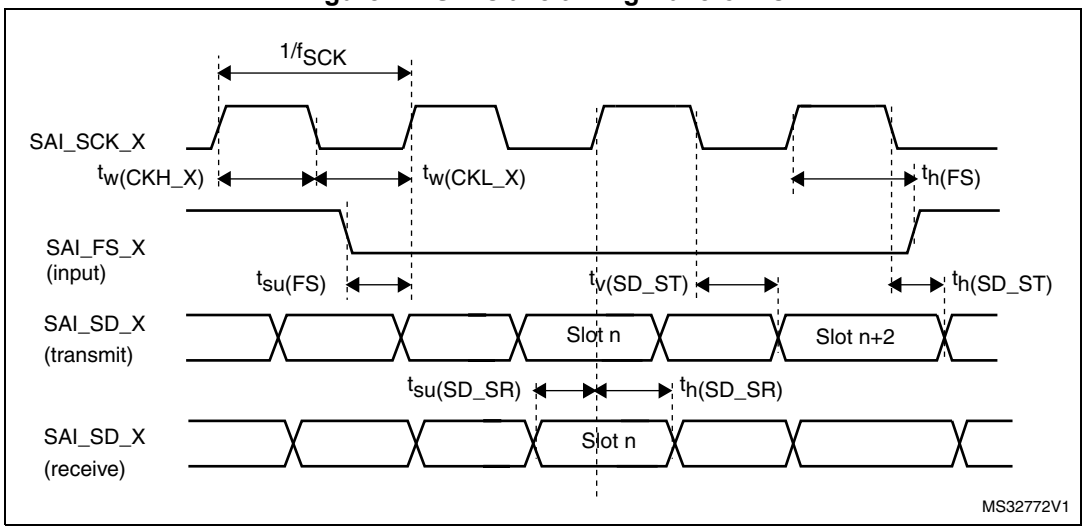


Figure 42. SAI slave timing waveforms



USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 68. USB OTG full speed startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG full speed transceiver startup time	1	µs

1. Guaranteed by design.

6.3.26 FMC characteristics

Unless otherwise specified, the parameters given in *Table 86* to *Table 93* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitance load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 50 through *Figure 53* represent asynchronous waveforms and *Table 86* through *Table 93* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 66. SD default mode

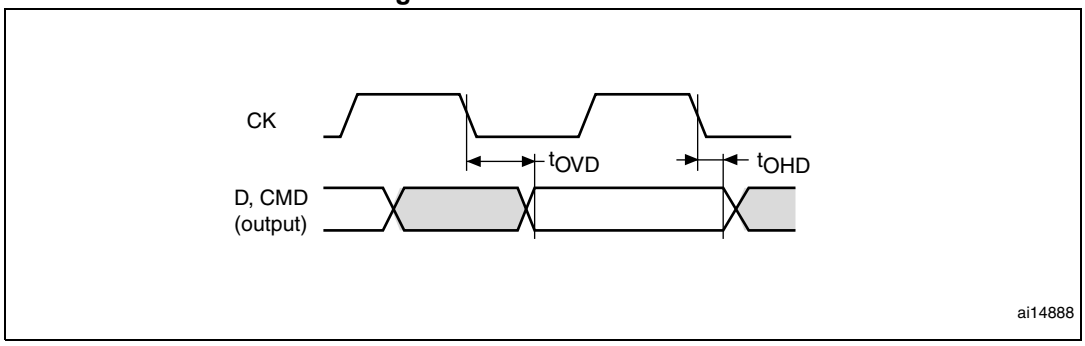


Table 105. Dynamic characteristics: SD / MMC characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50MHz	9.5	10.5	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50MHz	1	-	-	ns
t_{IH}	Input hold time HS	fpp =50MHz	4.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50MHz	-	12.5	13	ns
t_{OH}	Output hold time HS	fpp =50MHz	11	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25MHz	2.5	-	-	ns
t_{IHD}	Input hold time SD	fpp =25MHz	5.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =24MHz	-	3.5	4	ns
t_{OHD}	Output hold default time SD	fpp =24MHz	2	-	-	

1. Guaranteed based on test during characterization.
2. V_{DD} = 2.7 to 3.6 V.