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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446zej6

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1 Introduction

This document provides the description of the STM32F446xC/E products.

The STM32F446xC/E document should be read in conjunction with the STM32F4xx reference manual.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214), available from the *www.st.com*.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode

    The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
  - In Stop modes

    The MR can be configured in two ways during stop mode:

    MR operates in normal mode (default mode of MR in stop mode)

    MR operates in under-drive mode (reduced leakage mode).
- LPR is used in the Stop modes:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during stop mode:
  - LPR operates in normal mode (default mode when LPR is ON)
  - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

3.17.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

3.23 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. USART feature comparison(1)

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	X	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	X	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)

1. X = feature supported.

3.24 Serial peripheral interface (SPI)

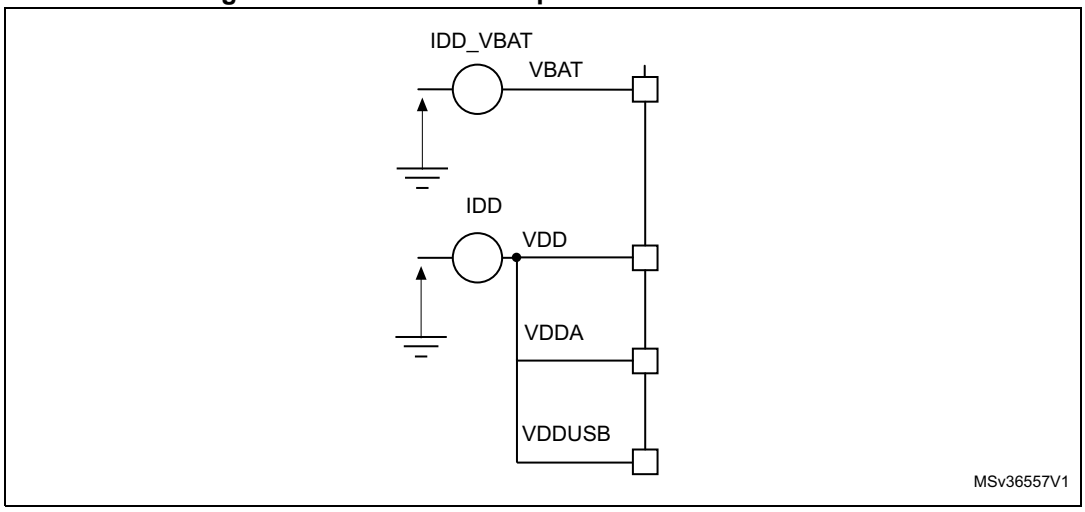
The devices feature up to four SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, and SPI4 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4	SPI2/3/4/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI/USART6/UART4/5/SPDIFRX	CAN1/2 TIM12/13/14/QUADSPI	SAI2/QUADSPI/OTG2_HS/OTG1_FS	OTG1_FS	FMC/SDIO/OTG2_FS	DCMI	-	SYS
Port C	PC0	-	-	-	-	-	-	SAI1_MCLK_B	-	-	-	OTG_HS_ULPI_STP	-	FMC_SDNWE	-	-	EVENTOUT
	PC1	-	-	-	-	-	SPI3_MOSI/I2S3_SD	SAI1_SD_A	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	-	-	-	-	OTG_HS_ULPI_DIR	-	FMC_SDNE0	-	-	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI/I2S2_SD	-	-	-	-	OTG_HS_ULPI_NXT	-	FMC_SDCKE0	-	-	EVENTOUT
	PC4	-	-	-	-	-	I2S1_MCK	-	-	SPDIF_RX2	-	-	-	FMC_SDNE0	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	USART3_RX	SPDIF_RX3	-	-	-	FMC_SDCKE0	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	FMPI2C1_SCL	I2S2_MCK	-	-	USART6_TX	-	-	-	SDIO_D6	DCMI_D0	-	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	FMPI2C1_SDA	SPI2_SCK/I2S2_CK	I2S3_MCK	SPDIF_RX1	USART6_RX	-	-	-	SDIO_D7	DCMI_D1	-	EVENTOUT
	PC8	TRACED0	-	TIM3_CH3	TIM8_CH3	-	-	-	UART5_RTS	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	UART5_CTS	-	QUADSPI_BK1_IO0	-	-	SDIO_D1	DCMI_D3	-	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	QUADSPI_BK1_IO1	-	-	SDIO_D2	DCMI_D8	-	EVENTOUT
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	-	-	SDIO_D3	DCMI_D4	-	EVENTOUT
	PC12	-	-	-	-	I2C2_SDA	-	SPI3_MOSI/I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

6.1.7 Current consumption measurement

Figure 19. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics*, and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD}, V_{DDUSB} and V_{BAT})(1)	–0.3	4.0	V
V_{IN}	Input voltage on FT & FTf pins(2)	V_{SS}–0.3	V_{DD}+4.0	
	Input voltage on TTa pins	V_{SS}–0.3	4.0	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.15: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 14* for the values of the maximum allowed injected current.

Table 21. reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed based on test during characterization.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 22*. They are sbject to general operating conditions for T_A.

Table 22. Over-drive switching characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	µs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed based on test during characterization.

6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 19: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 17: Limitations depending on the operating power supply range*).
- Regulator ON
- The voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 120$ MHz
  - Scale 2 for 120 MHz < $f_{HCLK} \leq 144$ MHz
  - Scale 1 for 144 MHz < $f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 8 MHz and PLL is ON when f_{HCLK} is higher than 16 MHz.
- Flash is enabled except if explicitly mentioned as disable.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 30. Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), VDD=1.7 V(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode from V_{DD} supply	All Peripherals enabled	168	65.11	70.0	79.7	90.0	mA
			150	58.31	62.8	73.4	79.9	
			144	53.14	57.1	69.9	75.3	
			120	39.58	47.2	60.7	71.4	
			90	29.99	34.70	45.23	49.34	
			60	20.37	25.2	35.2	38.2	
			30	11.37	12.9	28.4	33.2	
			25	9.65	10.9	17.8	24.3	
		All Peripherals disabled	168	29.74	32.43	42.4	48.5	
			150	25.81	29.12	39.4	43.8	
			144	24.57	26.61	36.0	41.9	
			120	17.69	22.09	32.9	40.8	
			90	13.58	15.92	30.0	36.5	
			60	9.41	11.05	24.4	30.2	
			30	5.44	6.64	15.0	22.0	
			25	4.73	5.72	12.57	19.06	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

Table 35. Peripheral current consumption

Peripheral		I_{DD}(Typ Appli)			Unit
		Scale 1 + OverDrive	Scale 2	Scale 3	
AHB1	GPIOA	2.29	2.14	1.89	µA/MHz
	GPIOB	2.29	2.13	1.89	
	GPIOC	2.33	2.17	1.93	
	GPIOD	2.34	2.19	1.94	
	GPIOE	2.39	2.19	1.93	
	GPIOF	2.31	2.14	1.91	
	GPIOG	2.36	2.19	1.94	
	GPIOH	2.13	1.98	1.75	
	CRC	0.53	0.51	0.46	
	BKPSRAM	0.76	0.72	0.65	
	DMA1(1)	2.39N + 4.13	2.23N+3.56	1.97N+3.51	
	DMA2(1)	2.39N + 4.45	2.19N+3.72	2.00N+3.66	
	OTG_HS+ULPI	45.45	42.08	37.28	
AHB2	DCMI	3.74	3.42	3.01	µA/MHz
	OTGFS	30.04	27.88	24.69	
AHB3	FMC	16.15	15.01	13.33	µA/MHz
	QSPI	16.78	15.60	13.84	

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ Appli)			Unit
		Scale 1 + OverDrive	Scale 2	Scale 3	
APB1	TIM2	18.18	16.92	15.07	µA/MHz
	TIM3	14.49	13.47	12.00	
	TIM4	15.18	14.11	12.50	
	TIM5	16.91	15.69	14.07	
	TIM6	2.69	2.47	2.20	
	TIM7	2.56	2.44	2.17	
	TIM12	7.07	6.56	5.83	
	TIM13	4.96	4.64	4.07	
	TIM14	5.09	4.72	4.27	
	WWDG	1.07	1.00	0.93	
	SPI2(2)	1.89	1.78	1.57	
	SPI3(2)	1.93	1.81	1.67	
	SPDIFRX	6.91	6.44	5.80	
	USART2	4.20	3.83	3.40	
	USART3	4.22	3.94	3.50	
	UART4	4.13	3.89	3.40	
	UART5	4.04	3.78	3.33	
	I2C1	3.98	3.69	3.33	
	I2C2	3.91	3.61	3.17	
	I2C3	3.76	3.53	3.13	
	FMPI2C1	5.51	5.19	4.57	
	CAN1	6.58	6.14	5.43	
	CAN2	5.91	5.56	4.90	
	CEC	0.71	0.69	0.60	
	DAC	2.96	2.72	2.40	

The I^2C characteristics are described in *Table 61*. Refer also to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 61. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(4)	
$t_{v(SDA, ACK)}$	Data, ACK valid time	-	3.45	-	0.9	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.09(5)	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed based on test during characterization.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I^2C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

FMPI^{2}C characteristics

The FMPI2C characteristics are described in *Table 62*.

Refer also to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 62. FMPI^{2}C characteristics(1)

-	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
$f_{FMPI2CC}$	$F_{MPI2CCLK}$ frequency	2	-	8	-	17 16(2)	-	us
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	
$t_{su(SDA)}$	SDA setup time	0.25	-	0.10	-	0.05	-	
$t_{H(SDA)}$	SDA data hold time	0	-	0	-	0	-	
$t_{v(SDA,ACK)}$	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	0.100	-	0.30	-	0.12	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	0.30	-	0.30	-	0.12	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	0.26	-	
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	0.26	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.09	0.05	0.09	
C_b	Capacitive load for each bus Line	-	400	-	400	-	550(3)	pF

1. Guaranteed based on test during characterization.
2. When tr(SDA,SCL)<=110ns.
3. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:
   $t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$
   $R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

Table 65. QSPI dynamic characteristics in DDR Mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	QSPI clock high and low	-	$(T_{(CK)} / 2) - 2$	-	$T_{(CK)} / 2$	ns
$t_{w(CKL)}$			$T_{(CK)} / 2$	-	$(T_{(CK)} / 2) + 2$	
$t_{s(IN)}$	Data input setup time	-	0	-	-	
$t_{h(IN)}$	Data input hold time	-	5.5	-	-	
$t_{v(OUT)}$	Data output valid time	2.7V <VDD< 3.6V	-	5.5	6.5	
		1.71V <VDD< 3.6V	-	8	9.5	
$t_{h(OUT)}$	Data output hold time	-	3.5	-	-	

1. Guaranteed based on test during characterization.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 66* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

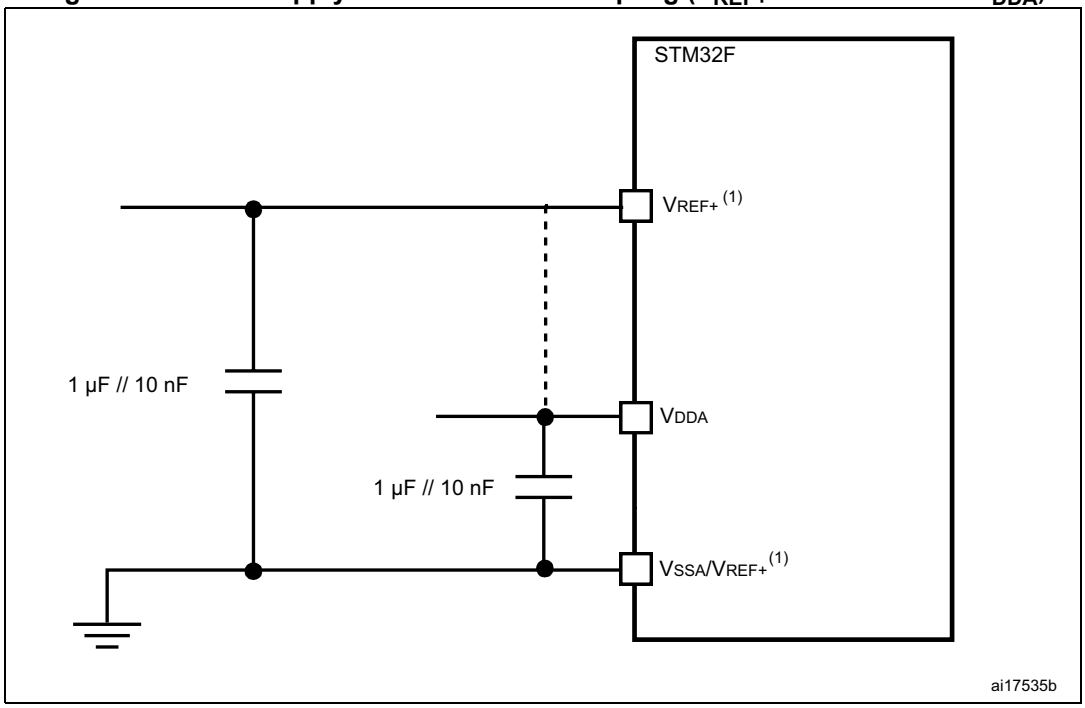
Table 66. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256 x Fs(2)	MHz
f_{CK}	I2S clock frequency	Master data	-	64 x Fs	MHz
		Slave data	-	64 x Fs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 47* or *Figure 48*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 47. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA144. V_{REF+} is also available on LQFP100, LQFP144, and WLCSP81. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}$ - 0.5	$8T_{HCLK}$ + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}$ - 0.5	$6T_{HCLK}$ + 1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}$ - 0.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$ + 2	-	

1. C_L = 30 pF.
2. Guaranteed based on test during characterization.

Figure 52. Asynchronous multiplexed PSRAM/NOR read waveforms

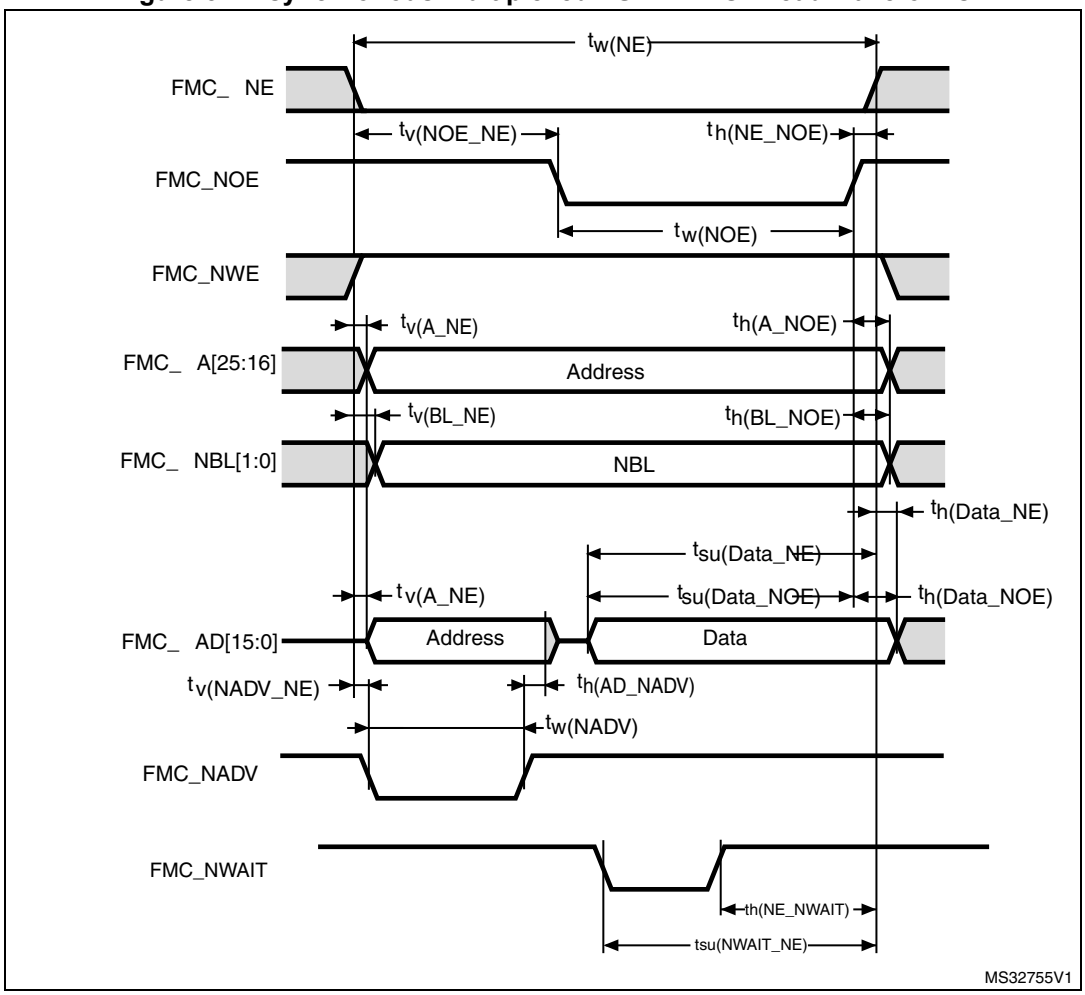
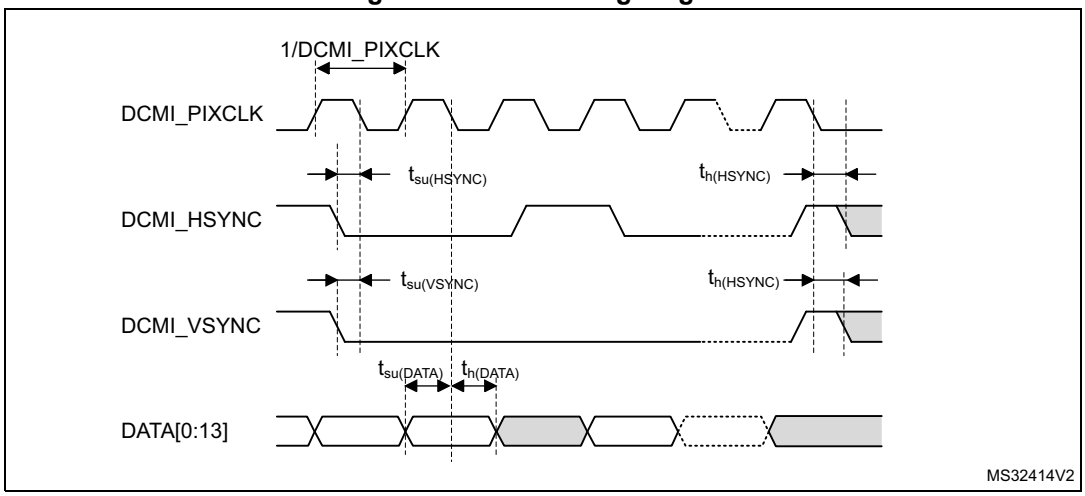


Figure 64. DCMI timing diagram



6.3.28 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 105* for the SDIO are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output characteristics.

Figure 65. SDIO high-speed mode

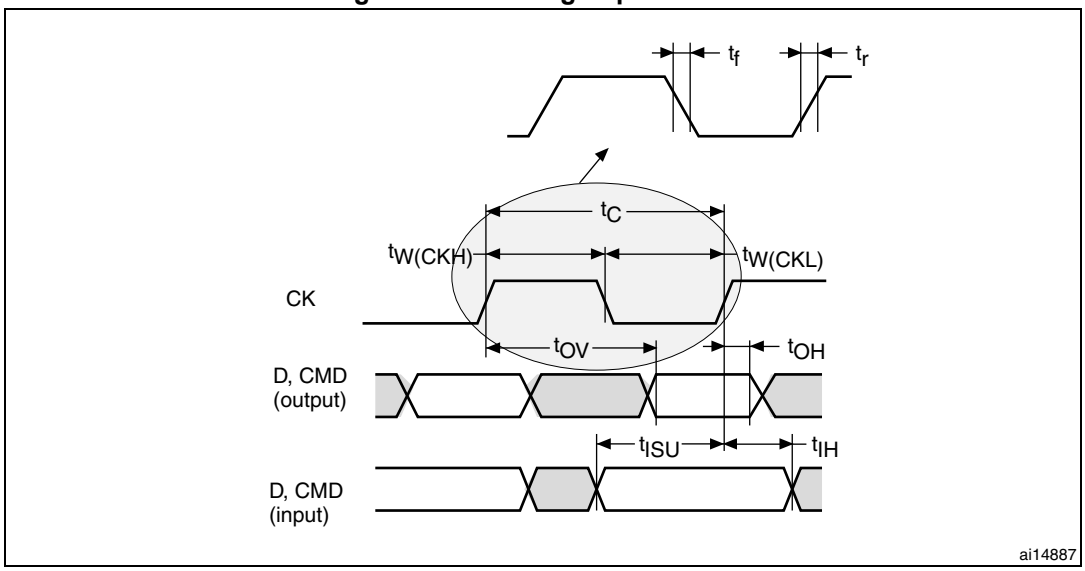


Table 111. UFBGA144 - 144-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 77. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

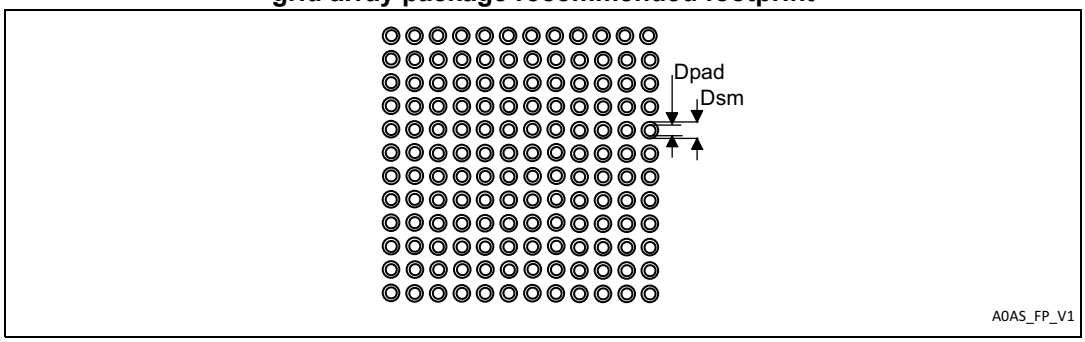


Table 112. UFBGA144 recommended PCB design rules (0.50 mm pitch BGA)

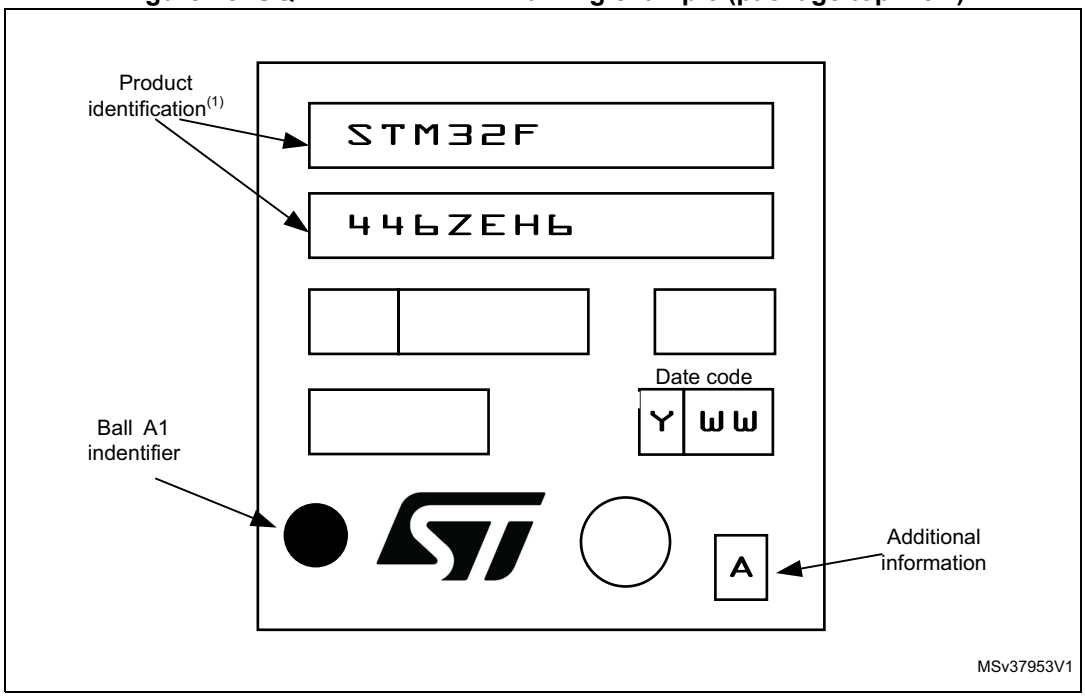
Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

Device marking for UFBGA144 7 x 7 mm package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 78. UQFP144 7 x 7 mm marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.