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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446zej6tr

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3.11 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 91 maskable interrupt channels plus the 16 interrupt lines of the Cortex[®]-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.12 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.13 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 180 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 180 MHz while the maximum frequency of the high-speed APB domains is 90 MHz. The maximum allowed frequency of the low-speed APB domain is 45 MHz.

The devices embed a dedicated PLL (PLL12S) and PLLSAI which allows to achieve audio class performance. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

Note: When the microcontroller is supplied from V_{BAT} , external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is not connected to V_{DD} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD} .

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.25 HDMI (high-definition multimedia interface) consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support of consumer electronics control (CEC) (Appendix supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead.

3.26 Inter-integrated sound (I²S)

Three standard I²S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

3.27 SPDIF-RX Receiver Interface (SPDIFRX)

The SPDIF-RX peripheral, is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main features of the SPDIF-RX are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIF-RX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream.

The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIF-RX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.41 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F446xx through a small number of ETM pins to an external hardware trace port analyser (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
40	66	D1	E11	99	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDIO_D1, DCMI_D3, EVENTOUT	-
41	67	E2	E12	100	PA8	I/O	FT	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT	-
42	68	F4	D12	101	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, SAI1_SD_B, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_VBUS
43	69	E3	D11	102	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
44	70	C1	C12	103	PA11 ⁽¹⁾	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
45	71	E4	B12	104	PA12 ⁽¹⁾	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	72	D2	A12	105	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
-	73	C2	G9	106	VCAP_2	S	-	-	-	-
47	74	B1	G10	107	VSS	S	-	-	-	-
48	75	A1	F9	108	VDD	S	-	-	-	-
49	76	C3	A11	109	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
50	77	B2	A10	110	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, UART4_RTS, EVENTOUT	-

Table 11. Alternate function

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11/ CEC	I2C1/2/3 /4/CEC	SPI1/2/3/ 4	SPI2/3/4/ SAI1	SPI2/3/ USART1/ 2/3/UART 5/SPDIFR X	SAI/ USART6/ UART4/5/ SPDIFRX	CAN1/2 TIM12/13/ 14/ QUADSPI	SAI2/ QUADSPI/ OTG2_HS/ OTG1_FS	OTG1_FS	FMC/ SDIO/ OTG2_FS	DCMI	-	SYS
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_ CTS	UART4_ TX	-	-	-	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_ RTS	UART4_ RX	QUADSPI_ BK1_IO3	SAI2_ MCLK_B	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_ TX	SAI2_ SCK_B	-	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	SAI1_ FS_A	USART2_ RX	-	-	OTG_HS_ ULPI_D0	-	-	-	-	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	USART2_ CK	-	-	-	-	OTG_HS_ SOF	DCMI_ HSYNC	-	EVENT OUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	TIM8_ CH1N	-	SPI1_SCK/ I2S1_CK	-	-	-	-	OTG_HS_ ULPI_CK	-	-	-	-	EVENT OUT
	PA6	-	TIM1_ BKIN	TIM3_CH1	TIM8_ BKIN	-	SPI1_MISO	I2S2_ MCK	-	-	TIM13_CH1	-	-	-	DCMI_ PIXCLK	-	EVENT OUT
	PA7	-	TIM1_ CH1N	TIM3_CH2	TIM8_ CH1N	-	SPI1_MOSI/ I2S1_SD	-	-	-	TIM14_CH1	-	-	FMC_ SDNWE	-	-	EVENT OUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_ SCL	-	-	USART1_ CK	-	-	OTG_FS_ SOF	-	-	-	-	EVENT OUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	SPI2_SCK/ I2S2_CK	SAI1_ SD_B	USART1_ TX	-	-	-	-	-	DCMI_D0	-	EVENT OUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_ RX	-	-	OTG_FS_ ID	-	-	DCMI_D1	-	EVENT OUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_ CTS	-	CAN1_RX	OTG_FS_ DM	-	-	-	-	EVENT OUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_ RTS	SAI2_ FS_B	CAN1_TX	OTG_FS_ DP	-	-	-	-	EVENT OUT
	PA13	JTMS- SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK- SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-	HDMI_ CEC	SPI1_NSS/ I2S1_WS	SPI3_ NSS/ I2S3_WS	-	UART4_RT S	-	-	-	-	-	-	EVENT OUT



Table 11. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11/ CEC	I2C1/2/3 /4/CEC	SPI1/2/3/ 4	SPI2/3/4/ SAI1	SPI2/3/ USART1/ 2/3/UART 5/SPDIFR X	SAI/ USART6/ UART4/5/ SPDIFRX	CAN1/2 TIM12/13/ 14/ QUADSPI	SAI2/ QUADSPI/ OTG2_HS/ OTG1_FS	OTG1_FS	FMC/ SDIO/ OTG2_FS	DCMI	-	SYS
Port F	PF0	-	-	-	-	I2C2_ SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENT OUT
	PF1	-	-	-	-	I2C2_ SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENT OUT
	PF2	-	-	-	-	I2C2_ SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENT OUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENT OUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENT OUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENT OUT
	PF6	-	-	-	TIM10_ CH1	-	-	SAI1_ SD_B	-	-	QUADSPI_ BK1_IO3	-	-	-	-	-	EVENT OUT
	PF7	-	-	-	TIM11_ CH1	-	-	SAI1_ MCLK_B	-	-	QUADSPI_ BK1_IO2	-	-	-	-	-	EVENT OUT
	PF8	-	-	-	-	-	-	SAI1_ SCK_B	-	-	TIM13_CH1	QUADSPI_ BK1_IO0	-	-	-	-	EVENT OUT
	PF9	-	-	-	-	-	-	SAI1_ FS_B	-	-	TIM14_CH1	QUADSPI_ BK1_IO1	-	-	-	-	EVENT OUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	-	DCMI_ D11	-	EVENT OUT
	PF11	-	-	-	-	-	-	-	-	-	-	SAI2_SD_B	-	FMC_ SDNRAS	DCMI_ D12	-	EVENT OUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENT OUT
	PF13	-	-	-	-	FMPI2C1_ SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENT OUT
	PF14	-	-	-	-	FMPI2C1_ SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENT OUT
	PF15	-	-	-	-	FMPI2C1_ SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENT OUT

Table 16. General operating conditions (continued)

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
V _{DD}	Standard operating voltage	-	1.7 ⁽²⁾	-	3.6	V
V _{DDA} ⁽³⁾⁽⁴⁾	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V _{DD} ⁽⁵⁾	1.7 ⁽²⁾	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V _{BAT}	Backup operating voltage	-	1.65	-	3.6	
V _{DDUSB}	USB supply voltage (supply voltage for PA11, PA12, PB14 and PB15 pins)	USB not used	1.7	-	3.6	
		USB used	3	-	3.6	
V ₁₂	Regulator ON: 1.2 V internal voltage on V _{CAP_1} /V _{CAP_2} pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 120 MHz HCLK max frequency)	1.08	1.14	1.20	
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 144 MHz HCLK max frequency with over-drive OFF or 168 MHz with over-drive ON)	1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON)	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V _{CAP_1} /V _{CAP_2} pins ⁽⁶⁾	Max frequency 120 MHz	1.10	1.14	1.20	
		Max frequency 144 MHz	1.20	1.26	1.32	
		Max frequency 168 MHz	1.26	1.32	1.38	
V _{IN}	Input voltage on RST, FTf and FT pins ⁽⁷⁾	2 V ≤ V _{DD} ≤ 3.6 V	-0.3	-	5.5	V
		1.7 V ≤ V _{DD} ≤ 2 V	-0.3	-	5.2	
	Input voltage on TTa pins	-	-0.3	-	V _{DDA} +0.3	
	Input voltage on BOOT0 pin	-	0	-	9	
P _D	Power dissipation at T _A = 85 °C for suffix 6 or T _A = 105 °C for suffix 7 ⁽⁸⁾	LQFP64	-	-	345	mW
		WLCSP81	-	-	417	
		LQFP100	-	-	476	
		LQFP 144	-	-	606	
		UFBGA144 (7x7)	-	-	392	
		UFBGA144(10x10)	-	-	417	
T _A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	-	85	°C
		Low power dissipation ⁽⁹⁾	-40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	-	105	°C
		Low power dissipation ⁽⁹⁾	-40	-	125	
T _J	Junction temperature range	6 suffix version	-40	-	105	°C
		7 suffix version	-40	-	125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.16.2: Internal reset OFF](#)).
3. When the ADC is used, refer to [Table 74: ADC characteristics](#).
4. If V_{REF+} pin is present, it must respect the following condition: $V_{DDA}-V_{REF+} < 1.2$ V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. The over-drive mode is not supported when the internal regulator is OFF.
7. To sustain a voltage higher than $V_{DD}+0.3$, the internal Pull-up and Pull-Down resistors must be disabled
8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} .
9. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} .

Table 17. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum HCLK frequency vs Flash memory wait states (1)(2)	I/O operation	Possible Flash memory operations
$V_{DD} = 1.7$ to 2.1 V ⁽³⁾	Conversion time up to 1.2 Msps	20 MHz ⁽⁴⁾	168 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only
$V_{DD} = 2.1$ to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	180 MHz with 8 wait states and over-drive ON	– No I/O compensation	16-bit erase and program operations
$V_{DD} = 2.4$ to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	180 MHz with 7 wait states and over-drive ON	– I/O compensation works	16-bit erase and program operations
$V_{DD} = 2.7$ to 3.6 V ⁽⁵⁾	Conversion time up to 2.4 Msps	30 MHz	180 MHz with 5 wait states and over-drive ON	– I/O compensation works	32-bit erase and program operations

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.16.2: Internal reset OFF](#)).
4. Prefetch is not available.
5. The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

6.3.2 VCAP_1/VCAP_2 external capacitor

Stabilization for the main regulator is achieved by connecting external capacitor C_{EXT} to the V_{CAP_1} and V_{CAP_2} pin. For packages supporting only 1 V_{CAP} pin, the 2 C_{EXT} capacitors are replaced by a single capacitor. C_{EXT} is specified in [Table 18](#).

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled with prefetch) or RAM⁽¹⁾

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽²⁾			Unit
					T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in RUN mode	External clock, PLL ON, all peripherals enabled ⁽³⁾⁽⁴⁾	180	86	93.0	115.0	125.0	mA
			168 ⁽⁵⁾	79	85.1	111.2	117.7	
			150	73	79.6	104.8	111.2	
			144 ⁽⁵⁾	68	73.5	97.3	103.3	
			120	54	59.3	79.7	84.7	
			90	42	47.23	65.50	70.10	
			60	29	33.7	49.5	53.4	
			30	16	20.8	34.0	37.4	
			25	13	18.4	31.2	34.5	
		HSI, PLL OFF, all peripherals enabled ⁽³⁾⁽⁴⁾	16	8	13.8	25.0	28.3	
			8	5	10.8	21.1	24.2	
			4	3.0	9.1	18.9	22.0	
			2	2.1	8.1	17.8	20.9	
		External clock, PLL ON, all Peripherals disabled ⁽³⁾	180	46	55.0	75.0	86.0	
			168	43	49.6	67.5	72.6	
			150	41	48.2	65.8	70.8	
			144 ⁽⁵⁾	38	43.6	61.9	66.8	
			120	32	37.3	53.7	58.0	
			90	26	30.7	46.0	50.0	
			60	18	22.8	36.4	40.1	
			30	10	14.9	27.1	30.2	
			25	9	13.55	25.40	28.54	
		HSI, PLL OFF, all peripherals disabled ⁽³⁾	16	5	11.1	21.8	25.0	
			8	3	9.5	19.4	22.5	
			4	2.4	8.34	18.10	21.17	
			2	1.8	7.77	17.39	20.50	

1. Code and data processing running from SRAM1 using boot pins.

2. Guaranteed based on test during characterization.

3. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

4. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

5. Overdrive OFF

Table 32. Typical current consumption in Sleep mode, regulator ON, $V_{DD}=1.7\text{ V}^{(1)}$

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max			Unit
					$T_A = 25\text{ °C}$	$T_A = 85\text{ °C}$	$T_A = 105\text{ °C}$	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	All Peripherals enabled Flash on	168	43.7	47.5	66.5	79.3	mA
			150	39.2	42.7	60.7	73.3	
			144	35.7	38.8	55.3	66.9	
			120	26.5	28.6	41.8	51.6	
			90	20.0	21.91	33.85	43.20	
			60	13.6	15.2	25.8	34.9	
			30	7.4	8.5	18.4	27.0	
			25	6.3	7.5	16.9	25.5	
		All Peripherals disabled, flash on	168	7.3	8.6	21.2	31.9	
			150	6.6	7.94	20.4	31.0	
			144	6.0	7.3	18.6	28.5	
			120	4.6	5.5	14.9	23.4	
			90	3.6	4.6	13.6	22.1	
			60	2.6	3.4	12.5	20.8	
			30	1.8	2.7	11.3	19.7	
			25	1.6	2.49	11.09	19.42	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 35: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 34. Switching output I/O current consumption⁽¹⁾

Symbol	Parameter	Conditions	I/O toggling frequency (fsw)	Typ	Unit
I _{DDIO}	I/O switching Current	V _{DD} = 3.3 V C = C _{INT} ⁽²⁾	2 MHz	0.0	mA
			8 MHz	0.2	
			25 MHz	0.6	
			50 MHz	1.1	
			60 MHz	1.3	
			84 MHz	1.8	
			90 MHz	1.9	
		V _{DD} = 3.3 V C _{EXT} = 0 pF C = C _{INT} + C _{EXT} + C _S	2 MHz	0.1	
			8 MHz	0.4	
			25 MHz	1.23	
			50 MHz	2.43	
			60 MHz	2.93	
			84 MHz	3.86	
			90 MHz	4.07	

Table 49. Flash memory programming with V_{PP} (continued)

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
$t_{VPP}^{(3)}$	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 50. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value Min ⁽¹⁾	Unit
-	-			
N_{END}	Endurance	$T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions)	10	Kcycles
t_{RET}	Data retention	1 kcycle ⁽²⁾ at $T_A = 85$ °C	30	Years
		1 kcycle ⁽²⁾ at $T_A = 105$ °C	10	
		10 kcycles ⁽²⁾ at $T_A = 55$ °C	20	

1. Guaranteed based on test during characterization.
2. Cycling performed over the whole temperature range.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

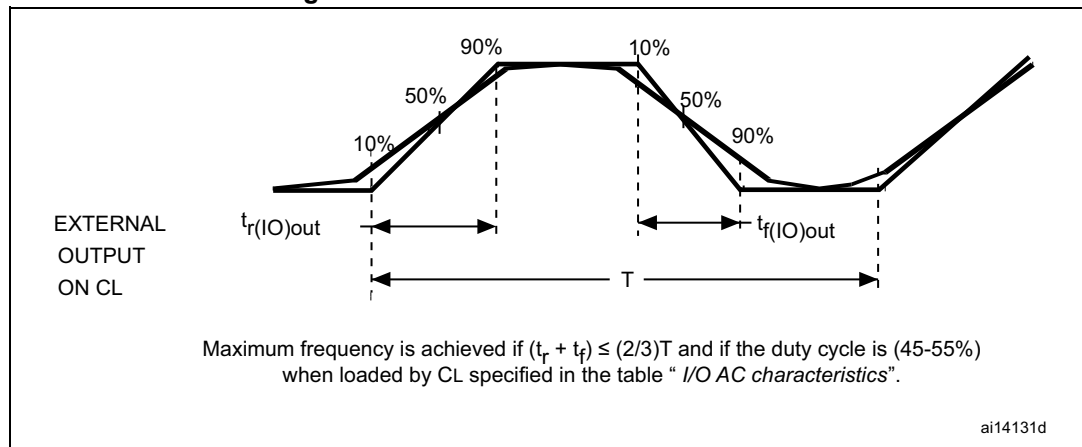
- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB:** A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 51](#). They are based on the EMS levels and classes defined in application note AN1709.

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in [Figure 32](#).
4. For maximum frequencies above 50 MHz and $V_{DD} > 2.4$ V, the compensation cell should be used.

Figure 32. I/O AC characteristics definition



6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 56: I/O static characteristics](#)).

Unless otherwise specified, the parameters given in [Table 59](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 16](#).

Table 59. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}^{(2)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(2)}$	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	μ s

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Table 92. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK} - 2$	$4T_{HCLK} + 0.5$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}	$T_{HCLK} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{HCLK} - 2$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{HCLK} + 1.5$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK} + 0.5$	-	

1. $C_L = 30$ pF.
2. Guaranteed based on test during characterization.

Table 93. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK} + 0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK} + 2$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK} + 1.5$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} - 1$	-	

1. $C_L = 30$ pF.
2. Guaranteed based on test during characterization.

Synchronous waveforms and timings

[Figure 54](#) through [Figure 57](#) represent synchronous waveforms and [Table 94](#) through [Table 97](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F446 reference manual: RM0390)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Table 103. LPDDR SDRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$F_{(SDCLK)}$	Frequency of operation	-	84	MHz
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK} - 0.5$	$2T_{HCLK} + 0.5$	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0.5	-	
$t_{d(SDCLK_Add)}$	Address valid time	-	3	
$t_{d(SDCLKL_SDNWE)}$	SDNWE valid time	-	3	
$t_{h(SDCLKL_SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	2.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	2	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. CL = 10 pF.

2. Guaranteed based on test during characterization.

6.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in [Table 104](#) for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 16](#), with the following configuration:

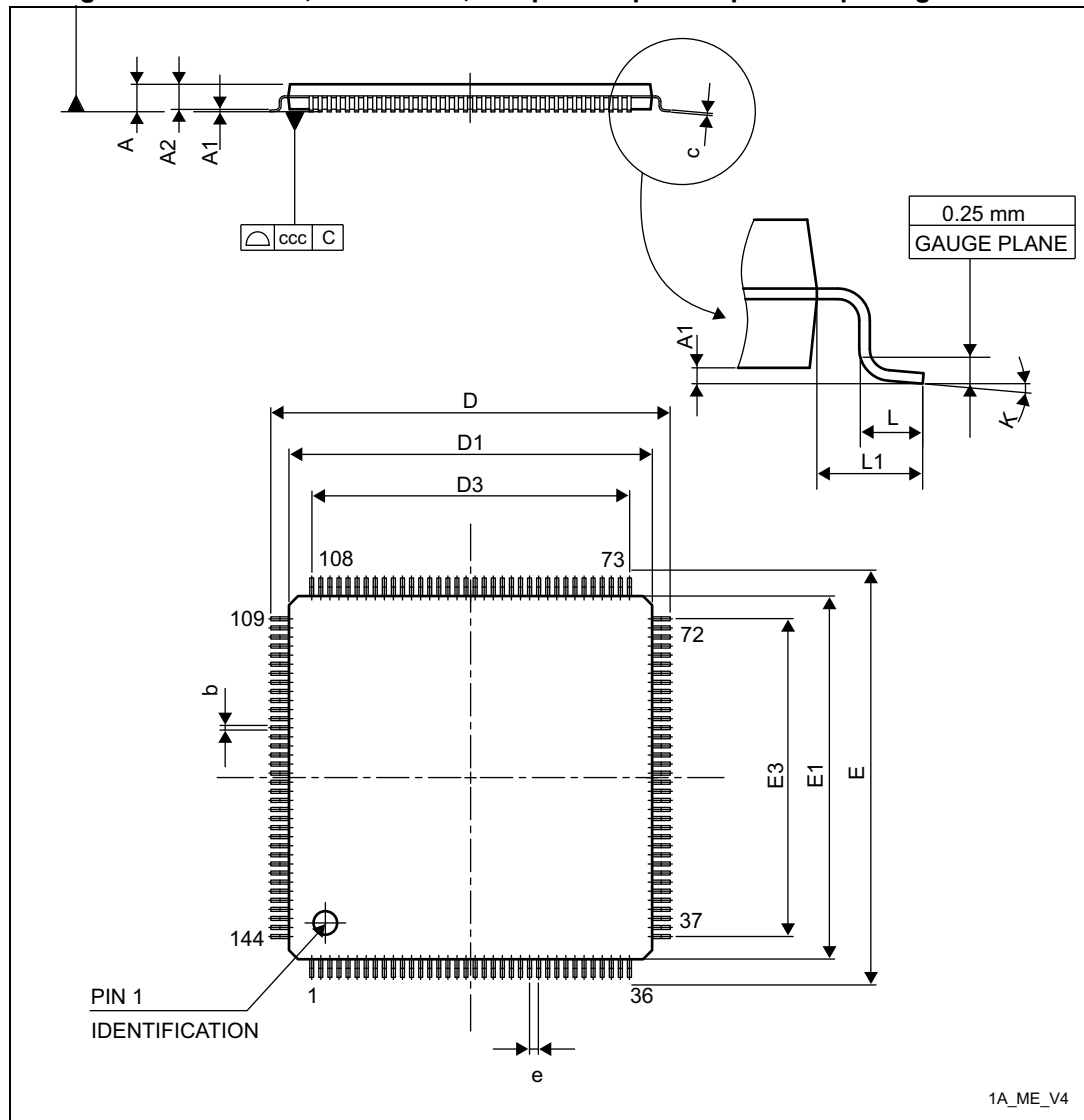
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 104. DCMI characteristics

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/ f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	1	-	ns
$t_{h(DATA)}$	Data input hold time	3.5	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	2	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	0	-	

7.3 LQFP144 package information.

Figure 73. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 110. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

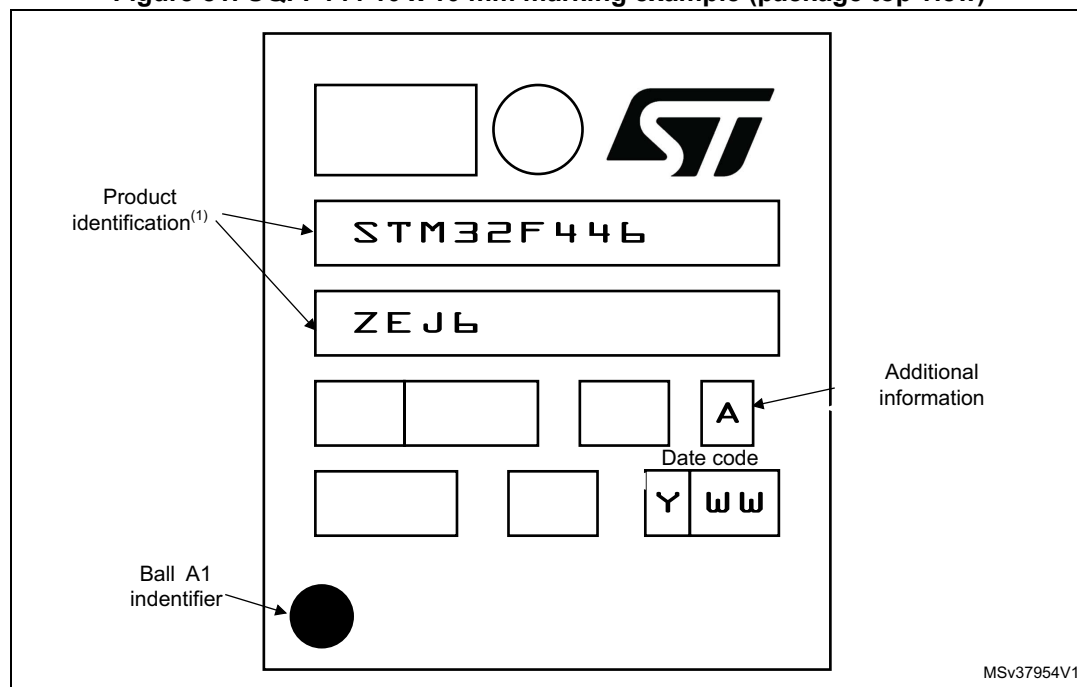
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for UFBGA144 10 x 10 mm package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 81. UQFP144 10 x 10 mm marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.