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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f446zej7

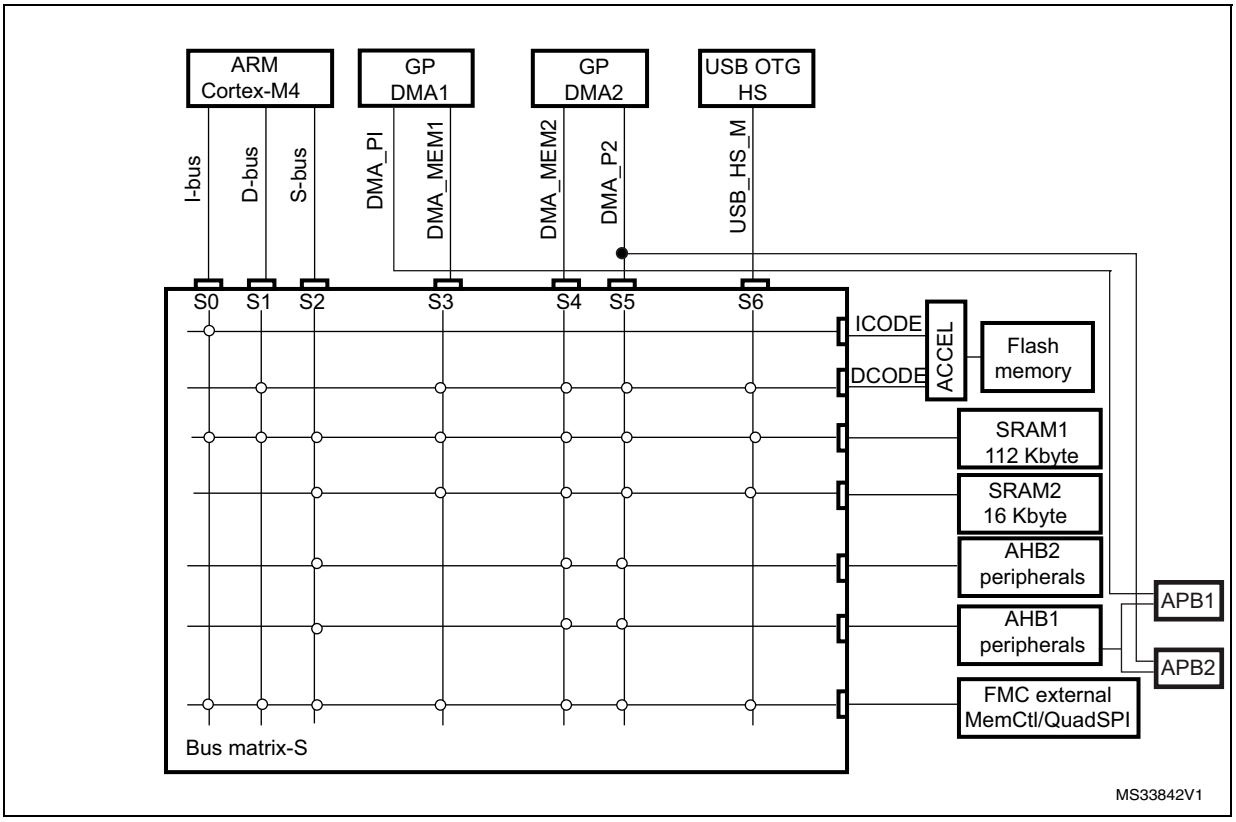
1 Introduction

This document provides the description of the STM32F446xC/E products.

The STM32F446xC/E document should be read in conjunction with the STM32F4xx reference manual.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214), available from the *www.st.com*.

Figure 4. STM32F446xC/E and Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is not connected to V_{DD} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

The SPDIF-RX also offers a signal named spdifrx_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

3.28 Serial Audio interface (SAI)

The devices feature two serial audio interfaces (SAI1 and SAI2). Each serial audio interfaces based on two independent audio sub blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub blocks can be configured in master or in slave mode. The SAIs use a PLL to achieve audio class accuracy.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 and SA2 can be served by the DMA controller.

3.29 Audio PLL (PLLI^{2}S)

The devices feature an additional dedicated PLL for audio I^{2}S and SAI applications. It allows to achieve error-free I^{2}S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^{2}S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I^{2}S/SAI flow with an external PLL (or Codec output).

3.30 Serial Audio Interface PLL(PLLSAI)

An additional PLL dedicated to audio and USB is used for SAI1 and SAI2 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the 48MHz clock for USB FS and SDIO in case the system PLL is programmed with factors not multiple of 48MHz.

3.31 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

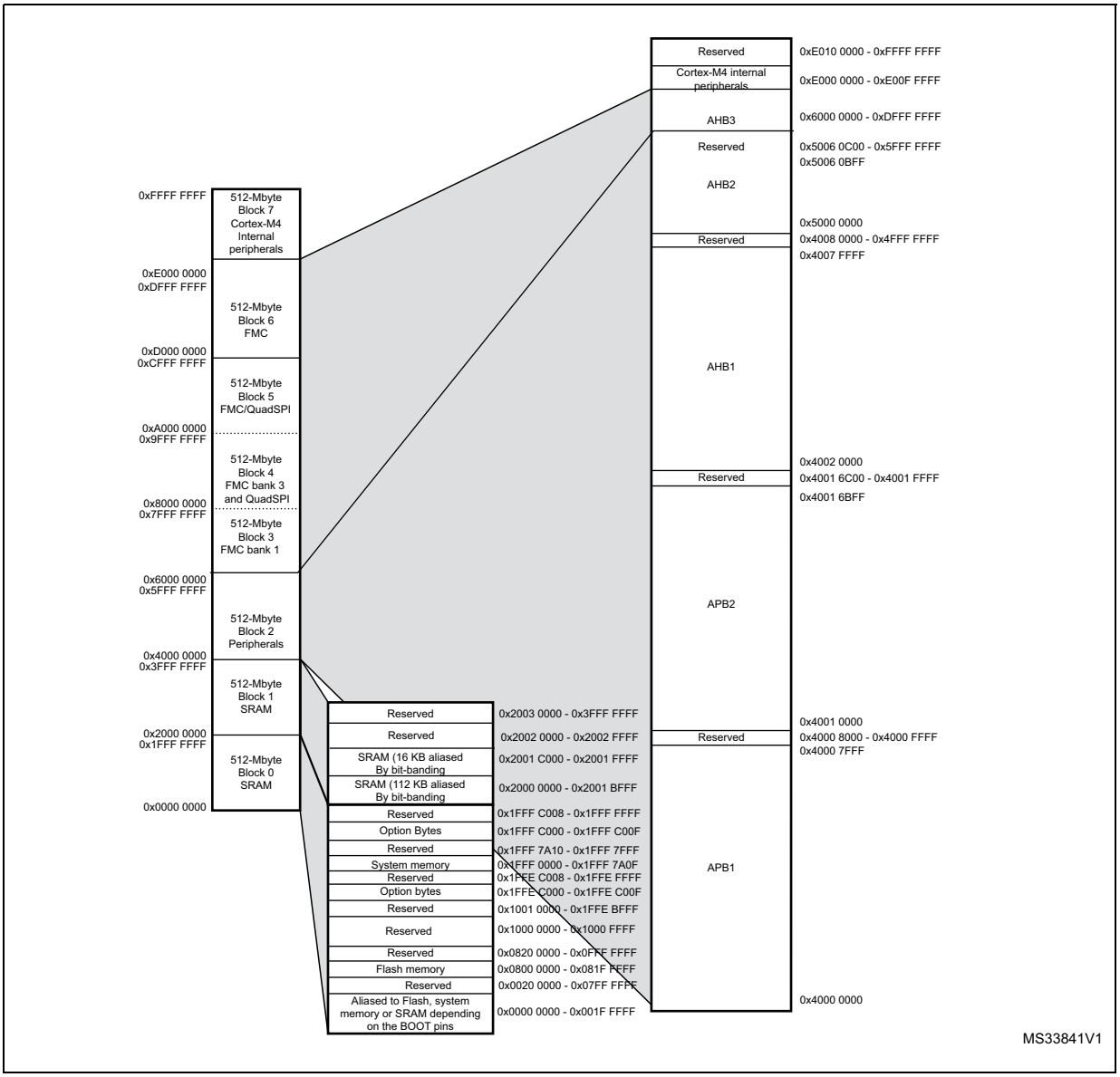
Table 10. STM32F446xx pin and ball descriptions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP 81	UFBGA144	LQFP144						
-	61	-	K11	85	PD14	I/O	FTf	-	TIM4_CH3, FMPI2C1_SCL, SAI2_SCK_A, FMC_D0, EVENTOUT	-
-	62	-	K12	86	PD15	I/O	FTf	-	TIM4_CH4, FMPI2C1_SDA, FMC_D1, EVENTOUT	-
-	-	-	J12	87	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	-	-	J11	88	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	-	-	J10	89	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	-	-	H12	90	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	-	-	H11	91	PG6	I/O	FT	-	QUADSPI_BK1_NCS, DCMI_D12, EVENTOUT	-
-	-	-	H10	92	PG7	I/O	FT	-	USART6_CK, FMC_INT, DCMI_D13, EVENTOUT	-
-	-	-	G11	93	PG8	I/O	FT	-	SPDIFRX_IN2, USART6_RTS, FMC_SDCLK, EVENTOUT	-
-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	F10	-	VDD	S	-	-	-	-
-	-	E1	C11	95	VDDUSB	S	-	-	-	-
37	63	F1	G12	96	PC6	I/O	FTf	-	TIM3_CH1, TIM8_CH1, FMPI2C1_SCL, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, EVENTOUT	-
38	64	F2	F12	97	PC7	I/O	FTf	-	TIM3_CH2, TIM8_CH2, FMPI2C1_SDA, SPI2_SCK/I2S2_CK, I2S3_MCK, SPDIFRX_IN1, USART6_RX, SDIO_D7, DCMI_D1, EVENTOUT	-
39	65	F3	F11	98	PC8	I/O	FT	-	TRACED0, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-

5 Memory mapping

The memory map is shown in *Figure 15*

Figure 15. Memory map



6.3 Operating conditions

6.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF		0	-	120	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-	144	
			Over-drive ON		-	168	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-	168	
			Over-drive ON		-	180	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		0	-	42	
		Over-drive ON		0	-	45	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		0	-	84	
		Over-drive ON		0	-	90	

Table 27. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max			Unit
				V_{DD} = 3.6 V			
			T_A = 25 °C	T_A = 25 °C(1)	T_A = 85 °C	T_A = 105 °C(1)	
$I_{DD\_STOP\_NM}$ (normal mode)	Supply current in Stop mode with voltage regulator in main regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.234	1.2	10	16	mA
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.205	1	9.5	15	
	Supply current in Stop mode with voltage regulator in Low Power regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.15	0.95	8.5	14	
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.121	0.9	6	12	
$I_{DD\_STOP\_UDM}$ (under-drive mode)	Supply current in Stop mode with voltage regulator in main regulator and under-drive mode	Flash memory in Deep power down mode, main regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.119	0.4	3	5	
	Supply current in Stop mode with voltage regulator in Low Power regulator and under-drive mode	Flash memory in Deep power down mode, Low Power regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.055	0.35	3	5	

1. Data based on characterization, tested in production.

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ Appli)			Unit
		Scale 1 + OverDrive	Scale 2	Scale 3	
APB1	TIM2	18.18	16.92	15.07	µA/MHz
	TIM3	14.49	13.47	12.00	
	TIM4	15.18	14.11	12.50	
	TIM5	16.91	15.69	14.07	
	TIM6	2.69	2.47	2.20	
	TIM7	2.56	2.44	2.17	
	TIM12	7.07	6.56	5.83	
	TIM13	4.96	4.64	4.07	
	TIM14	5.09	4.72	4.27	
	WWDG	1.07	1.00	0.93	
	SPI2(2)	1.89	1.78	1.57	
	SPI3(2)	1.93	1.81	1.67	
	SPDIFRX	6.91	6.44	5.80	
	USART2	4.20	3.83	3.40	
	USART3	4.22	3.94	3.50	
	UART4	4.13	3.89	3.40	
	UART5	4.04	3.78	3.33	
	I2C1	3.98	3.69	3.33	
	I2C2	3.91	3.61	3.17	
	I2C3	3.76	3.53	3.13	
	FMPI2C1	5.51	5.19	4.57	
	CAN1	6.58	6.14	5.43	
	CAN2	5.91	5.56	4.90	
	CEC	0.71	0.69	0.60	
	DAC	2.96	2.72	2.40	

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	6	6	CPU clock cycle
$T_{WUSLEEPFDSM}$(1)	Wakeup from Sleep with Flash memory in Deep power down mode	-	33.5	50	µs
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	12.8	15	
		Main regulator is ON and Flash memory in Deep power down mode	104.9	115	
		Low power regulator is ON	20.6	28	
		Low power regulator is ON and Flash memory in Deep power down mode	112.8	120	
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	110	140	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	114.4	128	
$t_{WUSTDBY}$(2)(3)	Wakeup from Standby mode	-	325	400	

1. Guaranteed based on test during characterization.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ maximum value is given at –40 °C.

6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 56: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 23*.

The characteristics given in *Table 37* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

Table 43. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{LOCK}	PLL lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed based on test during characterization.

Table 44. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)	-		0.95(2)	1	2.10	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock	-		-	-	216	MHz
f_{VCO_OUT}	PLLI2S VCO output	-		100	-	432	MHz
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	-
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps

Table 57. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+ 8mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 14*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 14* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

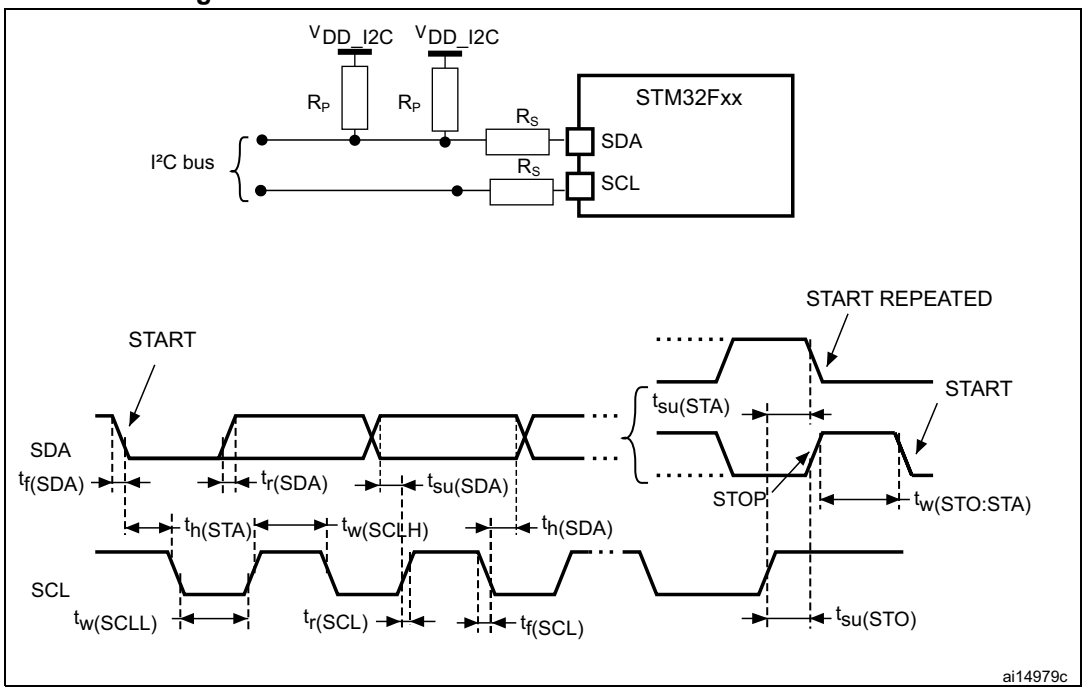
The definition and values of input/output AC characteristics are given in *Figure 32* and *Table 58*, respectively.

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 58. I/O AC characteristics(1)(2)

OSPEEDRy[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.7 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	4	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns

Figure 34. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 67* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 67. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	SAI Main clock output	-	256 x 8K	256 x Fs	MHz
f_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128 x Fs(3)	MHz
		Slave data: 32 bits	-	128 x Fs(3)	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤3.6 V	-	14	%
		Master mode 1.71 V ≤ V_{DD} ≤3.6 V	-	17.5	ns
$t_{h(FS)}$	FS hold time	Master mode	7	-	
$t_{su(FS)}$	FS setup time	Slave mode	1	-	
$t_{h(FS)}$	FS hold time	Slave mode	1	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	1	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave trasmitter (after enable edge 2.7 V ≤ V_{DD} ≤3.6 V	-	9.5	
		Slave transmitter (after enable edge 1.71 V ≤ V_{DD} ≤3.6 V	-	16	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge	6	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Master transmitter (after enable edge 2.7 V ≤ V_{DD} ≤3.6 V	-	15	
		Master transmitter (after enable edge 1.71 V ≤ V_{DD} ≤3.6 V	-	18	
$t_{h(SD\_B\_ST)}$	Data output hold time	Master transmitter (after enable edge	7	-	

1. Guaranteed based on test during characterization.
2. 256xFs maximum corresponds to 45 MHz (APB2 xaximum frequency)
3. With Fs = 192 KHz

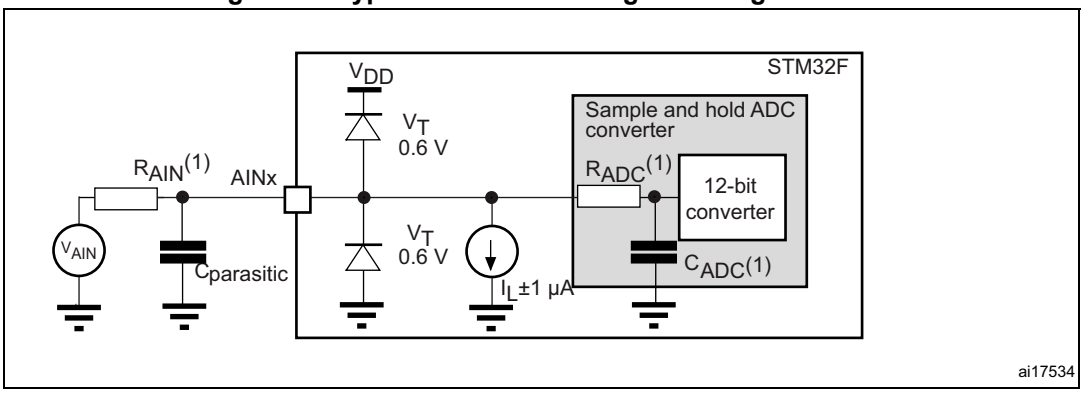
6.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 74* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 16*.

Table 74. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	V_{DDA} –V_{REF+} < 1.2 V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Figure 46. Typical connection diagram using the ADC



1. Refer to *Table 74* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.23 V_{BAT} monitoring characteristics

Table 82. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	- 1	-	+ 1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.24 Reference voltage

The parameters given in *Table 83* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 83. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient	-	-	30	50	ppm/°C
t_{START}(2)	Startup time	-	-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 84. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C $_{VDDA}$ = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

6.3.25 DAC electrical characteristics

Table 85. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	-	1.7(1)	-	3.6	V	-
V_{REF+}	Reference supply voltage	-	1.7(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$

Table 103. LPSDR SDRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$F_{(SDCLK)}$	Frequency of operation	-	84	MHz
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}$ - 0.5	$2T_{HCLK}$ + 0.5	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	5	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0.5	-	
$t_{d(SDCLK\_Add)}$	Address valid time	-	3	
$t_{d(SDCLKL\_SDNWE))}$	SDNWE valid time	-	3	
$t_{h(SDCLKL\_SDNWE))}$	SDNWE hold time	0	-	
$t_{d(SDCLKL\_SDNE))}$	Chip select valid time	-	2.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	2	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. CL = 10 pF.
2. Guaranteed based on test during characterization.

6.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 104* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 16*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 104. DCMI characteristics

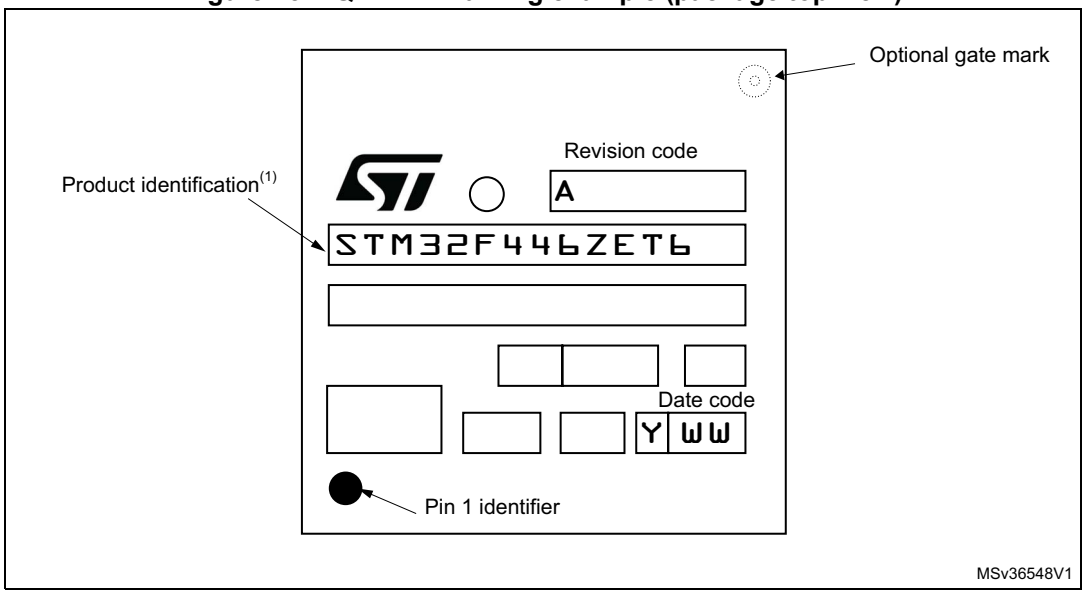
Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	1	-	ns
$t_{h(DATA)}$	Data input hold time	3.5	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	2	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	0	-	

Device marking for LQFP144 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 75. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Revision history

Table 119. Document revision history

Date	Revision	Changes
17-Feb-2015	1	Initial release.
16-Mar-2015	2	Added note 2 inside *Table 2* Updated *Table 11*, *Table 23*, *Table 24*, *Table 25*, *Table 26*, *Table 30*, *Table 51*, *Table 52*, *Table 53*, and *Table 61* Added condition inside *Typical and maximum current consumption* and *Additional current consumption* Added *FMPI2C characteristics* Added *Table 62* and *Figure 35*
29-May-2015	3	Updated: – *Section 6.3.15: Absolute maximum ratings (electrical sensitivity)* – *Section 7: Package information* – *Table 2: STM32F446xC/E features and peripheral counts* – *Table 13: STM32F446xC/xE WLCSP81 ballout* – *Figure 53: ESD absolute maximum ratings* – *Figure 54: Synchronous multiplexed NOR/PSRAM read timings* Added: – *Figure 78: UQFP144 7 x 7 mm marking example (package top view)*, – *Figure 81: UQFP144 10 x 10 mm marking example (package top view)*, – *Figure 84: WLCSP81 10 x 10 mm marking example (package top view)*
10-Aug-2015	4	Updated: – *Figure 14: STM32F446xC/xE UFBGA144 ballout* – *Table 10: STM32F446xx pin and ball descriptions* – *Table 18: VCAP_1/VCAP_2 operating conditions* – *Section 3.15: Power supply schemes* – *Section 6.3.2: VCAP_1/VCAP_2 external capacitor* Added: – *Figure 5: VDDUSB connected to an external independent power supply* – Notes *3* and *4* below *Figure 18: Power supply scheme*