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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21322dnsp-w4

Table 1.2 Specifications for R8C/32D Group (2)

Item	Function	Specification
Flash Memory		• Programming and erasure voltage: $V_{CC} = 2.7$ to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		$f(XIN) = 20$ MHz ($V_{CC} = 2.7$ to 5.5 V) $f(XIN) = 5$ MHz ($V_{CC} = 1.8$ to 5.5 V)
Current consumption		Typ. 6.5 mA ($V_{CC} = 5.0$ V, $f(XIN) = 20$ MHz) Typ. 3.5 mA ($V_{CC} = 3.0$ V, $f(XIN) = 10$ MHz) Typ. 3.5 μ A ($V_{CC} = 3.0$ V, wait mode ($f(XCIN) = 32$ kHz)) Typ. 2.0 μ A ($V_{CC} = 3.0$ V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾
Package		20-pin LSSOP Package code: PLSP0020JB-A (previous code: 20P2F-A)

Note:

1. Specify the D version if D version functions are to be used.

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

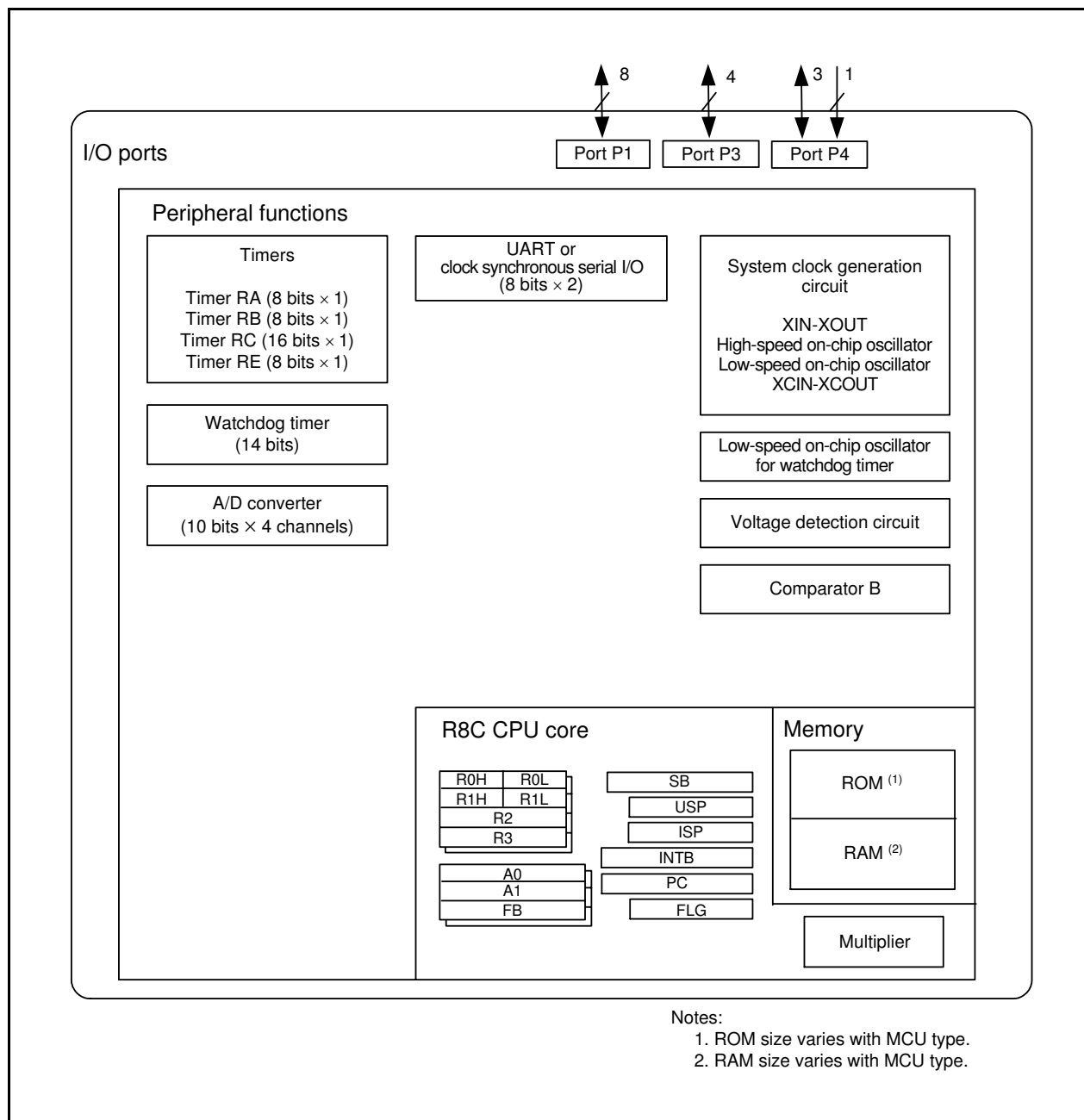


Figure 1.2 Block Diagram

Table 4.6 SFR Information (6) ⁽¹⁾

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RC Pin Select Register	TRBRCR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch			
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
FFDFh	ID1		(Note 2)
FFE3h	ID2		(Note 2)
FFEBh	ID3		(Note 2)
FFEFh	ID4		(Note 2)
FFF3h	ID5		(Note 2)
FFF7h	ID6		(Note 2)
FFFBh	ID7		(Note 2)
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		–0.3 to 6.5	V
V _I	Input voltage		–0.3 to V _{CC} + 0.3	V
V _O	Output voltage		–0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	–40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		–20 to 85 (N version) / –40 to 85 (D version)	°C
T _{stg}	Storage temperature		–65 to 150	°C

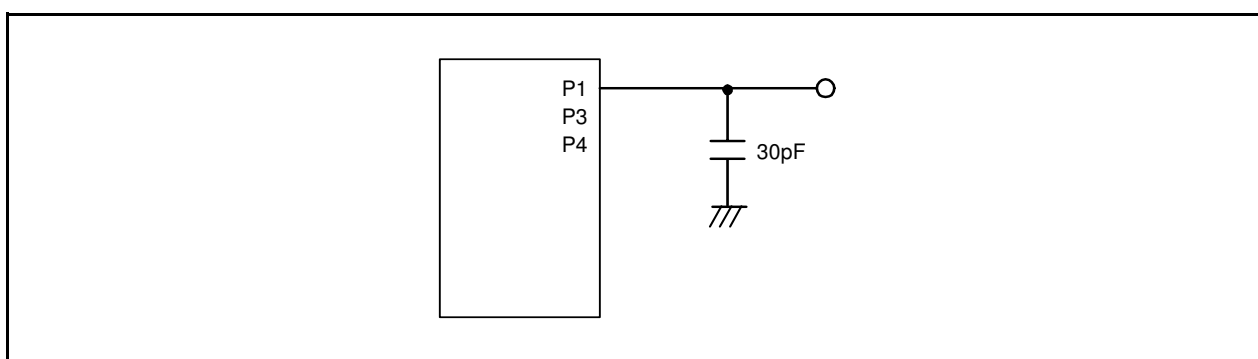


Figure 5.1 Ports P1, P3, P4 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		Vref = AVCC		–	–	10	Bit
–	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN8 to AN11 input	–	–	±3	LSB
			Vref = AVCC = 3.3 V	AN8 to AN11 input	–	–	±5	LSB
			Vref = AVCC = 3.0 V	AN8 to AN11 input	–	–	±5	LSB
			Vref = AVCC = 2.2 V	AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 3.3 V	AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 3.0 V	AN8 to AN11 input	–	–	±2	LSB
			Vref = AVCC = 2.2 V	AN8 to AN11 input	–	–	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	20	MHz
			3.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	16	MHz
			2.7 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	10	MHz
			2.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.15	–	–	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.15	–	–	μs
tsAMP	Sampling time		φAD = 20 MHz		0.75	–	–	μs
IVref	Vref current		VCC = 5 V, XIN = f1 = φAD = 20 MHz		–	45	–	μA
Vref	Reference voltage				2.2	–	AVCC	V
VIA	Analog input voltage (3)				0	–	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2\text{ to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = -20\text{ to }85^\circ\text{C}$ (N version) / $-40\text{ to }85^\circ\text{C}$ (D version), unless otherwise specified.
- The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
VI	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
td	Comparator output delay time ⁽²⁾	$V_I = V_{ref} \pm 100\text{ mV}$	—	0.1	—	μs
ICMP	Comparator operating current	$V_{CC} = 5.0\text{ V}$	—	17.5	—	μA

Notes:

- $V_{CC} = 2.7\text{ to }5.5\text{ V}$, $T_{opr} = -20\text{ to }85^\circ\text{C}$ (N version) / $-40\text{ to }85^\circ\text{C}$ (D version), unless otherwise specified.
- When the digital filter is disabled.

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level V _{det0_0} ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level V _{det0_1} ⁽²⁾		2.15	2.35	2.50	V
	Voltage detection level V _{det0_2} ⁽²⁾		2.70	2.85	3.05	V
	Voltage detection level V _{det0_3} ⁽²⁾		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽⁴⁾	At the falling of V _{CC} from 5 V to (V _{det0_0} – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 5.0 V	—	1.5	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level V _{det1_0} ⁽²⁾	At the falling of V _{CC}	2.00	2.20	2.40	V
	Voltage detection level V _{det1_1} ⁽²⁾	At the falling of V _{CC}	2.15	2.35	2.55	V
	Voltage detection level V _{det1_2} ⁽²⁾	At the falling of V _{CC}	2.30	2.50	2.70	V
	Voltage detection level V _{det1_3} ⁽²⁾	At the falling of V _{CC}	2.45	2.65	2.85	V
	Voltage detection level V _{det1_4} ⁽²⁾	At the falling of V _{CC}	2.60	2.80	3.00	V
	Voltage detection level V _{det1_5} ⁽²⁾	At the falling of V _{CC}	2.75	2.95	3.15	V
	Voltage detection level V _{det1_6} ⁽²⁾	At the falling of V _{CC}	2.85	3.10	3.40	V
	Voltage detection level V _{det1_7} ⁽²⁾	At the falling of V _{CC}	3.00	3.25	3.55	V
	Voltage detection level V _{det1_8} ⁽²⁾	At the falling of V _{CC}	3.15	3.40	3.70	V
	Voltage detection level V _{det1_9} ⁽²⁾	At the falling of V _{CC}	3.30	3.55	3.85	V
	Voltage detection level V _{det1_A} ⁽²⁾	At the falling of V _{CC}	3.45	3.70	4.00	V
	Voltage detection level V _{det1_B} ⁽²⁾	At the falling of V _{CC}	3.60	3.85	4.15	V
	Voltage detection level V _{det1_C} ⁽²⁾	At the falling of V _{CC}	3.75	4.00	4.30	V
	Voltage detection level V _{det1_D} ⁽²⁾	At the falling of V _{CC}	3.90	4.15	4.45	V
	Voltage detection level V _{det1_E} ⁽²⁾	At the falling of V _{CC}	4.05	4.30	4.60	V
	Voltage detection level V _{det1_F} ⁽²⁾	At the falling of V _{CC}	4.20	4.45	4.75	V
—	Hysteresis width at the rising of V _{CC} in voltage detection 1 circuit	V _{det1_0} to V _{det1_5} selected	—	0.07	—	V
		V _{det1_6} to V _{det1_F} selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	At the falling of V _{CC} from 5 V to (V _{det1_0} – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time ⁽²⁾	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.9 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	⁽¹⁾	0	—	50000	mV/msec

Notes:

1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

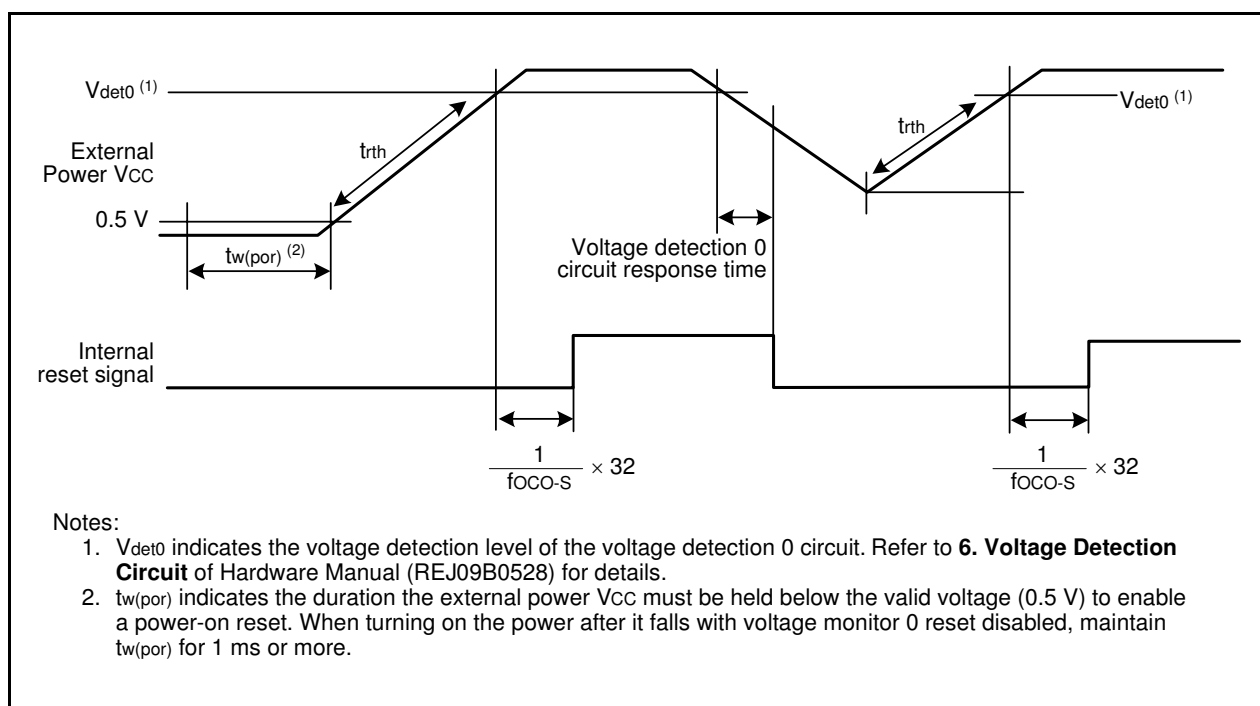
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	38.4	40	41.6	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽³⁾	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	35.389	36.864	38.338	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	30.72	32	33.28	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	30.40	32	33.60	MHz
–	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	0.5	3	ms
–	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	400	–	μA

Notes:

1. $V_{CC} = 1.8$ to 5.5 V , $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.
3. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	30	100	μs
–	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	2	–	μA

Note:

1. $V_{CC} = 1.8$ to 5.5 V , $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		–	–	2000	μs

Notes:

1. The measurement condition is $V_{CC} = 1.8$ to 5.5 V and $T_{opr} = 25^{\circ}\text{C}$.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output “H” voltage	Other than XOUT	Drive capacity High VCC = 5 V	IOH = –20 mA	VCC – 2.0	–	VCC	V
			Drive capacity Low VCC = 5 V	IOH = –5 mA	VCC – 2.0	–	VCC	V
		XOUT	VCC = 5V	IOH = –200 μA	1.0	–	VCC	V
VOL	Output “L” voltage	Other than XOUT	Drive capacity High VCC = 5 V	IOL = 20 mA	–	–	2.0	V
			Drive capacity Low VCC = 5 V	IOL = 5 mA	–	–	2.0	V
		XOUT	VCC = 5V	IOL = 200 μA	–	–	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2			0.1	1.2	–	V
		RESET			0.1	1.2	–	V
IIH	Input “H” current		VI = 5 V, VCC = 5.0 V		–	–	5.0	μA
IIL	Input “L” current		VI = 0 V, VCC = 5.0 V		–	–	–5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, VCC = 5.0 V		25	50	100	kΩ
RfXIN	Feedback resistance	XIN			–	0.3	–	MΩ
RfXCIN	Feedback resistance	XCIN			–	8	–	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	–	–	V

1. $4.2\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ at $T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), $f(\text{XIN}) = 20\text{ MHz}$, unless otherwise specified.

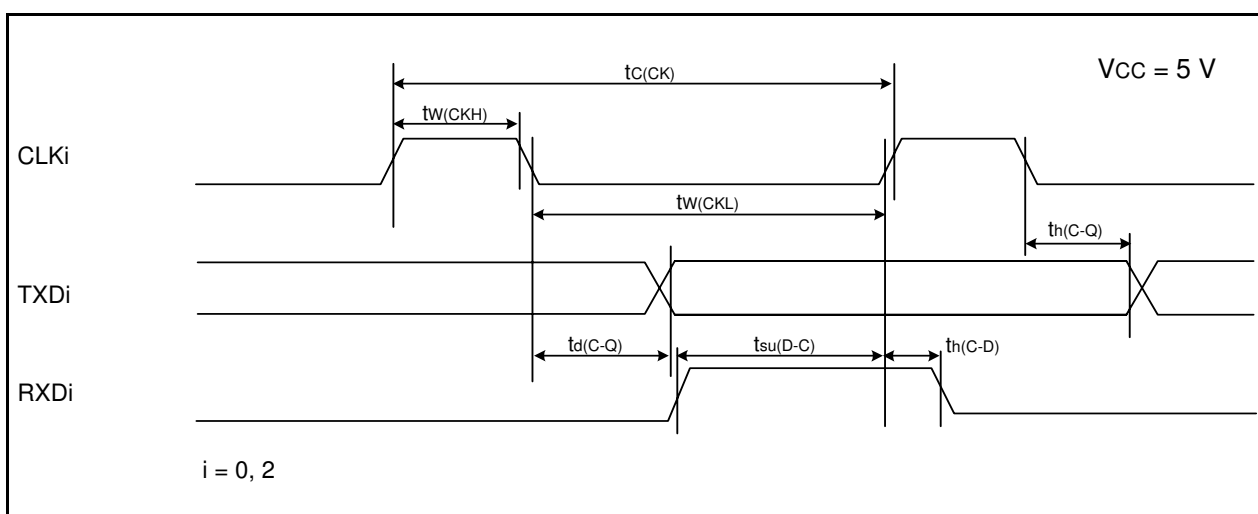
Table 5.14 Electrical Characteristics (2) [$3.3\text{ V} \leq V_{CC} \leq 5.5\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on f _{OCO-F} = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on f _{OCO-F} = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on f _{OCO-F} = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	—	85	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	—	47	—	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	15	100	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	4	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	—	3.5	—	μA
		Stop mode	XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	μA
			XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	5.0	—	μA

Table 5.17 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{w(CKH)}$	CLKi input "H" width	100	—	ns
$t_{w(CKL)}$	CLKi input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0, 2

**Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.18 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{Kli}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	250 (1)	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	250 (2)	—	ns

Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

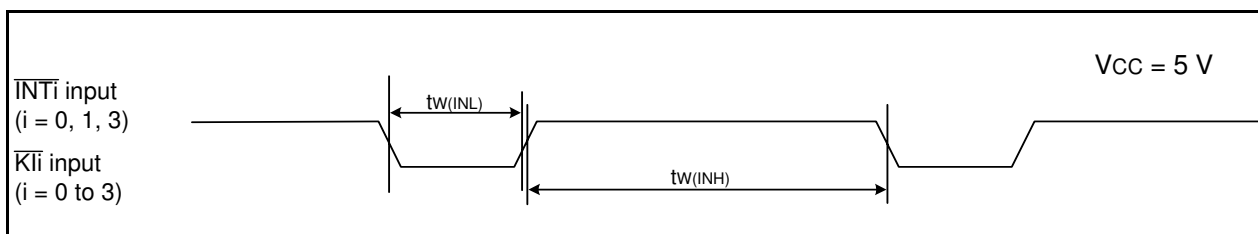
**Figure 5.7 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 5 V**

Table 5.19 Electrical Characteristics (3) [$2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Other than XOUT	Drive capacity High	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT		I _{OH} = -200 μ A	1.0	—	V _{CC}	V
V _{OL}	Output "L" voltage	Other than XOUT	Drive capacity High	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
		XOUT		I _{OL} = 200 μ A	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2	V _{CC} = 3.0 V		0.1	0.4	—	V
		RESET	V _{CC} = 3.0 V		0.1	0.5	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3.0 V		—	—	4.0	μ A
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3.0 V		—	—	-4.0	μ A
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3.0 V		42	84	168	k Ω
R _{FXIN}	Feedback resistance	XIN			—	0.3	—	M Ω
R _{FXCIN}	Feedback resistance	XCIN			—	8	—	M Ω
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:

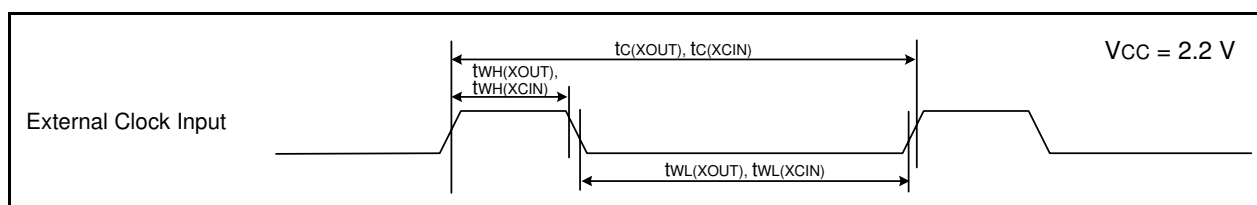
1. $2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$ at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.26 Electrical Characteristics (6) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]
($T_{opr} = -20\text{ to }85^{\circ}\text{C}$ (N version) / $-40\text{ to }85^{\circ}\text{C}$ (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	2.2	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	0.8	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.7	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRC = 1	–	1	–	mA
		Low-speed on- chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	300	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	80	350	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.5	–	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	μA

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$)****Table 5.27 External Clock Input (XOUT, XCIN)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{XOUT})$	XOUT input cycle time	200	–	ns
$t_{WH}(\text{XOUT})$	XOUT input “H” width	90	–	ns
$t_{WL}(\text{XOUT})$	XOUT input “L” width	90	–	ns
$t_c(\text{XCIN})$	XCIN input cycle time	14	–	μs
$t_{WH}(\text{XCIN})$	XCIN input “H” width	7	–	μs
$t_{WL}(\text{XCIN})$	XCIN input “L” width	7	–	μs

**Figure 5.12 External Clock Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.28 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{TRAIO})$	TRAIO input cycle time	500	–	ns
$t_{WH}(\text{TRAIO})$	TRAIO input “H” width	200	–	ns
$t_{WL}(\text{TRAIO})$	TRAIO input “L” width	200	–	ns

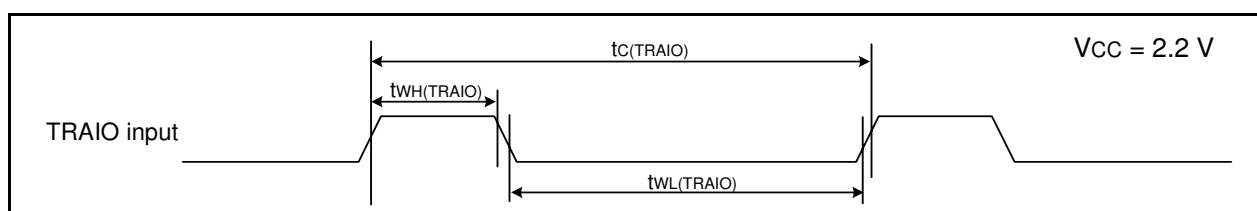
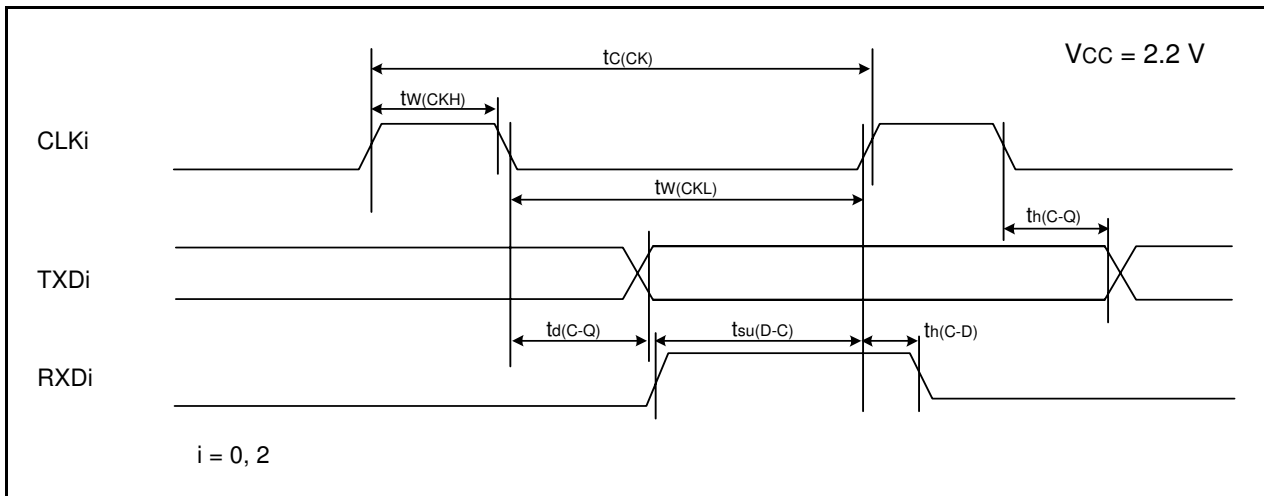
**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.29 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{w(CKH)}$	CLKi input "H" width	400	—	ns
$t_{w(CKL)}$	CLKi input "L" width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

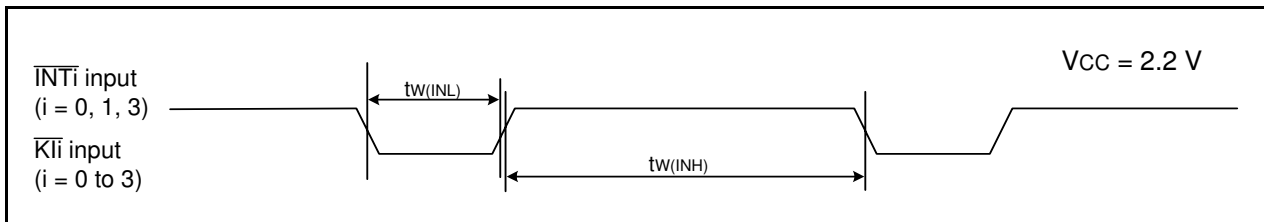
i = 0, 2

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.30 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{Kli}$ (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width, $\overline{Kli}$ input "H" width	1000 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width, $\overline{Kli}$ input "L" width	1000 ⁽²⁾	—	ns

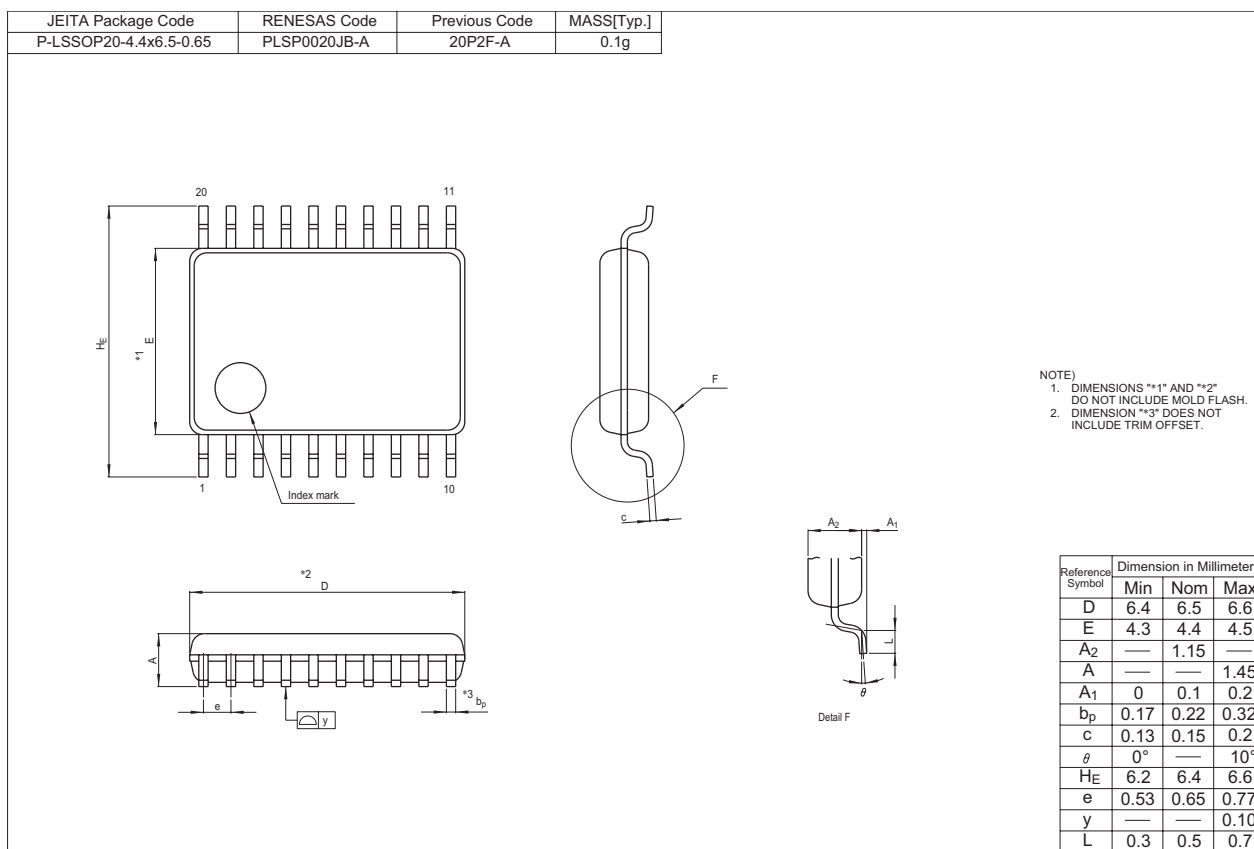
Notes:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

**Figure 5.15 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{Kli}$ when Vcc = 2.2 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/32D Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Feb. 26, 2008	–	First Edition issued
1.00	Feb. 26, 2010	All pages 4 22 to 41	“Preliminary”, “Under development” deleted Table 1.3 revised “5. Electrical Characteristics” added

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