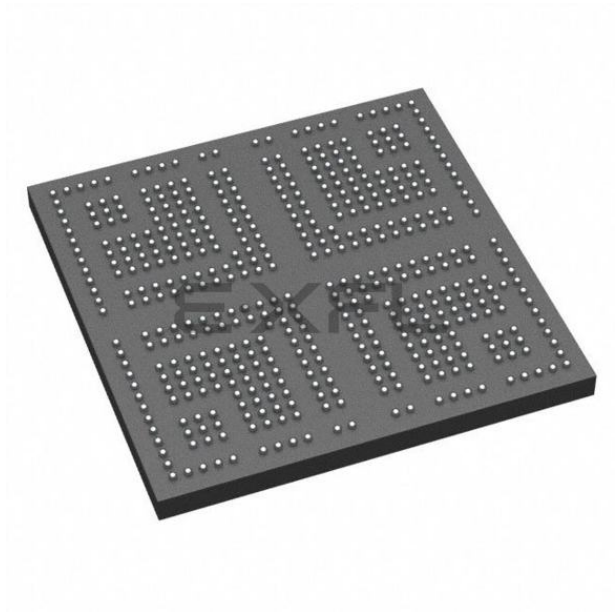


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	56480
Number of Logic Elements/Cells	149500
Total RAM Bits	7880704
Number of I/O	240
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-LFBGA
Supplier Device Package	484-MBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5ceba7m15c7n

Contents

Cyclone V Device Overview

The Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

Related Information

Cyclone V Device Handbook: Known Issues
Lists the planned updates to the Cyclone V Device Handbook chapters.

Key Advantages of Cyclone V Devices

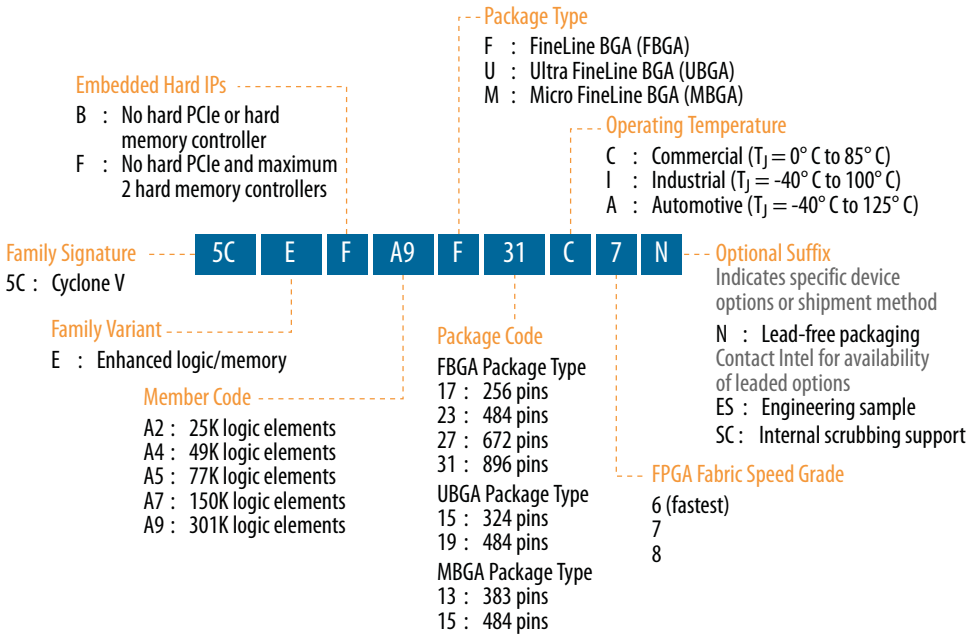
Table 1. Key Advantages of the Cyclone V Device Family

Advantage	Supporting Feature
Lower power consumption	• Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks • Up to 40% lower power consumption than the previous generation device
Improved logic integration and differentiation capabilities	• 8-input adaptive logic module (ALM) • Up to 13.59 megabits (Mb) of embedded memory • Variable-precision digital signal processing (DSP) blocks
Increased bandwidth capacity	• 3.125 gigabits per second (Gbps) and 6.144 Gbps transceivers • Hard memory controllers
Hard processor system (HPS) with integrated Arm* Cortex*-A9 MPCore* processor	• Tight integration of a dual-core Arm Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC) • Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric
Lowest system cost	• Requires only two core voltages to operate • Available in low-cost wirebond packaging • Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration

Available Options

Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Maximum Resources

Table 4. Maximum Resource Counts for Cyclone V E Devices

Resource		Member Code				
		A2	A4	A5	A7	A9
Logic Elements (LE) (K)		25	49	77	150	301
ALM		9,430	18,480	29,080	56,480	113,560
Register		37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860	12,200
	MLAB	196	303	424	836	1,717
Variable-precision DSP Block		25	66	150	156	342
18 x 18 Multiplier		50	132	300	312	684
PLL		4	4	6	7	8
GPIO		224	224	240	480	480
LVDS	Transmitter	56	56	60	120	120
	Receiver	56	56	60	120	120
Hard Memory Controller		1	1	2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 5. Package Plan for Cyclone V E Devices

Member Code	M383 (13 mm)	M484 (15 mm)	U324 (15 mm)	F256 (17 mm)	U484 (19 mm)	F484 (23 mm)	F672 (27 mm)	F896 (31 mm)
	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
A2	223	—	176	128	224	224	—	—
A4	223	—	176	128	224	224	—	—
A5	175	—	—	—	224	240	—	—
A7	—	240	—	—	240	240	336	480
A9	—	—	—	—	240	224	336	480

Cyclone V GX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide
Provides the latest information about Intel products.

Resource		Member Code		
		D5	D7	D9
	Receiver	84	120	140
PCIe Hard IP Block		2	2	2
Hard Memory Controller		2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 9. Package Plan for Cyclone V GT Devices

Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	129	4	175	6	—	—	224	6
D7	—	—	—	—	240	3	240	6
D9	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	240	6	336	6	—	—	—	—
D7	240	6	336	9 (6)	480	9 (6)	—	—
D9	224	6	336	9 (6)	480	12 (7)	560	12 (7)

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

(6) If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

(7) If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

Cyclone V SE

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SE devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

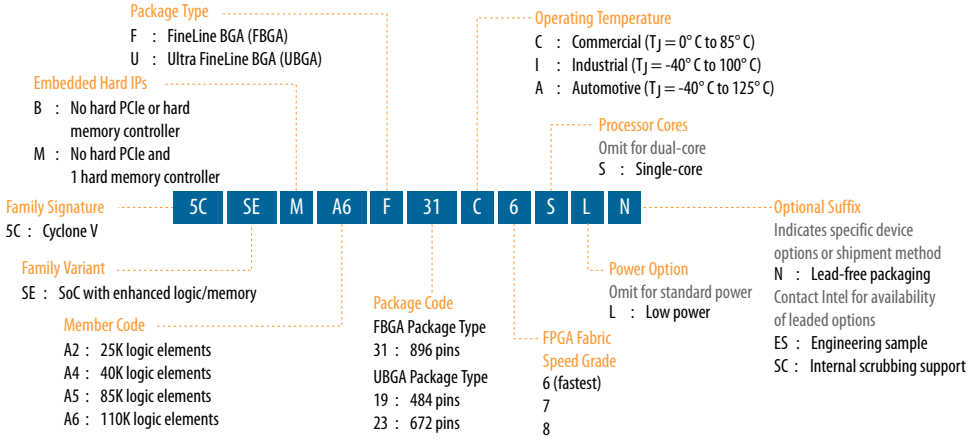
Product Selector Guide
Provides the latest information about Intel products.

Available Options

Figure 4. Sample Ordering Code and Available Options for Cyclone V SE Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



Maximum Resources

Table 10. Maximum Resource Counts for Cyclone V SE Devices

Resource		Member Code			
		A2	A4	A5	A6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,430	15,880	32,070	41,910
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6
HPS PLL		3	3	3	3
FPGA GPIO		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 11. Package Plan for Cyclone V SE Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U484 (19 mm)		U672 (23 mm)		F896 (31 mm)	
	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O
A2	66	151	145	181	—	—
A4	66	151	145	181	—	—
A5	66	151	145	181	288	181
A6	66	151	145	181	288	181

Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

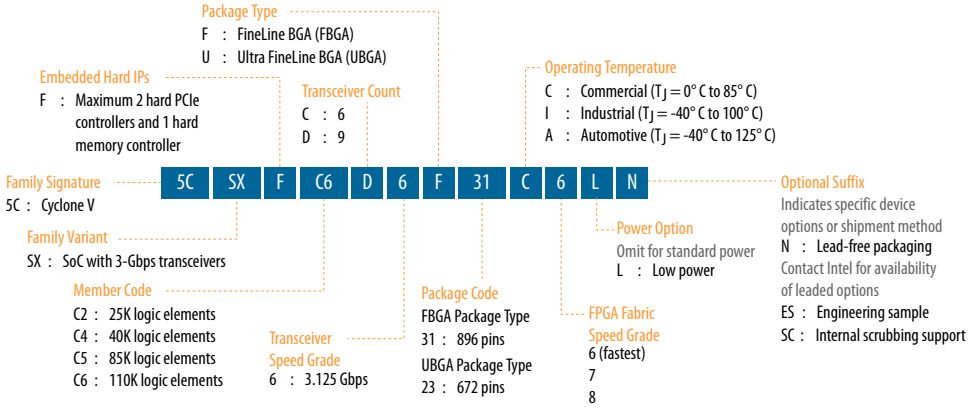
Product Selector Guide
Provides the latest information about Intel products.

Available Options

Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



Maximum Resources

Table 12. Maximum Resource Counts for Cyclone V SX Devices

Resource		Member Code			
		C2	C4	C5	C6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,430	15,880	32,070	41,910
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6

continued...

Resource		Member Code	
		D5	D6
	Receiver	72	72
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		1	1
HPS Hard Memory Controller		1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

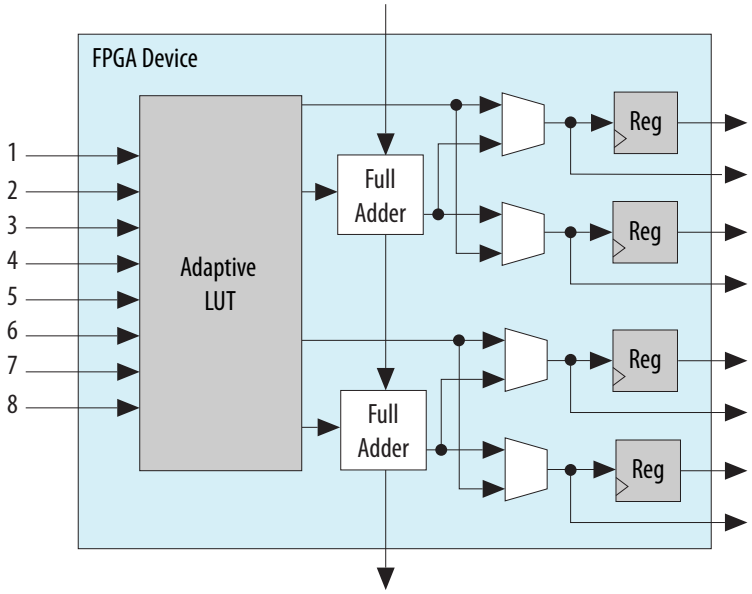
Member Code	F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR
D5	288	181	9 (11)
D6	288	181	9 (11)

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

(11) If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

Figure 8. ALM for Cyclone V Devices



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

Related Information

Embedded Memory Capacity in Cyclone V Devices on page 21
Lists the embedded memory capacity for each device.

Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software

Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters and general DSP usage	Two 18 x 18 with accumulate	1
High precision fixed- or floating-point implementations	One 27 x 27 with accumulate	1

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Table 17. Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier		
Cyclone V E	A2	25	75	50	25	25	25
	A4	66	198	132	66	66	66
	A5	150	450	300	150	150	150
	A7	156	468	312	156	156	156
	A9	342	1,026	684	342	342	342
Cyclone V GX	C3	57	171	114	57	57	57
	C4	70	210	140	70	70	70
	C5	150	450	300	150	150	150
	C7	156	468	312	156	156	156
	C9	342	1,026	684	342	342	342
Cyclone V GT	D5	150	450	300	150	150	150
	D7	156	468	312	156	156	156
	D9	342	1,026	684	342	342	342
Cyclone V SE	A2	36	108	72	36	36	36
	A4	84	252	168	84	84	84
	A5	87	261	174	87	87	87
	A6	112	336	224	112	112	112
Cyclone V SX	C2	36	108	72	36	36	36
	C4	84	252	168	84	84	84
	C5	87	261	174	87	87	87

continued...

Variant	Member Code	M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Cyclone V GT	D5	446	4,460	679	424	4,884
	D7	686	6,860	1338	836	7,696
	D9	1,220	12,200	2748	1,717	13,917
Cyclone V SE	A2	140	1,400	221	138	1,538
	A4	270	2,700	370	231	2,460
	A5	397	3,970	768	480	4,450
	A6	553	5,530	994	621	6,151
Cyclone V SX	C2	140	1,400	221	138	1,538
	C4	270	2,700	370	231	2,460
	C5	397	3,970	768	480	4,450
	C6	553	5,530	994	621	6,151
Cyclone V ST	D5	397	3,970	768	480	4,450
	D6	553	5,530	994	621	6,151

Embedded Memory Configurations

Table 19. Supported Embedded Memory Block Configurations for Cyclone V Devices

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

Clock Networks and PLL Clock Sources

550 MHz Cyclone V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Intel's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

Note: To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

External Memory Performance

Table 20. External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

Interface	Voltage (V)	Maximum Frequency (MHz)		Minimum Frequency (MHz)
		Hard Controller	Soft Controller	
DDR3 SDRAM	1.5	400	303	303
	1.35	400	303	303
DDR2 SDRAM	1.8	400	300	167
LPDDR2 SDRAM	1.2	333	300	167

Related Information

External Memory Interface Spec Estimator
For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 21. HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
LPDDR2 SDRAM	1.2	333

Related Information

External Memory Interface Spec Estimator
For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

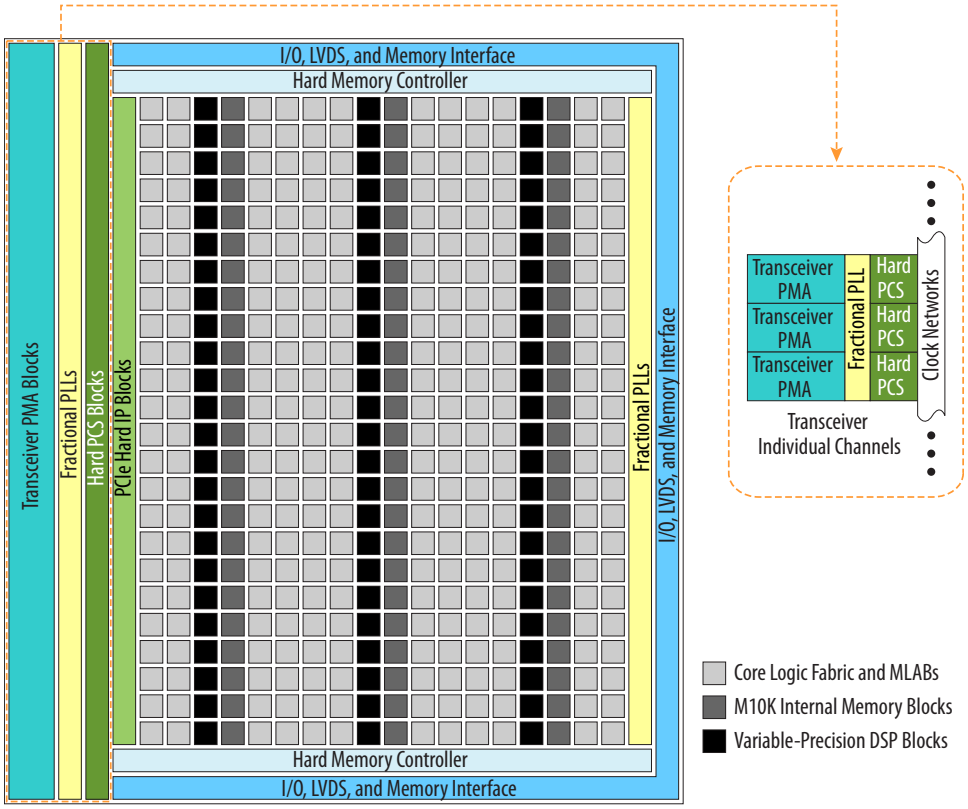
Cyclone V devices deliver the industry’s lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

Figure 10. Device Chip Overview for Cyclone V GX and GT Devices

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.



PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 22. PMA Features of the Transceivers in Cyclone V Devices

Features	Capability
Backplane support	Driving capability up to 6.144 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	• Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization • No decision feedback equalizer (DFE)
Ring oscillator transmit PLLs	614 Mbps to 6.144 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO® (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 6.144 Gbps are supported.

Table 23. Transceiver PCS Features for Cyclone V Devices

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
3-Gbps and 6-Gbps Basic	0.614 to 6.144	• Phase compensation FIFO • Byte serializer • 8B/10B encoder • Transmitter bit-slip	• Word aligner • Deskew FIFO • Rate-match FIFO • 8B/10B decoder • Byte deserializer • Byte ordering • Receiver phase compensation FIFO
PCIe Gen1 (x1, x2, x4)	2.5 and 5.0	• Dedicated PCIe PHY IP core • PIPE 2.0 interface to the core logic	• Dedicated PCIe PHY IP core • PIPE 2.0 interface to the core logic
PCIe Gen2 (x1, x2, x4)(12)			
GbE	1.25	• Custom PHY IP core with preset feature • GbE transmitter synchronization state machine	• Custom PHY IP core with preset feature • GbE receiver synchronization state machine
XAUI (13)	3.125	• Dedicated XAUI PHY IP core • XAUI synchronization state machine for bonding four channels	• Dedicated XAUI PHY IP core • XAUI synchronization state machine for realigning four channels
HiGig	3.75		
SRIO 1.3 and 2.1	1.25 to 3.125	• Custom PHY IP core with preset feature • SRIO version 2.1-compliant x2 and x4 channel bonding	• Custom PHY IP core with preset feature • SRIO version 2.1-compliant x2 and x4 deskew state machine
SDI, SD/HD, and 3G-SDI	0.27(14), 1.485, and 2.97	Custom PHY IP core with preset feature	Custom PHY IP core with preset feature
JESD204A	0.3125(15) to 3.125		

continued...

(12) PCIe Gen2 is supported for Cyclone V GT and ST devices. The PCIe Gen2 x4 support is PCIe-compatible.

(13) XAUI is supported through the soft PCS.

(14) The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

(15) The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature
Serial ATA Gen1 and Gen2	1.5 and 3.0	• Custom PHY IP core with preset feature • Electrical idle	• Custom PHY IP core with preset feature • Signal detect • Wider spread of asynchronous SSC
CPRI 4.1(16)	0.6144 to 6.144	• Dedicated deterministic latency PHY IP core • Transmitter (TX) manual bit-slip mode	• Dedicated deterministic latency PHY IP core • Receiver (RX) deterministic latency state machine
OBSAI RP3	0.768 to 3.072		
V-by-One HS	Up to 3.75	Custom PHY IP core	• Custom PHY IP core • Wider spread of asynchronous SSC
DisplayPort 1.2(17)	1.62 and 2.7		

SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

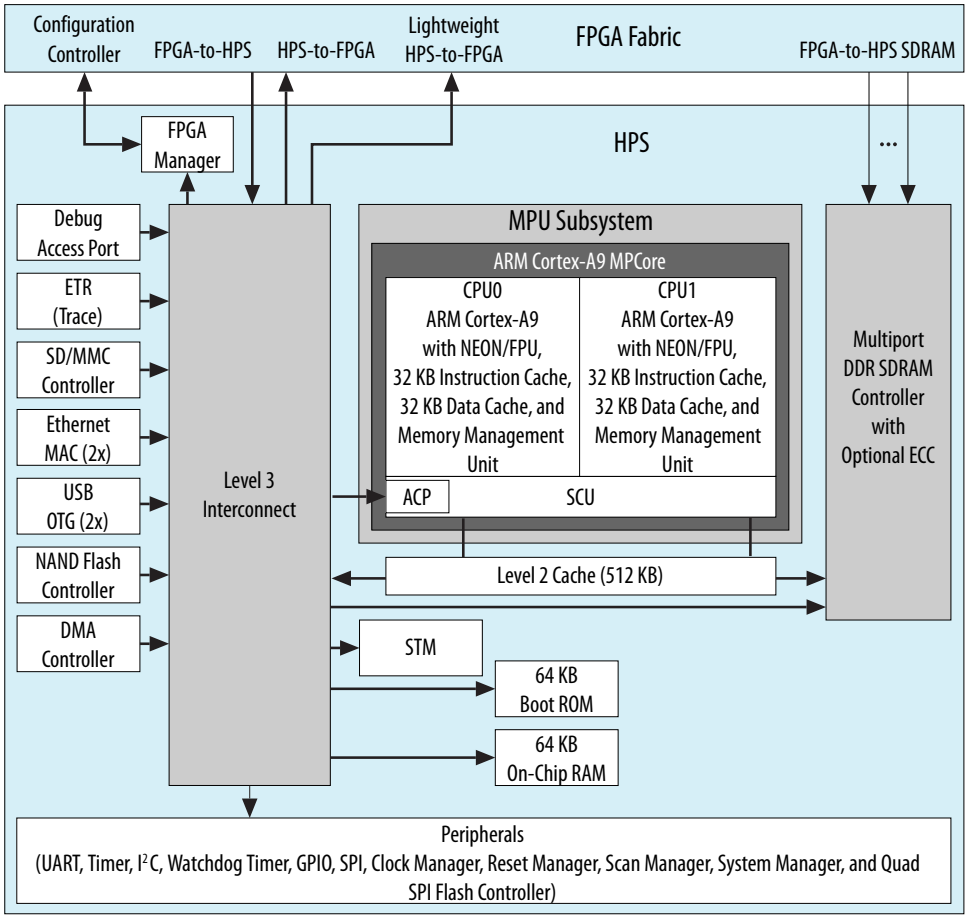
HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

(16) High-voltage output mode (1000-BASE-CX) is not supported.

(17) Pending characterization.

Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor



System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

Document Revision History for Cyclone V Device Overview

Document Version	Changes
2018.05.07	• Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the *Sample Ordering Code and Available Options* diagrams. • Rebranded as Intel.

Date	Version	Changes
December 2017	2017.12.18	• Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices.
June 2016	2016.06.10	Updated Cyclone V GT speed grade to –7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram.
December 2015	2015.12.21	• Added descriptions to package plan tables for Cyclone V GT and ST devices. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.12	• Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives. • Updated logic elements (LE) (K) for the following devices: — Cyclone V E A7: Updated from 149.5 to 150 — Cyclone V GX C3: Updated from 35.5 to 36 — Cyclone V GX C7: Updated from 149.7 to 150 — Cyclone V GT D7: Updated from 149.5 to 150 • Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows: — Cyclone V GX C3: Updated from 291 to 182 — Cyclone V GX C4: Updated from 678 to 424 — Cyclone V GX C5: Updated from 678 to 424 — Cyclone V GX C7: Updated from 1,338 to 836 — Cyclone V GX C9: Updated from 2,748 to 1,717

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Date	Version	Changes
		• Updated HPS I/O for U484 (19 mm) in Table 11 with '151' for A2, A4, A5 and A6. • Updated Memory (Kb) for Maximum Resource Counts for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. • Updated FPGA PLL for Maximum Resource Counts for Cyclone V SE A2, SX C2, devices. • Removed '36 x 36' from the Variable-Precision DSP Block. • Updated Variable-precision DSP Blocks and 18 x 18 Multiplier for Maximum Resource Counts for Cyclone V SX C4 device. • Updated the HPS I/O counts for Cyclone V SE, SX, and ST devices. • Updated Figure 7 which shows the I/O vertical migration table. • Updated Table 17 for Cyclone V SX C4 device. • Updated Embedded Memory Capacity and Distribution table for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. • Removed 'Counter reconfiguration' from the PLL Features. • Updated Low-Power Serial Transceivers by replacing 5 Gbps with 6.144 Gbps. • Removed 'Distributed Memory' symbol. • Updated the Capability in Table 22 of Backplane support to '6.144 Gbps'. • Updated Capability in Table 22 of Ring oscillator transmit PLLs with 6.144 Gbps. • Updated the PCS Support in Table 23 from 5 Gbps to '6 Gbps'. • Updated the Data Rates (Gbps) in Table 23 of 3 Gbps and 6 Gbps Basic to '6.144 Gbps'. • Updated the Data Rates (Gbps) in Table 23 of CPRI 4.1 to '6.144 Gbps'. • Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.
December 2012	2012.12.28	• Updated the pin counts for the MBGA packages. • Updated the GPIO and transceiver counts for the MBGA packages. • Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices. • Updated the vertical migration table for vertical migration of the U484 packages. • Updated the MLAB supported programmable widths at 32 bits depth.
November 2012	2012.11.19	• Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT. • Added ordering code for five-transceiver devices for Cyclone V GT and ST. • Updated the vertical migration table to add MBGA packages. • Added performance information for HPS memory controller. • Removed DDR3U support. • Updated Cyclone V ST speed grade information. • Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance. • Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software. • Updated template.
July 2012	2.1	Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible)
June 2012	2.0	• Restructured the document. • Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections. • Added Table 1, Table 3, Table 16, Table 19, and Table 20. • Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18.

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		• Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10. • Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. • Text edits throughout the document.
February 2012	1.2	• Updated Table 1–2, Table 1–3, and Table 1–6. • Updated "Cyclone V Family Plan" on page 1–4 and "Clock Networks and PLL Clock Sources" on page 1–15. • Updated Figure 1–1 and Figure 1–6.
November 2011	1.1	• Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6. • Updated Figure 1–4, Figure 1–5, Figure 1–6, Figure 1–7, and Figure 1–8. • Updated "System Peripherals" on page 1–18, "HPS–FPGA AXI Bridges" on page 1–19, "HPS SDRAM Controller Subsystem" on page 1–19, "FPGA Configuration and Processor Booting" on page 1–19, and "Hardware and Software Development" on page 1–20. • Minor text edits.
October 2011	1.0	Initial release.