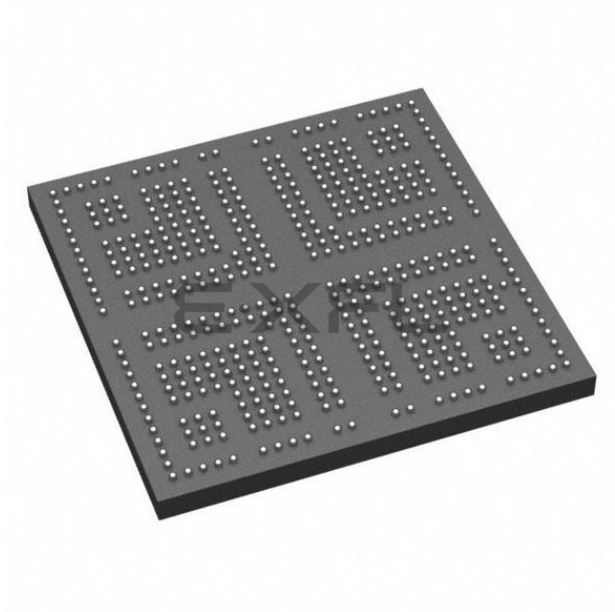


**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 56480 |
| Number of Logic Elements/Cells | 149500 |
| Total RAM Bits | 7880704 |
| Number of I/O | 240 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-LFBGA |
| Supplier Device Package | 484-MBGA (15x15) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5ceba7m15c8n |

# Summary of Cyclone V Features

## Table 2. Summary of Features for Cyclone V Devices

| Feature | Description | |
|---|---|---|
| Technology | • TSMC's 28-nm low-power (28LP) process technology<br>• 1.1 V core voltage | |
| Packaging | • Wirebond low-halogen packages<br>• Multiple device densities with compatible package footprints for seamless migration between different device densities<br>• RoHS-compliant and leaded(1) options | |
| High-performance FPGA fabric | Enhanced 8-input ALM with four registers | |
| Internal memory blocks | • M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC)<br>• Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory | |
| Embedded Hard IP blocks | Variable-precision DSP | • Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block<br>• 64-bit accumulator and cascade<br>• Embedded internal coefficient memory<br>• Preadder/subtractor for improved efficiency |
| | Memory controller | DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support |
| | Embedded transceiver I/O | PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port |
| Clock networks | • Up to 550 MHz global clock network<br>• Global, quadrant, and peripheral clock networks<br>• Clock networks that are not used can be powered down to reduce dynamic power | |
| Phase-locked loops (PLLs) | • Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)<br>• Integer mode and fractional mode | |
| FPGA General-purpose I/Os (GPIOs) | • 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter<br>• 400 MHz/800 Mbps external memory interface<br>• On-chip termination (OCT)<br>• 3.3 V support with up to 16 mA drive strength | |
| Low-power high-speed serial interface | • 614 Mbps to 6.144 Gbps integrated transceiver speed<br>• Transmit pre-emphasis and receiver equalization<br>• Dynamic partial reconfiguration of individual channels | |
| HPS (Cyclone V SE, SX, and ST devices only) | • Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing<br>• Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), $I^2C$ interface, and up to 85 HPS GPIO interfaces<br>• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers<br>• On-chip RAM and boot ROM | |

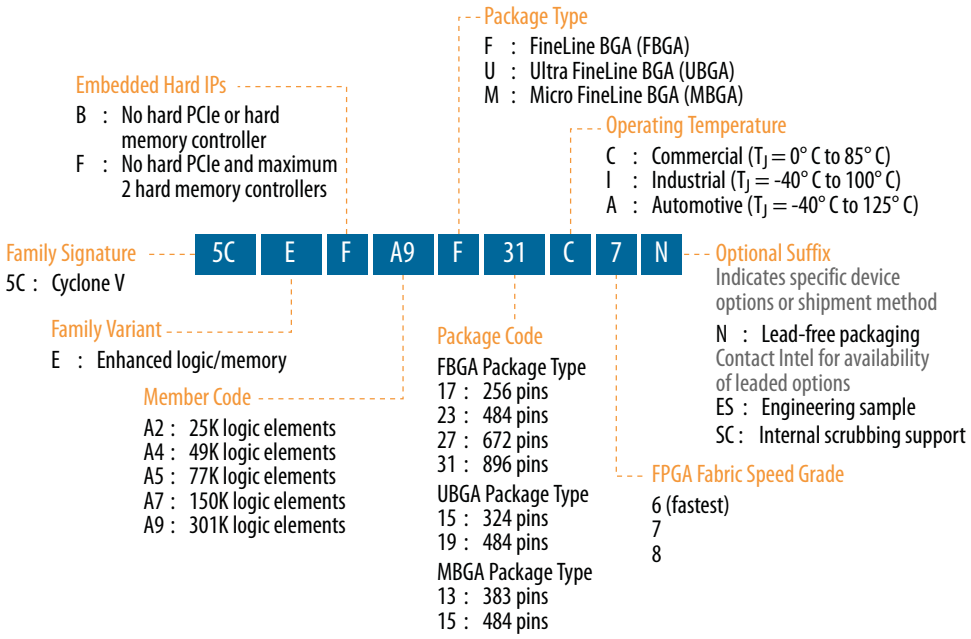
***continued...***

(1) Contact Intel for availability.

## Available Options

### Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.




## Maximum Resources

### Table 4. Maximum Resource Counts for Cyclone V E Devices

| Resource | | Member Code | | | | |
|---|---|---|---|---|---|---|
| | | A2 | A4 | A5 | A7 | A9 |
| Logic Elements (LE) (K) | | 25 | 49 | 77 | 150 | 301 |
| ALM | | 9,430 | 18,480 | 29,080 | 56,480 | 113,560 |
| Register | | 37,736 | 73,920 | 116,320 | 225,920 | 454,240 |
| Memory (Kb) | M10K | 1,760 | 3,080 | 4,460 | 6,860 | 12,200 |
| | MLAB | 196 | 303 | 424 | 836 | 1,717 |
| Variable-precision DSP Block | | 25 | 66 | 150 | 156 | 342 |
| 18 x 18 Multiplier | | 50 | 132 | 300 | 312 | 684 |
| PLL | | 4 | 4 | 6 | 7 | 8 |
| GPIO | | 224 | 224 | 240 | 480 | 480 |
| LVDS | Transmitter | 56 | 56 | 60 | 120 | 120 |
| | Receiver | 56 | 56 | 60 | 120 | 120 |
| Hard Memory Controller | | 1 | 1 | 2 | 2 | 2 |

| Resource | | Member Code | | | | |
|---|---|---|---|---|---|---|
| | | C3 | C4 | C5 | C7 | C9 |
| LVDS | Transmitter | 52 | 84 | 84 | 120 | 140 |
| | Receiver | 52 | 84 | 84 | 120 | 140 |
| PCIe Hard IP Block | | 1 | 2 | 2 | 2 | 2 |
| Hard Memory Controller | | 1 | 2 | 2 | 2 | 2 |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 7. Package Plan for Cyclone V GX Devices

| Member Code | M301 (11 mm) | | M383 (13 mm) | | M484 (15 mm) | | U324 (15 mm) | | U484 (19 mm) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| C3 | — | — | — | — | — | — | 144 | 3 | 208 | 3 |
| C4 | 129 | 4 | 175 | 6 | — | — | — | — | 224 | 6 |
| C5 | 129 | 4 | 175 | 6 | — | — | — | — | 224 | 6 |
| C7 | — | — | — | — | 240 | 3 | — | — | 240 | 6 |
| C9 | — | — | — | — | — | — | — | — | 240 | 5 |

| Member Code | F484 (23 mm) | | F672 (27 mm) | | F896 (31 mm) | | F1152 (35 mm) | |
|---|---|---|---|---|---|---|---|---|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| C3 | 208 | 3 | — | — | — | — | — | — |
| C4 | 240 | 6 | 336 | 6 | — | — | — | — |
| C5 | 240 | 6 | 336 | 6 | — | — | — | — |
| C7 | 240 | 6 | 336 | 9 | 480 | 9 | — | — |
| C9 | 224 | 6 | 336 | 9 | 480 | 12 | 560 | 12 |

# Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

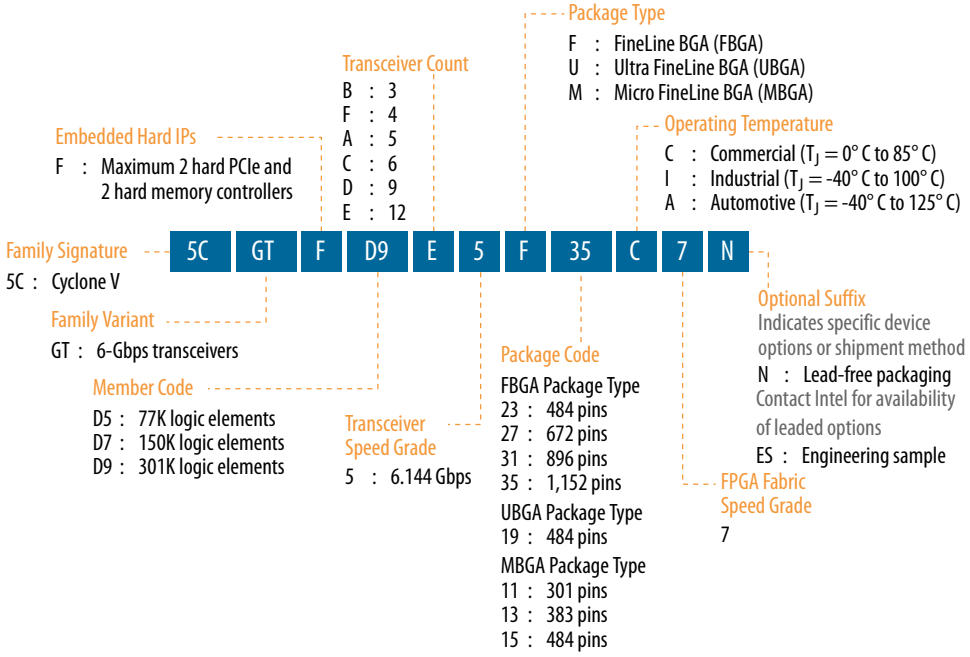
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

Product Selector Guide
Provides the latest information about Intel products.

## Available Options

### Figure 3. Sample Ordering Code and Available Options for Cyclone V GT Devices




## Maximum Resources

### Table 8. Maximum Resource Counts for Cyclone V GT Devices

| Resource | | Member Code | | |
|---|---|---|---|---|
| | | D5 | D7 | D9 |
| Logic Elements (LE) (K) | | 77 | 150 | 301 |
| ALM | | 29,080 | 56,480 | 113,560 |
| Register | | 116,320 | 225,920 | 454,240 |
| Memory (Kb) | M10K | 4,460 | 6,860 | 12,200 |
| | MLAB | 424 | 836 | 1,717 |
| Variable-precision DSP Block | | 150 | 156 | 342 |
| 18 x 18 Multiplier | | 300 | 312 | 684 |
| PLL | | 6 | 7 | 8 |
| 6 Gbps Transceiver | | 6 | 9 | 12 |
| GPIO(5) | | 336 | 480 | 560 |
| LVDS | Transmitter | 84 | 120 | 140 |

continued...

(5) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

| Resource | | Member Code | | |
|---|---|---|---|---|
| | | D5 | D7 | D9 |
| | Receiver | 84 | 120 | 140 |
| PCIe Hard IP Block | | 2 | 2 | 2 |
| Hard Memory Controller | | 2 | 2 | 2 |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 9. Package Plan for Cyclone V GT Devices

Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

| Member Code | M301 (11 mm) | | M383 (13 mm) | | M484 (15 mm) | | U484 (19 mm) | |
|---|---|---|---|---|---|---|---|---|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| D5 | 129 | 4 | 175 | 6 | — | — | 224 | 6 |
| D7 | — | — | — | — | 240 | 3 | 240 | 6 |
| D9 | — | — | — | — | — | — | 240 | 5 |

| Member Code | F484 (23 mm) | | F672 (27 mm) | | F896 (31 mm) | | F1152 (35 mm) | |
|---|---|---|---|---|---|---|---|---|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| D5 | 240 | 6 | 336 | 6 | — | — | — | — |
| D7 | 240 | 6 | 336 | 9 (6) | 480 | 9 (6) | — | — |
| D9 | 224 | 6 | 336 | 9 (6) | 480 | 12 (7) | 560 | 12 (7) |

### Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

(6) If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

(7) If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

# Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

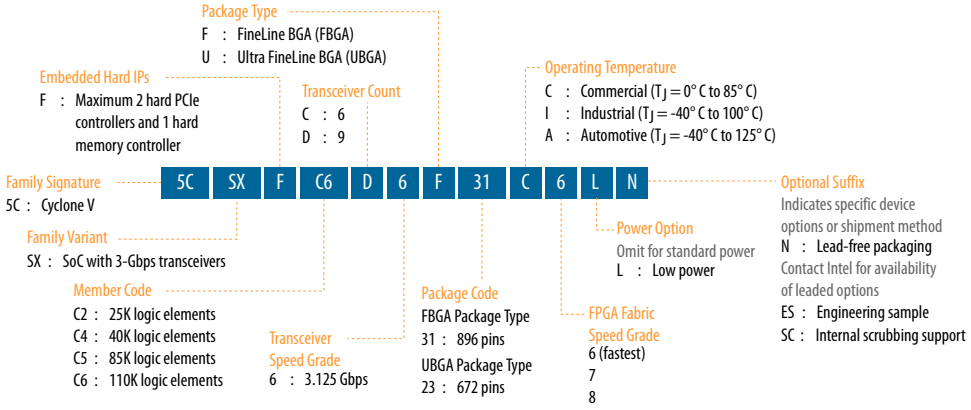
Product Selector Guide
Provides the latest information about Intel products.

## Available Options

### Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.




## Maximum Resources

### Table 12. Maximum Resource Counts for Cyclone V SX Devices

| Resource | | Member Code | | | |
|---|---|---|---|---|---|
| | | C2 | C4 | C5 | C6 |
| Logic Elements (LE) (K) | | 25 | 40 | 85 | 110 |
| ALM | | 9,430 | 15,880 | 32,070 | 41,910 |
| Register | | 37,736 | 60,376 | 128,300 | 166,036 |
| Memory (Kb) | M10K | 1,400 | 2,700 | 3,970 | 5,570 |
| | MLAB | 138 | 231 | 480 | 621 |
| Variable-precision DSP Block | | 36 | 84 | 87 | 112 |
| 18 x 18 Multiplier | | 72 | 168 | 174 | 224 |
| FPGA PLL | | 5 | 5 | 6 | 6 |

*continued...*

| Resource | | Member Code | | | |
|---|---|---|---|---|---|
| | | C2 | C4 | C5 | C6 |
| HPS PLL | | 3 | 3 | 3 | 3 |
| 3 Gbps Transceiver | | 6 | 6 | 9 | 9 |
| FPGA GPIO (8) | | 145 | 145 | 288 | 288 |
| HPS I/O | | 181 | 181 | 181 | 181 |
| LVDS | Transmitter | 32 | 32 | 72 | 72 |
| | Receiver | 37 | 37 | 72 | 72 |
| PCIe Hard IP Block | | 2 | 2 | 2 (9) | 2 (9) |
| FPGA Hard Memory Controller | | 1 | 1 | 1 | 1 |
| HPS Hard Memory Controller | | 1 | 1 | 1 | 1 |
| Arm Cortex-A9 MPCore Processor | | Dual-core | Dual-core | Dual-core | Dual-core |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 13. Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

| Member Code | U672 (23 mm) | | | F896 (31 mm) | | |
|---|---|---|---|---|---|---|
| | FPGA GPIO | HPS I/O | XCVR | FPGA GPIO | HPS I/O | XCVR |
| C2 | 145 | 181 | 6 | — | — | — |
| C4 | 145 | 181 | 6 | — | — | — |
| C5 | 145 | 181 | 6 | 288 | 181 | 9 |
| C6 | 145 | 181 | 6 | 288 | 181 | 9 |

# Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

(8) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

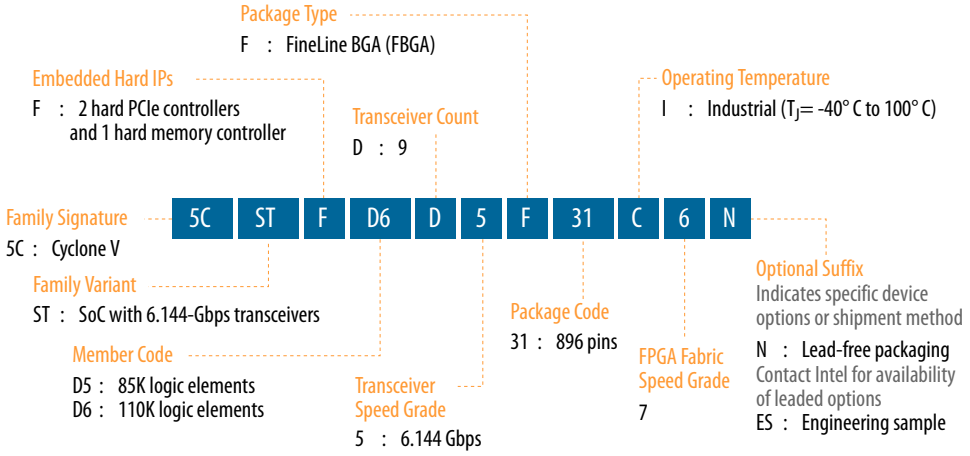
(9) 1 PCIe Hard IP Block in U672 package.

### Related Information

Product Selector Guide
Provides the latest information about Intel products.

## Available Options

### Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices




## Maximum Resources

### Table 14. Maximum Resource Counts for Cyclone V ST Devices

| Resource | | Member Code | |
|---|---|---|---|
| | | D5 | D6 |
| Logic Elements (LE) (K) | | 85 | 110 |
| ALM | | 32,070 | 41,910 |
| Register | | 128,300 | 166,036 |
| Memory (Kb) | M10K | 3,970 | 5,570 |
| | MLAB | 480 | 621 |
| Variable-precision DSP Block | | 87 | 112 |
| 18 x 18 Multiplier | | 174 | 224 |
| FPGA PLL | | 6 | 6 |
| HPS PLL | | 3 | 3 |
| 6.144 Gbps Transceiver | | 9 | 9 |
| FPGA GPIO(10) | | 288 | 288 |
| HPS I/O | | 181 | 181 |
| LVDS | Transmitter | 72 | 72 |

continued...

(10) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

| Resource | | Member Code | |
|---|---|---|---|
| | | D5 | D6 |
| | Receiver | 72 | 72 |
| PCIe Hard IP Block | | 2 | 2 |
| FPGA Hard Memory Controller | | 1 | 1 |
| HPS Hard Memory Controller | | 1 | 1 |
| Arm Cortex-A9 MPCore Processor | | Dual-core | Dual-core |

### Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

## Package Plan

### Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

| Member Code | F896 (31 mm) | | |
|---|---|---|---|
| | FPGA GPIO | HPS I/O | XCVR |
| D5 | 288 | 181 | 9 (11) |
| D6 | 288 | 181 | 9 (11) |

### Related Information

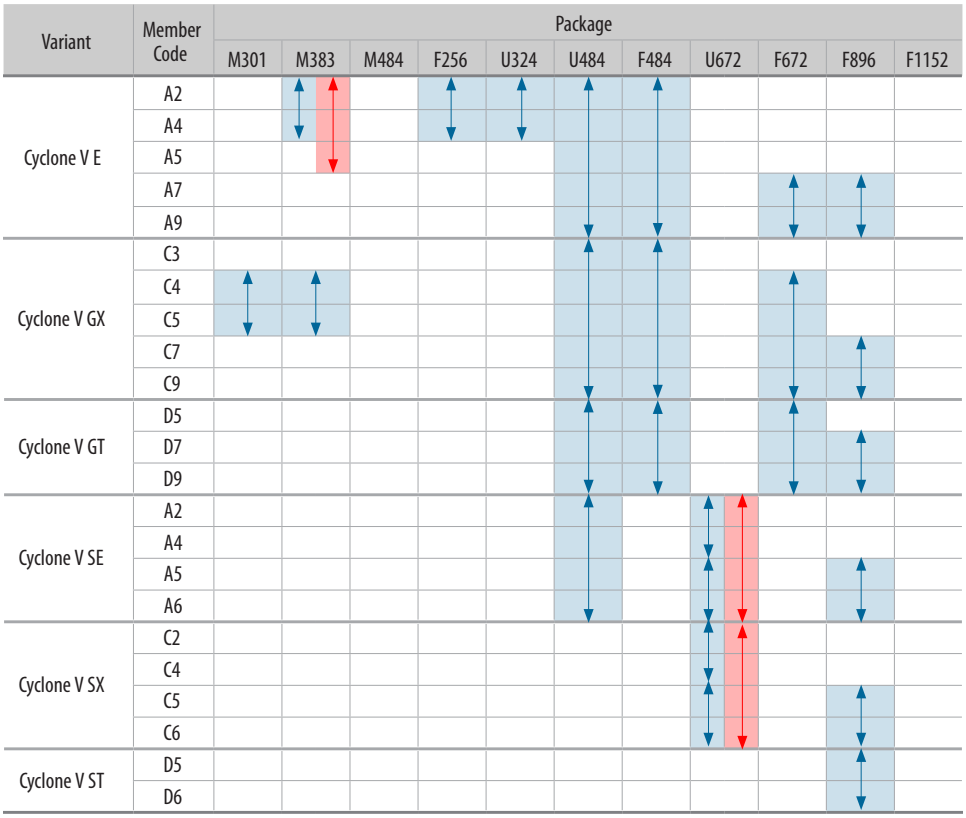
6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

(11) If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

# I/O Vertical Migration for Cyclone V Devices

**Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities**

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.




You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

*Note:* To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

# Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

### Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices

| Usage Example | Multiplier Size (Bit) | DSP Block Resource |
|---|---|---|
| Low precision fixed point for video applications | Three 9 x 9 | 1 |
| Medium precision fixed point in FIR filters | Two 18 x 18 | 1 |
| FIR filters and general DSP usage | Two 18 x 18 with accumulate | 1 |
| High precision fixed- or floating-point implementations | One 27 x 27 with accumulate | 1 |

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

### Table 17. Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

| Variant | Member Code | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | | 18 x 18 Multiplier Adder Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---|---|---|---|---|---|---|---|
| | | | 9 x 9 Multiplier | 18 x 18 Multiplier | 27 x 27 Multiplier | | |
| Cyclone V E | A2 | 25 | 75 | 50 | 25 | 25 | 25 |
| | A4 | 66 | 198 | 132 | 66 | 66 | 66 |
| | A5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | A7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | A9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V GX | C3 | 57 | 171 | 114 | 57 | 57 | 57 |
| | C4 | 70 | 210 | 140 | 70 | 70 | 70 |
| | C5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | C7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | C9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V GT | D5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | D7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | D9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V SE | A2 | 36 | 108 | 72 | 36 | 36 | 36 |
| | A4 | 84 | 252 | 168 | 84 | 84 | 84 |
| | A5 | 87 | 261 | 174 | 87 | 87 | 87 |
| | A6 | 112 | 336 | 224 | 112 | 112 | 112 |
| Cyclone V SX | C2 | 36 | 108 | 72 | 36 | 36 | 36 |
| | C4 | 84 | 252 | 168 | 84 | 84 | 84 |
| | C5 | 87 | 261 | 174 | 87 | 87 | 87 |

*continued...*

| Variant | Member Code | M10K | | MLAB | | Total RAM Bit (Kb) |
|---|---|---|---|---|---|---|
| | | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) | |
| Cyclone V GT | D5 | 446 | 4,460 | 679 | 424 | 4,884 |
| | D7 | 686 | 6,860 | 1338 | 836 | 7,696 |
| | D9 | 1,220 | 12,200 | 2748 | 1,717 | 13,917 |
| Cyclone V SE | A2 | 140 | 1,400 | 221 | 138 | 1,538 |
| | A4 | 270 | 2,700 | 370 | 231 | 2,460 |
| | A5 | 397 | 3,970 | 768 | 480 | 4,450 |
| | A6 | 553 | 5,530 | 994 | 621 | 6,151 |
| Cyclone V SX | C2 | 140 | 1,400 | 221 | 138 | 1,538 |
| | C4 | 270 | 2,700 | 370 | 231 | 2,460 |
| | C5 | 397 | 3,970 | 768 | 480 | 4,450 |
| | C6 | 553 | 5,530 | 994 | 621 | 6,151 |
| Cyclone V ST | D5 | 397 | 3,970 | 768 | 480 | 4,450 |
| | D6 | 553 | 5,530 | 994 | 621 | 6,151 |

## Embedded Memory Configurations

### Table 19. Supported Embedded Memory Block Configurations for Cyclone V Devices

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

| Memory Block | Depth (bits) | Programmable Width |
|---|---|---|
| MLAB | 32 | x16, x18, or x20 |
| M10K | 256 | x40 or x32 |
| | 512 | x20 or x16 |
| | 1K | x10 or x8 |
| | 2K | x5 or x4 |
| | 4K | x2 |
| | 8K | x1 |

## Clock Networks and PLL Clock Sources

550 MHz Cyclone V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Intel's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

*Note:* To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

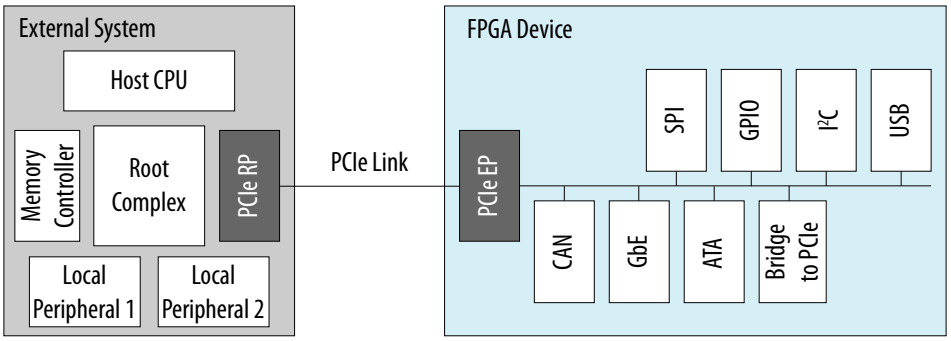
## PCIe Gen1 and Gen2 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen2 and Gen1 end point and root port for up to x4 lane configuration. The PCIe Gen2 x4 support is PCIe-compatible.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

**Figure 9. PCIe Multifunction for Cyclone V Devices**




The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

## External Memory Interface

This section provides an overview of the external memory interface in Cyclone V devices.

## Hard and Soft Memory Controllers

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Cyclone V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Cyclone V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices for maximum flexibility.

## External Memory Performance

### Table 20. External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

| Interface | Voltage (V) | Maximum Frequency (MHz) | | Minimum Frequency (MHz) |
|---|---|---|---|---|
| | | Hard Controller | Soft Controller | |
| DDR3 SDRAM | 1.5 | 400 | 303 | 303 |
| | 1.35 | 400 | 303 | 303 |
| DDR2 SDRAM | 1.8 | 400 | 300 | 167 |
| LPDDR2 SDRAM | 1.2 | 333 | 300 | 167 |

#### Related Information

External Memory Interface Spec Estimator
For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

## HPS External Memory Performance

### Table 21. HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

| Interface | Voltage (V) | HPS Hard Controller (MHz) |
|---|---|---|
| DDR3 SDRAM | 1.5 | 400 |
| | 1.35 | 400 |
| DDR2 SDRAM | 1.8 | 400 |
| LPDDR2 SDRAM | 1.2 | 333 |

#### Related Information

External Memory Interface Spec Estimator
For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

## Low-Power Serial Transceivers

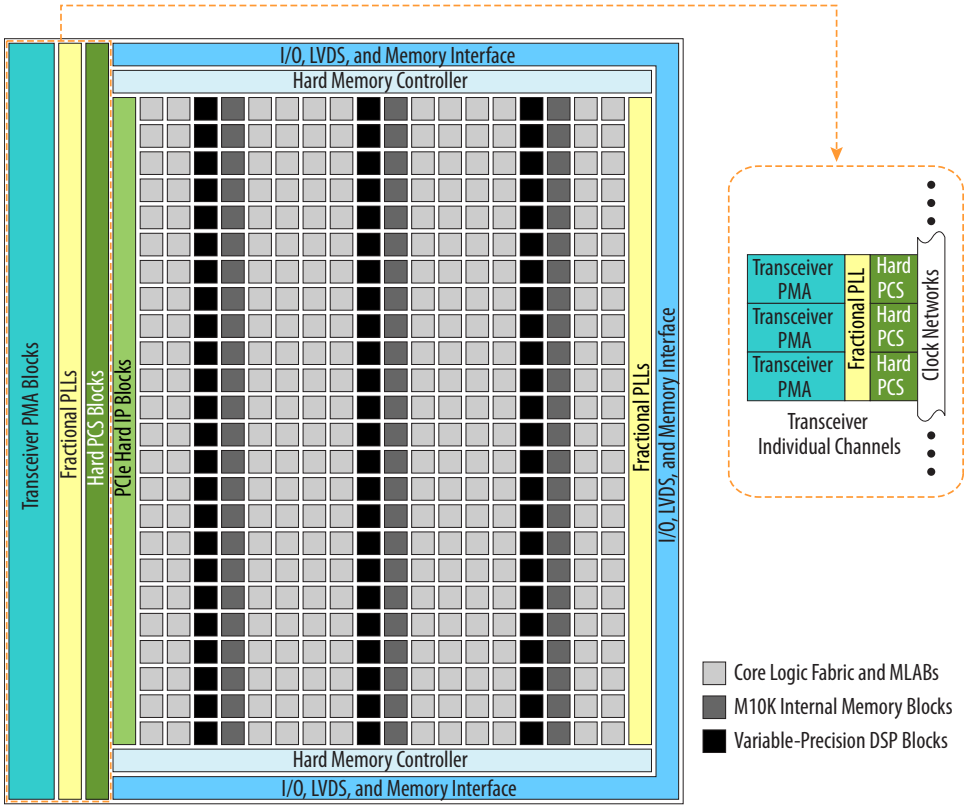
Cyclone V devices deliver the industry’s lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

## Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

**Figure 10. Device Chip Overview for Cyclone V GX and GT Devices**

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.




## PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

**Table 22. PMA Features of the Transceivers in Cyclone V Devices**

| Features | Capability |
|---|---|
| Backplane support | Driving capability up to 6.144 Gbps |
| PLL-based clock recovery | Superior jitter tolerance |
| Programmable deserialization and word alignment | Flexible deserialization width and configurable word alignment pattern |
| Equalization and pre-emphasis | • Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization<br>• No decision feedback equalizer (DFE) |
| Ring oscillator transmit PLLs | 614 Mbps to 6.144 Gbps |
| Input reference clock range | 20 MHz to 400 MHz |
| Transceiver dynamic reconfiguration | Allows the reconfiguration of a single channel without affecting the operation of other channels |

| PCS Support | Data Rates (Gbps) | Transmitter Data Path Feature | Receiver Data Path Feature |
|---|---|---|---|
| Serial ATA Gen1 and Gen2 | 1.5 and 3.0 | • Custom PHY IP core with preset feature<br>• Electrical idle | • Custom PHY IP core with preset feature<br>• Signal detect<br>• Wider spread of asynchronous SSC |
| CPRI 4.1(16) | 0.6144 to 6.144 | • Dedicated deterministic latency PHY IP core<br>• Transmitter (TX) manual bit-slip mode | • Dedicated deterministic latency PHY IP core<br>• Receiver (RX) deterministic latency state machine |
| OBSAI RP3 | 0.768 to 3.072 | | |
| V-by-One HS | Up to 3.75 | Custom PHY IP core | • Custom PHY IP core<br>• Wider spread of asynchronous SSC |
| DisplayPort 1.2(17) | 1.62 and 2.7 | | |

## SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

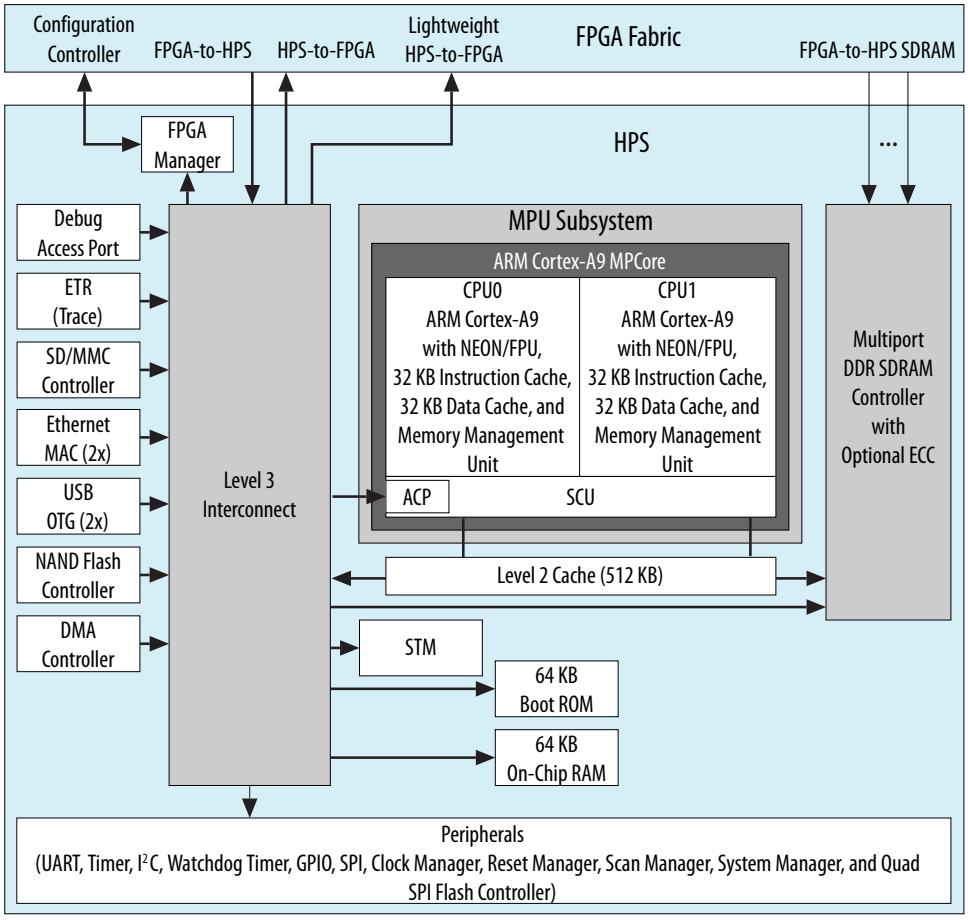
## HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

(16) High-voltage output mode (1000-BASE-CX) is not supported.

(17) Pending characterization.

**Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor**




## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.

## HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 400 MHz (800 Mbps data rate).

# FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

## Document Revision History for Cyclone V Device Overview

| Document Version | Changes |
|---|---|
| 2018.05.07 | • Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the *Sample Ordering Code and Available Options* diagrams.<br>• Rebranded as Intel. |

| Date | Version | Changes |
|---|---|---|
| December 2017 | 2017.12.18 | • Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices. |
| June 2016 | 2016.06.10 | Updated Cyclone V GT speed grade to –7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram. |
| December 2015 | 2015.12.21 | • Added descriptions to package plan tables for Cyclone V GT and ST devices.<br>• Changed instances of *Quartus II* to *Quartus Prime*. |
| June 2015 | 2015.06.12 | • Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives.<br>• Updated logic elements (LE) (K) for the following devices:<br>— Cyclone V E A7: Updated from 149.5 to 150<br>— Cyclone V GX C3: Updated from 35.5 to 36<br>— Cyclone V GX C7: Updated from 149.7 to 150<br>— Cyclone V GT D7: Updated from 149.5 to 150<br>• Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows:<br>— Cyclone V GX C3: Updated from 291 to 182<br>— Cyclone V GX C4: Updated from 678 to 424<br>— Cyclone V GX C5: Updated from 678 to 424<br>— Cyclone V GX C7: Updated from 1,338 to 836<br>— Cyclone V GX C9: Updated from 2,748 to 1,717 |

***continued...***

| Date | Version | Changes |
|---|---|---|
| | | • Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10.<br>• Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections.<br>• Text edits throughout the document. |
| February 2012 | 1.2 | • Updated Table 1–2, Table 1–3, and Table 1–6.<br>• Updated "Cyclone V Family Plan" on page 1–4 and "Clock Networks and PLL Clock Sources" on page 1–15.<br>• Updated Figure 1–1 and Figure 1–6. |
| November 2011 | 1.1 | • Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6.<br>• Updated Figure 1–4, Figure 1–5, Figure 1–6, Figure 1–7, and Figure 1–8.<br>• Updated "System Peripherals" on page 1–18, "HPS–FPGA AXI Bridges" on page 1–19, "HPS SDRAM Controller Subsystem" on page 1–19, "FPGA Configuration and Processor Booting" on page 1–19, and "Hardware and Software Development" on page 1–20.<br>• Minor text edits. |
| October 2011 | 1.0 | Initial release. |