Intel - 5CEFA7F23C7N Datasheet





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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	56480
Number of Logic Elements/Cells	149500
Total RAM Bits	7880704
Number of I/O	240
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cefa7f23c7n

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Summary of Cyclone V Features

Table 2. Summary of Features for Cyclone V Devices

Feature		Description				
Technology	 TSMC's 28-nm low-p 1.1 V core voltage 	ower (28LP) process technology				
Packaging	 Wirebond low-haloge Multiple device densi different device dens RoHS-compliant and 	Wirebond low-halogen packages Multiple device densities with compatible package footprints for seamless migration between different device densities RoHS-compliant and leaded ⁽¹⁾ options				
High-performance FPGA fabric	Enhanced 8-input ALM v	nhanced 8-input ALM with four registers				
Internal memory blocks	 M10K—10-kilobits (K Memory logic array to of the ALMs as MLAB 	 M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory 				
Embedded Hard IP blocks	Variable-precision DSP	 Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block 64-bit accumulator and cascade Embedded internal coefficient memory Preadder/subtractor for improved efficiency 				
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support				
	Embedded transceiver I/O	PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port				
Clock networks	 Up to 550 MHz globa Global, quadrant, an Clock networks that 	Il clock network d peripheral clock networks are not used can be powered down to reduce dynamic power				
Phase-locked loops (PLLs)	Precision clock synthInteger mode and frame	esis, clock delay compensation, and zero delay buffering (ZDB) actional mode				
FPGA General-purpose I/Os (GPIOs)	 875 megabits per se 400 MHz/800 Mbps e On-chip termination 3.3 V support with u 	cond (Mbps) LVDS receiver and 840 Mbps LVDS transmitter external memory interface (OCT) p to 16 mA drive strength				
Low-power high-speed serial interface	 614 Mbps to 6.144 Gbps integrated transceiver speed Transmit pre-emphasis and receiver equalization Dynamic partial reconfiguration of individual channels 					
HPS (Cyclone V SE, SX, and ST devices only)	 Single or dual-core A support for symmetr Interface peripherals On-The-GO (OTG) conflash controller, Secunetwork (CAN), seria interfaces System peripherals-controller, FPGA conf On-chip RAM and bo 	Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with ic and asymmetric multiprocessing 5—10/100/1000 Ethernet media access control (EMAC), USB 2.0 ontroller, quad serial peripheral interface (QSPI) flash controller, NAND ire Digital/MultiMediaCard (SD/MMC) controller, UART, controller area al peripheral interface (SPI), I ² C interface, and up to 85 HPS GPIO -general-purpose timers, watchdog timers, direct memory access (DMA) figuration manager, and clock and reset managers ot ROM				
		continued				

⁽¹⁾ Contact Intel for availability.



Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices Provides the number of LVDS channels in each device package.

Package Plan

Table 5. Package Plan for Cyclone V E Devices

Member Code	M383 (13 mm)	M484 (15 mm)	U324 (15 mm)	F256 (17 mm)	U484 (19 mm)	F484 (23 mm)	F672 (27 mm)	F896 (31 mm)
	GPIO							
A2	223	_	176	128	224	224	_	_
A4	223	—	176	128	224	224	_	—
A5	175	_	_	_	224	240	_	_
A7	_	240	_	_	240	240	336	480
A9	_	_	_	_	240	224	336	480

Cyclone V GX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide

Provides the latest information about Intel products.



Available Options

Figure 2. Sample Ordering Code and Available Options for Cyclone V GX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Maximum Resources

Table 6. Maximum Resource Counts for Cyclone V GX Devices

Resource		Member Code						
		C3	C4	C5	C7	С9		
Logic Elements	(LE) (K)	36	50	77	150	301		
ALM		13,460	18,860	29,080	56,480	113,560		
Register	Register		75,440	116,320	225,920	454,240		
Memory (Kb)	M10K	1,350	2,500	4,460	6,860	12,200		
	MLAB	182	424	424	836	1,717		
Variable-precisio	on DSP Block	57	70	150	156	342		
18 x 18 Multiplie	er	114	140	300	312	684		
PLL		4	6	6	7	8		
3 Gbps Transceiver		3	6	6	9	12		
GPIO ⁽⁴⁾		208	336	336	480	560		
						continued		

⁽⁴⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus[®] Prime software, the number of user I/Os includes transceiver I/Os.



Available Options

Figure 3. Sample Ordering Code and Available Options for Cyclone V GT Devices



Maximum Resources

Table 8. Maximum Resource Counts for Cyclone V GT Devices

R	esource	Member Code				
		D5	D7	D9		
Logic Elements (LE) (K)		77	150	301		
ALM		29,080	56,480	113,560		
Register		116,320	225,920	454,240		
Memory (Kb)	M10K	4,460	6,860	12,200		
	MLAB	424	836	1,717		
Variable-precision DS	SP Block	150	156	342		
18 x 18 Multiplier		300	312	684		
PLL		6	7	8		
6 Gbps Transceiver		6	6 9			
GPIO ⁽⁵⁾		336	480	560		
LVDS	Transmitter	84	120	140		
		•	·	continued		

⁽⁵⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.





Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



Maximum Resources

Table 12. Maximum Resource Counts for Cyclone V SX Devices

Res	ource	Member Code					
		C2	C4	C5	C6		
Logic Elements (LE) (K)		25	40	85	110		
ALM		9,430	15,880	32,070	41,910		
Register		37,736	60,376	128,300	166,036		
Memory (Kb)	M10K	1,400	2,700	3,970	5,570		
	MLAB	138	231	480	621		
Variable-precision	Variable-precision DSP Block		84	87	112		
18 x 18 Multiplier		72	168	168 174			
FPGA PLL		5	5	6	6		
		•	•		continued		

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Resource		Member Code					
		C2	C4	C5	C6		
HPS PLL		3	3	3	3		
3 Gbps Transceiver	-	6	6	9	9		
FPGA GPIO ⁽⁸⁾		145	145	288	288		
HPS I/O		181	181	181	181		
LVDS	Transmitter	32	32	72	72		
	Receiver	37	37	72	72		
PCIe Hard IP Block		2	2	2 (9)	2 (9)		
FPGA Hard Memory Controller		1	1	1	1		
HPS Hard Memory Controller		1	1	1	1		
Arm Cortex-A9 MP	Core Processor	Dual-core	Dual-core	Dual-core	Dual-core		

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices Provides the number of LVDS channels in each device package.

Package Plan

Table 13.Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
C2	145	181	6	_	_	_
C4	145	181	6	-	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ 1 PCIe Hard IP Block in U672 package.



Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices



Maximum Resources

Table 14. Maximum Resource Counts for Cyclone V ST Devices

Reso	ource	Member Code			
		D5	D6		
Logic Elements (LE) (K)		85	110		
ALM		32,070	41,910		
Register		128,300	166,036		
Memory (Kb)	M10K	3,970	5,570		
	MLAB	480	621		
Variable-precision DSP Block		87	112		
18 x 18 Multiplier		174	224		
FPGA PLL		6	6		
HPS PLL		3	3		
6.144 Gbps Transceiver		9	9		
FPGA GPIO ⁽¹⁰⁾		288	288		
HPS I/O		181	181		
LVDS Transmitter		72	72		
			continued		

⁽¹⁰⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



Figure 8. ALM for Cyclone V Devices



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

Related Information

Embedded Memory Capacity in Cyclone V Devices on page 21 Lists the embedded memory capacity for each device.

Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiplyaccumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software



Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters and general DSP usage	Two 18 x 18 with accumulate	1
High precision fixed- or floating-point implementations	One 27 x 27 with accumulate	1

You can configure each DSP block during compilation as independent three 9 x 9, two 18×18 , or one 27×27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Table 17. Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

Variant	Member Code	Variable- precision	Indepen Multi	dent Input an iplications Ope	d Output erator	18 x 18 Multiplier	18 x 18 Multiplier
		DSP BIOCK	9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier	- Adder Mode	Summed with 36 bit Input
Cyclone V E	A2	25	75	50	25	25	25
	A4	66	198	132	66	66	66
	A5	150	450	300	150	150	150
	A7	156	468	312	156	156	156
	A9	342	1,026	684	342	342	342
Cyclone V	C3	57	171	114	57	57	57
٩٨	C4	70	210	140	70	70	70
	C5	150	450	300	150	150	150
	C7	156	468	312	156	156	156
	C9	342	1,026	684	342	342	342
Cyclone V GT	D5	150	450	300	150	150	150
	D7	156	468	312	156	156	156
	D9	342	1,026	684	342	342	342
Cyclone V SE	A2	36	108	72	36	36	36
	A4	84	252	168	84	84	84
	A5	87	261	174	87	87	87
	A6	112	336	224	112	112	112
Cyclone V SX	C2	36	108	72	36	36	36
	C4	84	252	168	84	84	84
	C5	87	261	174	87	87	87
							continued



Variant	Member Code	Variable- precision	Indepen Multi	dent Input and plications Ope	18 x 18 Multiplier	18 x 18 Multiplier		
		DSP Block	9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier	Adder Mode	Summed with 36 bit Input	
	C6	112	336	224	112	112	112	
Cyclone V ST	D5	87	261	174	87	87	87	
	D6	112	336	224	112	112	112	

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Types of Embedded Memory

The Cyclone V devices contain two types of memory blocks:

- 10 Kb M10K blocks—blocks of dedicated memory resources. The M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Cyclone V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Cyclone V Devices

Table 18. Embedded Memory Capacity and Distribution in Cyclone V Devices

	Mombor	М10К		ML	Total DAM Bit	
Variant	Code	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	(Kb)
Cyclone V E	A2	176	1,760	314	196	1,956
	A4	308	3,080	485	303	3,383
	A5	446	4,460	679	424	4,884
	A7	686	6,860	1338	836	7,696
	A9	1,220	12,200	2748	1,717	13,917
Cyclone V GX	C3	135	1,350	291	182	1,532
	C4	250	2,500	678	424	2,924
	C5	446	4,460	678	424	4,884
	C7	686	6,860	1338	836	7,696
	C9	1,220	12,200	2748	1,717	13,917
						continued



	Mombor	M1	.0К	ML		
Variant	Code	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	(Kb)
Cyclone V GT	D5	446	4,460	679	424	4,884
	D7	686	6,860	1338	836	7,696
	D9	1,220	12,200	2748	1,717	13,917
Cyclone V SE	A2	140	1,400	221	138	1,538
	A4	270	2,700	370	231	2,460
	A5	397	3,970	768	480	4,450
	A6	553	5,530	994	621	6,151
Cyclone V SX	C2	140	1,400	221	138	1,538
	C4	270	2,700	370	231	2,460
	C5	397	3,970	768	480	4,450
	C6	553	5,530	994	621	6,151
Cyclone V ST	D5	397	3,970	768	480	4,450
	D6	553	5,530	994	621	6,151

Embedded Memory Configurations

Table 19. Supported Embedded Memory Block Configurations for Cyclone V Devices

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1К	x10 or x8
	2К	x5 or x4
	4К	x2
	8К	×1

Clock Networks and PLL Clock Sources

550 MHz Cyclone V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Intel's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

Note: To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.



PCIe Gen1 and Gen2 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen2 and Gen1 end point and root port for up to x4 lane configuration. The PCIe Gen2 x4 support is PCIe-compatible.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

Figure 9. PCIe Multifunction for Cyclone V Devices



The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

External Memory Interface

This section provides an overview of the external memory interface in Cyclone V devices.

Hard and Soft Memory Controllers

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Cyclone V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Cyclone V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices for maximum flexibility.



External Memory Performance

Table 20. External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

Interface	Voltage	Maximum Free	Minimum Frequency		
	(V)	Hard Controller	Soft Controller	(1112)	
DDR3 SDRAM	1.5	400	303	303	
	1.35	400	303	303	
DDR2 SDRAM	1.8	400	300	167	
LPDDR2 SDRAM	1.2	333	300	167	

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 21. HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
LPDDR2 SDRAM	1.2	333

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Cyclone V devices deliver the industry's lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.



PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO[®] (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 6.144 Gbps are supported.

Table 23.	Transceiver	PCS	Features	for	Cvclone	V	Devices
						_	

PCS Support	Data Rates (Gbps)	Transmitter Data Path Feature	Receiver Data Path Feature	
3-Gbps and 6-Gbps Basic	0.614 to 6.144	 Phase compensation FIFO Byte serializer 8B/10B encoder Transmitter bit-slip 	 Word aligner Deskew FIFO Rate-match FIFO 8B/10B decoder Byte deserializer Byte ordering Receiver phase compensation FIFO 	
PCIe Gen1 (x1, x2, x4)	2.5 and 5.0	 Dedicated PCIe PHY IP core PIPE 2.0 interface to the core logic 	 Dedicated PCIe PHY IP core PIPE 2.0 interface to the core logic 	
PCIe Gen2 (x1, x2, x4) ⁽¹²⁾		logic	logic	
GbE	1.25	 Custom PHY IP core with preset feature GbE transmitter synchronization state machine 	 Custom PHY IP core with preset feature GbE receiver synchronization state machine 	
XAUI (13)	3.125	Dedicated XAUI PHY IP core	Dedicated XAUI PHY IP core	
HiGig	3.75	XAUI synchronization state machine for bonding four channels	 XAUI synchronization state machine for realigning four channels 	
SRIO 1.3 and 2.1	1.25 to 3.125	 Custom PHY IP core with preset feature SRIO version 2.1-compliant x2 and x4 channel bonding 	 Custom PHY IP core with preset feature SRIO version 2.1-compliant x2 and x4 deskew state machine 	
SDI, SD/HD, and 3G-SDI	0.27 ⁽¹⁴⁾ , 1.485, and 2.97	Custom PHY IP core with preset feature	Custom PHY IP core with preset feature	
JESD204A	0.3125 ⁽¹⁵⁾ to 3.125			
			continued	

⁽¹²⁾ PCIe Gen2 is supported for Cyclone V GT and ST devices. The PCIe Gen2 x4 support is PCIe-compatible.

⁽¹⁵⁾ The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹³⁾ XAUI is supported through the soft PCS.

 $^{^{(14)}}$ The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.





PCS Support Data Rates (Gbps)		Transmitter Data Path Feature	Receiver Data Path Feature	
Serial ATA Gen1 and Gen2	1.5 and 3.0	Custom PHY IP core with preset featureElectrical idle	 Custom PHY IP core with preset feature Signal detect Wider spread of asynchronous SSC 	
CPRI 4.1 ⁽¹⁶⁾	0.6144 to 6.144	Dedicated deterministic latency PHY IP core	Dedicated deterministic latency PHY IP core	
OBSAI RP3	0.768 to 3.072	Transmitter (TX) manual bit-slip mode	Receiver (RX) deterministic latency state machine	
V-by-One HS	Up to 3.75	Custom PHY IP core	Custom PHY IP core	
DisplayPort 1.2 ⁽¹⁷⁾	1.62 and 2.7		Wider spread of asynchronous SSC	

SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

⁽¹⁶⁾ High-voltage output mode (1000-BASE-CX) is not supported.

⁽¹⁷⁾ Pending characterization.





Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.



Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

Document Revision History for Cyclone V Device Overview

Document Version	Changes
2018.05.07	 Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the Sample Ordering Code and Available Options diagrams. Rebranded as Intel

Date	Version	Changes
December 2017	2017.12.18	Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices.
June 2016	2016.06.10	Updated Cyclone V GT speed grade to -7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram.
December 2015	2015.12.21	 Added descriptions to package plan tables for Cyclone V GT and ST devices. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.
June 2015	2015.06.12	 Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives. Updated logic elements (LE) (K) for the following devices: Cyclone V E A7: Updated from 149.5 to 150 Cyclone V GX C3: Updated from 149.7 to 150 Cyclone V GT D7: Updated from 149.5 to 150 Cyclone V GT D7: Updated from 149.5 to 150 Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows: Cyclone V GX C3: Updated from 291 to 182 Cyclone V GX C4: Updated from 678 to 424 Cyclone V GX C7: Updated from 1,338 to 836 Cyclone V GX C9: Updated from 1,717
	1	continued

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July 2014	2014.07.07	Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices.
December 2013	2013.12.26	 Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz. Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. Removed the note "The number of GPIOs does not include transceiver I/Os." In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE. Added link to Altera Product Selector for each device variant. Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers. Added leaded package options. Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 84 to 60. Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 174 to 252. Corrected 18 x 18 multiplier for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32. Corrected turbs transmitter for Cyclone V ST devices ordering code from 4 to 5. Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency form 300 to 303 for voltage 1.35V. Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V. Added decompression support for the CvP configuration mode.
May 2013	2013.05.06	 Added link to the known document issues in the Knowledge Base. Moved all links to the Related Information section of respective topics for easy reference. Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2. Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'. Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'. Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'. Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3. Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'. Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values. Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device. Updated 5 Gbps to '6.144 Gbps' forCyclone V GT device.

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Date	Version	Changes
		 Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10. Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections. Text edits throughout the document.
February 2012	1.2	 Updated Table 1–2, Table 1–3, and Table 1–6. Updated "Cyclone V Family Plan" on page 1–4 and "Clock Networks and PLL Clock Sources" on page 1–15. Updated Figure 1–1 and Figure 1–6.
November 2011	1.1	 Updated Table 1-1, Table 1-2, Table 1-3, Table 1-4, Table 1-5, and Table 1-6. Updated Figure 1-4, Figure 1-5, Figure 1-6, Figure 1-7, and Figure 1-8. Updated "System Peripherals" on page 1-18, "HPS-FPGA AXI Bridges" on page 1-19, "HPS SDRAM Controller Subsystem" on page 1-19, "FPGA Configuration and Processor Booting" on page 1-19, and "Hardware and Software Development" on page 1-20. Minor text edits.
October 2011	1.0	Initial release.