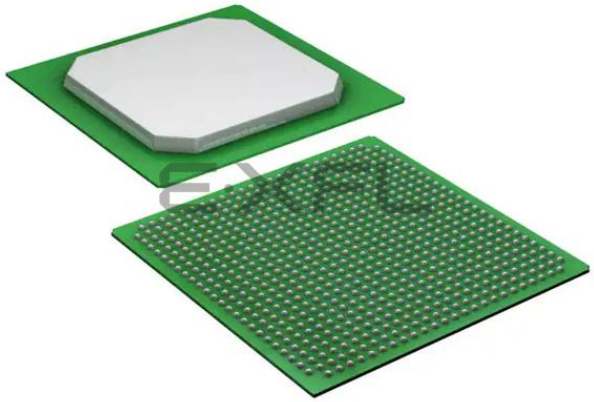


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	113560
Number of Logic Elements/Cells	301000
Total RAM Bits	14251008
Number of I/O	336
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cefa9f27c7n

Summary of Cyclone V Features

Table 2. Summary of Features for Cyclone V Devices

Feature	Description	
Technology	• TSMC's 28-nm low-power (28LP) process technology • 1.1 V core voltage	
Packaging	• Wirebond low-halogen packages • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS-compliant and leaded(1) options	
High-performance FPGA fabric	Enhanced 8-input ALM with four registers	
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) • Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory	
Embedded Hard IP blocks	Variable-precision DSP	• Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block • 64-bit accumulator and cascade • Embedded internal coefficient memory • Preadder/subtractor for improved efficiency
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support
	Embedded transceiver I/O	PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
Clock networks	• Up to 550 MHz global clock network • Global, quadrant, and peripheral clock networks • Clock networks that are not used can be powered down to reduce dynamic power	
Phase-locked loops (PLLs)	• Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) • Integer mode and fractional mode	
FPGA General-purpose I/Os (GPIOs)	• 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter • 400 MHz/800 Mbps external memory interface • On-chip termination (OCT) • 3.3 V support with up to 16 mA drive strength	
Low-power high-speed serial interface	• 614 Mbps to 6.144 Gbps integrated transceiver speed • Transmit pre-emphasis and receiver equalization • Dynamic partial reconfiguration of individual channels	
HPS (Cyclone V SE, SX, and ST devices only)	• Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing • Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I^2C interface, and up to 85 HPS GPIO interfaces • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • On-chip RAM and boot ROM	

continued...

(1) Contact Intel for availability.

Feature	Description
	• HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa • FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller • Arm CoreSight™ JTAG debug access port, trace port, and on-chip trace storage
Configuration	• Tamper protection—comprehensive design protection to protect your valuable IP investments • Enhanced advanced encryption standard (AES) design security features • CvP • Dynamic reconfiguration of the FPGA • Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8 and x16 configuration options • Internal scrubbing (2) • Partial reconfiguration (3)

Cyclone V Device Variants and Packages

Table 3. Device Variants for the Cyclone V Device Family

Variant	Description
Cyclone V E	Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications
Cyclone V GX	Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications
Cyclone V GT	The FPGA industry's lowest cost and lowest power requirement for 6.144 Gbps transceiver applications
Cyclone V SE	SoC with integrated Arm-based HPS
Cyclone V SX	SoC with integrated Arm-based HPS and 3.125 Gbps transceivers
Cyclone V ST	SoC with integrated Arm-based HPS and 6.144 Gbps transceivers

Cyclone V E

This section provides the available options, maximum resource counts, and package plan for the Cyclone V E devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Product Selector Guide.

Related Information

Product Selector Guide
Provides the latest information about Intel products.

(2) The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

(3) The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel® sales representatives.

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 5. Package Plan for Cyclone V E Devices

Member Code	M383 (13 mm)	M484 (15 mm)	U324 (15 mm)	F256 (17 mm)	U484 (19 mm)	F484 (23 mm)	F672 (27 mm)	F896 (31 mm)
	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
A2	223	—	176	128	224	224	—	—
A4	223	—	176	128	224	224	—	—
A5	175	—	—	—	224	240	—	—
A7	—	240	—	—	240	240	336	480
A9	—	—	—	—	240	224	336	480

Cyclone V GX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

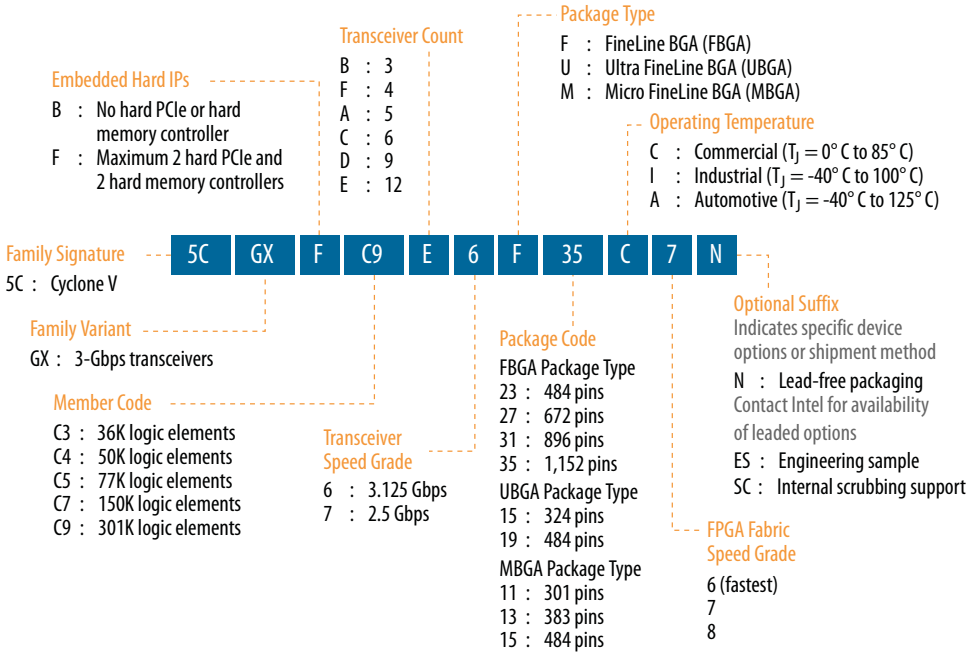
Related Information

Product Selector Guide
Provides the latest information about Intel products.

Available Options

Figure 2. Sample Ordering Code and Available Options for Cyclone V GX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Maximum Resources

Table 6. Maximum Resource Counts for Cyclone V GX Devices

Resource		Member Code				
		C3	C4	C5	C7	C9
Logic Elements (LE) (K)		36	50	77	150	301
ALM		13,460	18,860	29,080	56,480	113,560
Register		53,840	75,440	116,320	225,920	454,240
Memory (Kb)	M10K	1,350	2,500	4,460	6,860	12,200
	MLAB	182	424	424	836	1,717
Variable-precision DSP Block		57	70	150	156	342
18 x 18 Multiplier		114	140	300	312	684
PLL		4	6	6	7	8
3 Gbps Transceiver		3	6	6	9	12
GPIO(4)		208	336	336	480	560

continued...

(4) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus® Prime software, the number of user I/Os includes transceiver I/Os.

Resource		Member Code				
		C3	C4	C5	C7	C9
LVDS	Transmitter	52	84	84	120	140
	Receiver	52	84	84	120	140
PCIe Hard IP Block		1	2	2	2	2
Hard Memory Controller		1	2	2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 7. Package Plan for Cyclone V GX Devices

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U324 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	—	—	—	—	—	—	144	3	208	3
C4	129	4	175	6	—	—	—	—	224	6
C5	129	4	175	6	—	—	—	—	224	6
C7	—	—	—	—	240	3	—	—	240	6
C9	—	—	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	208	3	—	—	—	—	—	—
C4	240	6	336	6	—	—	—	—
C5	240	6	336	6	—	—	—	—
C7	240	6	336	9	480	9	—	—
C9	224	6	336	9	480	12	560	12

Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide
Provides the latest information about Intel products.

Resource		Member Code		
		D5	D7	D9
	Receiver	84	120	140
PCIe Hard IP Block		2	2	2
Hard Memory Controller		2	2	2

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 9. Package Plan for Cyclone V GT Devices

Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	129	4	175	6	—	—	224	6
D7	—	—	—	—	240	3	240	6
D9	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
D5	240	6	336	6	—	—	—	—
D7	240	6	336	9 (6)	480	9 (6)	—	—
D9	224	6	336	9 (6)	480	12 (7)	560	12 (7)

Related Information

6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

(6) If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

(7) If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

Maximum Resources

Table 10. Maximum Resource Counts for Cyclone V SE Devices

Resource		Member Code			
		A2	A4	A5	A6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,430	15,880	32,070	41,910
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6
HPS PLL		3	3	3	3
FPGA GPIO		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 11. Package Plan for Cyclone V SE Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U484 (19 mm)		U672 (23 mm)		F896 (31 mm)	
	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O
A2	66	151	145	181	—	—
A4	66	151	145	181	—	—
A5	66	151	145	181	288	181
A6	66	151	145	181	288	181

Resource		Member Code			
		C2	C4	C5	C6
HPS PLL		3	3	3	3
3 Gbps Transceiver		6	6	9	9
FPGA GPIO (8)		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
PCIe Hard IP Block		2	2	2 (9)	2 (9)
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core	Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 13. Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
C2	145	181	6	—	—	—
C4	145	181	6	—	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

(8) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(9) 1 PCIe Hard IP Block in U672 package.

Resource		Member Code	
		D5	D6
	Receiver	72	72
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		1	1
HPS Hard Memory Controller		1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices
Provides the number of LVDS channels in each device package.

Package Plan

Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR
D5	288	181	9 (11)
D6	288	181	9 (11)

Related Information

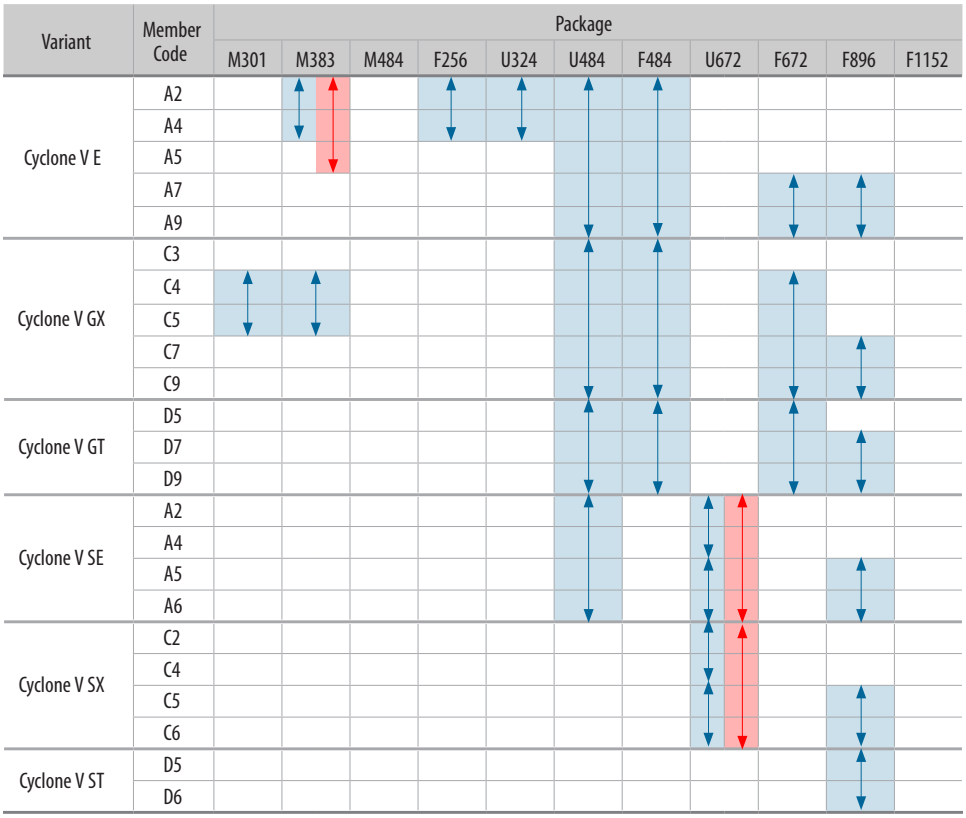
6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers
Provides more information about 6 Gbps transceiver channel count.

(11) If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

I/O Vertical Migration for Cyclone V Devices

Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.



You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

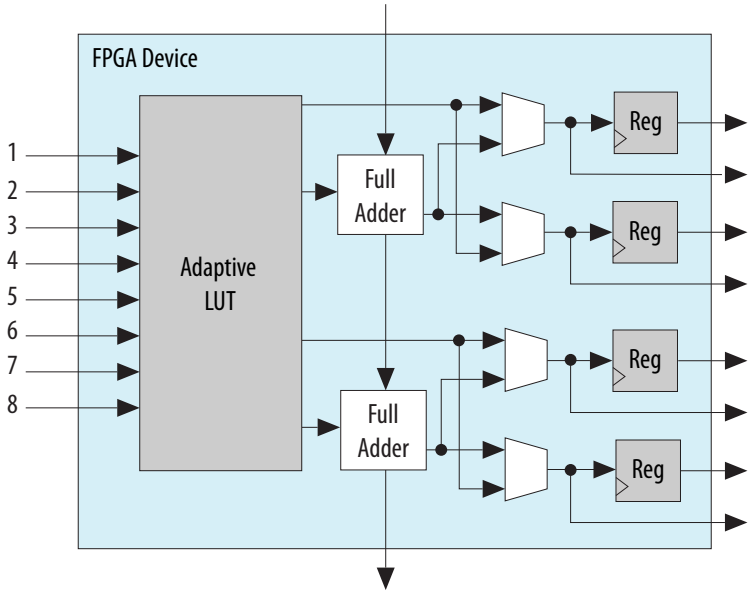
Note: To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

Figure 8. ALM for Cyclone V Devices



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

Related Information

Embedded Memory Capacity in Cyclone V Devices on page 21
Lists the embedded memory capacity for each device.

Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier		
	C6	112	336	224	112	112	112
Cyclone V ST	D5	87	261	174	87	87	87
	D6	112	336	224	112	112	112

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Types of Embedded Memory

The Cyclone V devices contain two types of memory blocks:

- 10 Kb M10K blocks—blocks of dedicated memory resources. The M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Cyclone V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Cyclone V Devices

Table 18. Embedded Memory Capacity and Distribution in Cyclone V Devices

Variant	Member Code	M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Cyclone V E	A2	176	1,760	314	196	1,956
	A4	308	3,080	485	303	3,383
	A5	446	4,460	679	424	4,884
	A7	686	6,860	1338	836	7,696
	A9	1,220	12,200	2748	1,717	13,917
Cyclone V GX	C3	135	1,350	291	182	1,532
	C4	250	2,500	678	424	2,924
	C5	446	4,460	678	424	4,884
	C7	686	6,860	1338	836	7,696
	C9	1,220	12,200	2748	1,717	13,917

continued...

Variant	Member Code	M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Cyclone V GT	D5	446	4,460	679	424	4,884
	D7	686	6,860	1338	836	7,696
	D9	1,220	12,200	2748	1,717	13,917
Cyclone V SE	A2	140	1,400	221	138	1,538
	A4	270	2,700	370	231	2,460
	A5	397	3,970	768	480	4,450
	A6	553	5,530	994	621	6,151
Cyclone V SX	C2	140	1,400	221	138	1,538
	C4	270	2,700	370	231	2,460
	C5	397	3,970	768	480	4,450
	C6	553	5,530	994	621	6,151
Cyclone V ST	D5	397	3,970	768	480	4,450
	D6	553	5,530	994	621	6,151

Embedded Memory Configurations

Table 19. Supported Embedded Memory Block Configurations for Cyclone V Devices

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

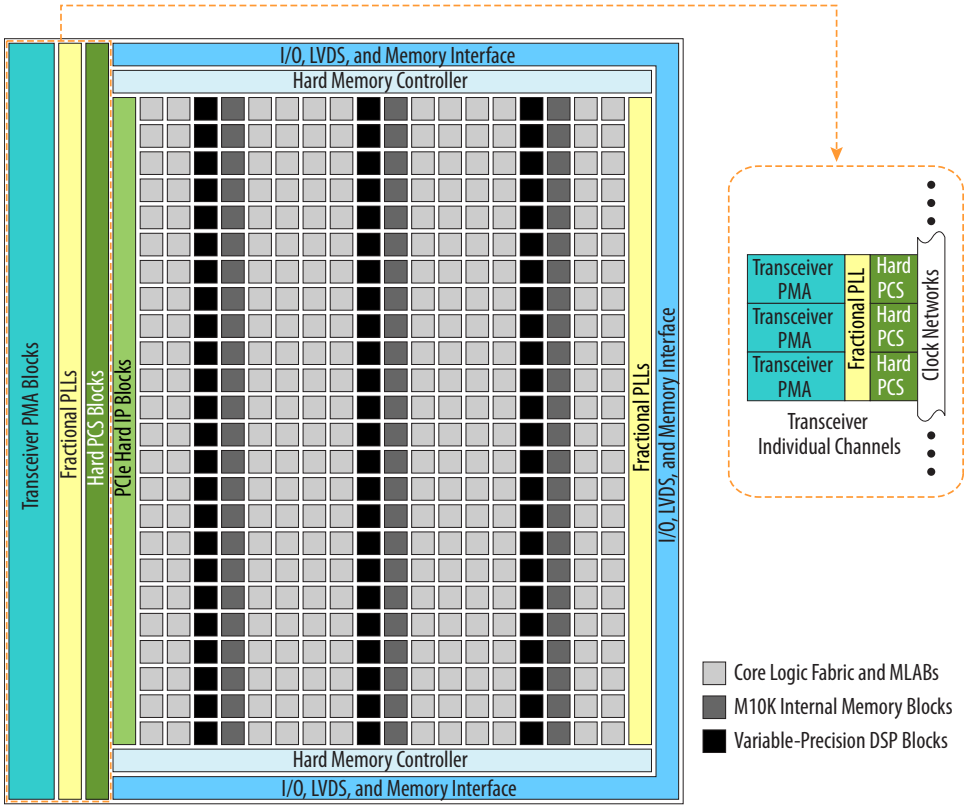
Clock Networks and PLL Clock Sources

550 MHz Cyclone V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Intel's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

Note: To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

Figure 10. Device Chip Overview for Cyclone V GX and GT Devices

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.



PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

Table 22. PMA Features of the Transceivers in Cyclone V Devices

Features	Capability
Backplane support	Driving capability up to 6.144 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	• Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization • No decision feedback equalizer (DFE)
Ring oscillator transmit PLLs	614 Mbps to 6.144 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

Note: Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

Related Information

Cyclone V Device Family Pin Connection Guidelines
Provides detailed information about power supply pin connection guidelines and power regulator sharing.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer (Standard) system integration tool in the Intel Quartus Prime software.

For software development, the Arm-based SoC devices inherit the rich software development ecosystem available for the Arm Cortex-A9 MPCore processor. The software development process for Intel SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Intel sales team.

You can begin device-specific firmware and software development on the Intel SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Related Information

International Altera Sales Support Offices

Dynamic and Partial Reconfiguration

The Cyclone V devices support dynamic reconfiguration and partial reconfiguration.

Dynamic Reconfiguration

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

Partial Reconfiguration

Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Intel simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Intel Quartus Prime design software. With the Intel solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.

Table 24. Configuration Schemes and Features Supported by Cyclone V Devices

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration[18]	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes	
CvP (PCIe)	x1, x2, and x4 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Related Information

Configuration via Protocol (CvP) Implementation in Intel FPGAs User Guide
Provides more information about CvP.

(18) The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

Document Revision History for Cyclone V Device Overview

Document Version	Changes
2018.05.07	• Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the *Sample Ordering Code and Available Options* diagrams. • Rebranded as Intel.

Date	Version	Changes
December 2017	2017.12.18	• Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices.
June 2016	2016.06.10	Updated Cyclone V GT speed grade to –7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram.
December 2015	2015.12.21	• Added descriptions to package plan tables for Cyclone V GT and ST devices. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.12	• Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives. • Updated logic elements (LE) (K) for the following devices: — Cyclone V E A7: Updated from 149.5 to 150 — Cyclone V GX C3: Updated from 35.5 to 36 — Cyclone V GX C7: Updated from 149.7 to 150 — Cyclone V GT D7: Updated from 149.5 to 150 • Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows: — Cyclone V GX C3: Updated from 291 to 182 — Cyclone V GX C4: Updated from 678 to 424 — Cyclone V GX C5: Updated from 678 to 424 — Cyclone V GX C7: Updated from 1,338 to 836 — Cyclone V GX C9: Updated from 2,748 to 1,717

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Date	Version	Changes
		• Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C3: Updated from 181 to 182 — Cyclone V GX C4: Updated from 295 to 424 • Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C3: Updated from 1,531 to 1,532 — Cyclone V GX C4: Updated from 2,795 to 2,924 • Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: — Cyclone V GX C4: Updated from 472 to 678 — Cyclone V GX C5: Updated from 679 to 678
March 2015	2015.03.31	• Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table. • Added optional suffix "SC: Internal scrubbing support" to the following diagrams: — Sample Ordering Code and Available Options for Cyclone V E Devices — Sample Ordering Code and Available Options for Cyclone V GX Devices — Sample Ordering Code and Available Options for Cyclone V SE Devices — Sample Ordering Code and Available Options for Cyclone V SX Devices
January 2015	2015.01.23	• Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and –7 speed grade. — Operating Temperature: Removed C and A temperature grades — FPGA Fabric Speed Grade: Removed –6 and –8 speed grades • Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps: — Device Variants for the Cyclone V Device Family table — Sample Ordering Code and Available Options for Cyclone V ST Devices figure — Maximum Resource Counts for Cyclone V ST Devices • Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices. — Logic elements (LE) (K): Updated from 35.7 to 35.5 — Variable-precision DSP block: Updated from 51 to 57 — 18 x 18 multiplier: Updated from 102 to 114 • Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices. — Variableprecision DSP Block: Updated from 51 to 57 — 9 x 9 Multiplier: Updated from 153 to 171 — 18 x 18 Multiplier: Updated from 102 to 114 — 27 x 27 Multiplier: Updated from 51 to 57 — 18 x 18 Multiplier Adder Mode: Updated from 51 to 57 — 18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57 • Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices. — M10K block: Updated from 119 to 135 — M10K RAM bit (Kb): Updated from 1,190 to 1,350 — MLAB block: Updated from 255 to 291 — MLAB RAM bit (Kb): Updated from 159 to 181 — Total RAM bit (Kb): Updated from 1,349 to 1,531
October 2014	2014.10.06	Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices.

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Date	Version	Changes
July 2014	2014.07.07	Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices.
December 2013	2013.12.26	• Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz. • Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. • Removed the note "The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE. • Added link to Altera Product Selector for each device variant. • Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers. • Added leaded package options. • Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. • Corrected max LVDS counts for transmitter and receiver for Cyclone V E A5 device from 84 to 60. • Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 140 to 120. • Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 58 to 84. • Corrected 18 x 18 multiplier for Cyclone V SE devices from 116 to 168. • Corrected 9 x 9 multiplier for Cyclone V SE devices from 174 to 252. • Corrected LVDS transmitter for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32. • Corrected LVDS receiver for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 35 to 37. • Corrected transceiver speed grade for Cyclone V ST devices ordering code from 4 to 5. • Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency from 300 to 303 for voltage 1.35V. • Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. • Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V. • Added decompression support for the CvP configuration mode.
May 2013	2013.05.06	• Added link to the known document issues in the Knowledge Base. • Moved all links to the Related Information section of respective topics for easy reference. • Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2. • Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'. • Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'. • Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'. • Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3. • Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'. • Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values. • Updated the package plan with M383 for the Cyclone V E device. • Removed the M301 and M383 packages from the Cyclone V GX C4 device. • Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device. • Updated 5 Gbps to '6.144 Gbps' forCyclone V GT device.

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Date	Version	Changes
		• Updated HPS I/O for U484 (19 mm) in Table 11 with '151' for A2, A4, A5 and A6. • Updated Memory (Kb) for Maximum Resource Counts for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. • Updated FPGA PLL for Maximum Resource Counts for Cyclone V SE A2, SX C2, devices. • Removed '36 x 36' from the Variable-Precision DSP Block. • Updated Variable-precision DSP Blocks and 18 x 18 Multiplier for Maximum Resource Counts for Cyclone V SX C4 device. • Updated the HPS I/O counts for Cyclone V SE, SX, and ST devices. • Updated Figure 7 which shows the I/O vertical migration table. • Updated Table 17 for Cyclone V SX C4 device. • Updated Embedded Memory Capacity and Distribution table for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices. • Removed 'Counter reconfiguration' from the PLL Features. • Updated Low-Power Serial Transceivers by replacing 5 Gbps with 6.144 Gbps. • Removed 'Distributed Memory' symbol. • Updated the Capability in Table 22 of Backplane support to '6.144 Gbps'. • Updated Capability in Table 22 of Ring oscillator transmit PLLs with 6.144 Gbps. • Updated the PCS Support in Table 23 from 5 Gbps to '6 Gbps'. • Updated the Data Rates (Gbps) in Table 23 of 3 Gbps and 6 Gbps Basic to '6.144 Gbps'. • Updated the Data Rates (Gbps) in Table 23 of CPRI 4.1 to '6.144 Gbps'. • Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.
December 2012	2012.12.28	• Updated the pin counts for the MBGA packages. • Updated the GPIO and transceiver counts for the MBGA packages. • Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices. • Updated the vertical migration table for vertical migration of the U484 packages. • Updated the MLAB supported programmable widths at 32 bits depth.
November 2012	2012.11.19	• Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT. • Added ordering code for five-transceiver devices for Cyclone V GT and ST. • Updated the vertical migration table to add MBGA packages. • Added performance information for HPS memory controller. • Removed DDR3U support. • Updated Cyclone V ST speed grade information. • Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance. • Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software. • Updated template.
July 2012	2.1	Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible)
June 2012	2.0	• Restructured the document. • Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections. • Added Table 1, Table 3, Table 16, Table 19, and Table 20. • Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18.

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