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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Active |
| Number of LABs/CLBs | 29080 |
| Number of Logic Elements/Cells | 77000 |
| Total RAM Bits | 5001216 |
| Number of I/O | 240 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5cgtfd5c5f23c7n |



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Cyclone V Device Overview

The Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

Related Information

[Cyclone V Device Handbook: Known Issues](#)

Lists the planned updates to the Cyclone V Device Handbook chapters.

Key Advantages of Cyclone V Devices

Table 1. Key Advantages of the Cyclone V Device Family

| Advantage | Supporting Feature |
|---|--|
| Lower power consumption | <ul style="list-style-type: none"> Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks Up to 40% lower power consumption than the previous generation device |
| Improved logic integration and differentiation capabilities | <ul style="list-style-type: none"> 8-input adaptive logic module (ALM) Up to 13.59 megabits (Mb) of embedded memory Variable-precision digital signal processing (DSP) blocks |
| Increased bandwidth capacity | <ul style="list-style-type: none"> 3.125 gigabits per second (Gbps) and 6.144 Gbps transceivers Hard memory controllers |
| Hard processor system (HPS) with integrated Arm* Cortex*-A9 MPCore* processor | <ul style="list-style-type: none"> Tight integration of a dual-core Arm Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC) Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric |
| Lowest system cost | <ul style="list-style-type: none"> Requires only two core voltages to operate Available in low-cost wirebond packaging Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration |

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*Other names and brands may be claimed as the property of others.

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Summary of Cyclone V Features

Table 2. Summary of Features for Cyclone V Devices

| Feature | Description | |
|--|---|---|
| Technology | <ul style="list-style-type: none"> TSMC's 28-nm low-power (28LP) process technology 1.1 V core voltage | |
| Packaging | <ul style="list-style-type: none"> Wirebond low-halogen packages Multiple device densities with compatible package footprints for seamless migration between different device densities RoHS-compliant and leaded⁽¹⁾ options | |
| High-performance FPGA fabric | Enhanced 8-input ALM with four registers | |
| Internal memory blocks | <ul style="list-style-type: none"> M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory | |
| Embedded Hard IP blocks | Variable-precision DSP | <ul style="list-style-type: none"> Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block 64-bit accumulator and cascade Embedded internal coefficient memory Padder/subtractor for improved efficiency |
| | Memory controller | DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support |
| | Embedded transceiver I/O | PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port |
| Clock networks | <ul style="list-style-type: none"> Up to 550 MHz global clock network Global, quadrant, and peripheral clock networks Clock networks that are not used can be powered down to reduce dynamic power | |
| Phase-locked loops (PLLs) | <ul style="list-style-type: none"> Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) Integer mode and fractional mode | |
| FPGA General-purpose I/Os (GPIOs) | <ul style="list-style-type: none"> 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter 400 MHz/800 Mbps external memory interface On-chip termination (OCT) 3.3 V support with up to 16 mA drive strength | |
| Low-power high-speed serial interface | <ul style="list-style-type: none"> 614 Mbps to 6.144 Gbps integrated transceiver speed Transmit pre-emphasis and receiver equalization Dynamic partial reconfiguration of individual channels | |
| HPS (Cyclone V SE, SX, and ST devices only) | <ul style="list-style-type: none"> Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-Go (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I²C interface, and up to 85 HPS GPIO interfaces System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers On-chip RAM and boot ROM | |

continued...

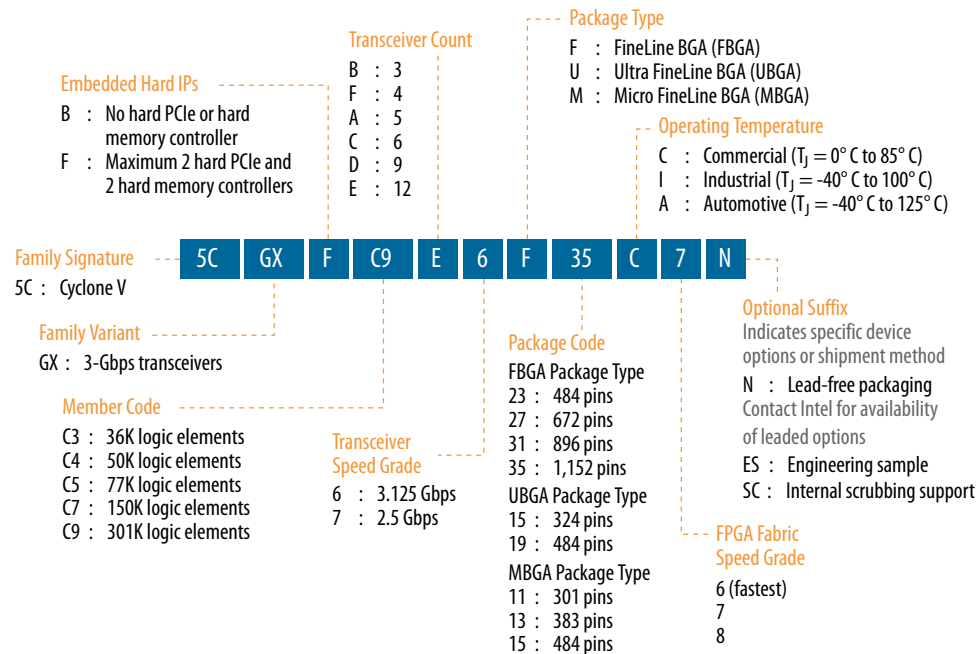
⁽¹⁾ Contact Intel for availability.



Available Options

Figure 2. Sample Ordering Code and Available Options for Cyclone V GX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Maximum Resources

Table 6. Maximum Resource Counts for Cyclone V GX Devices

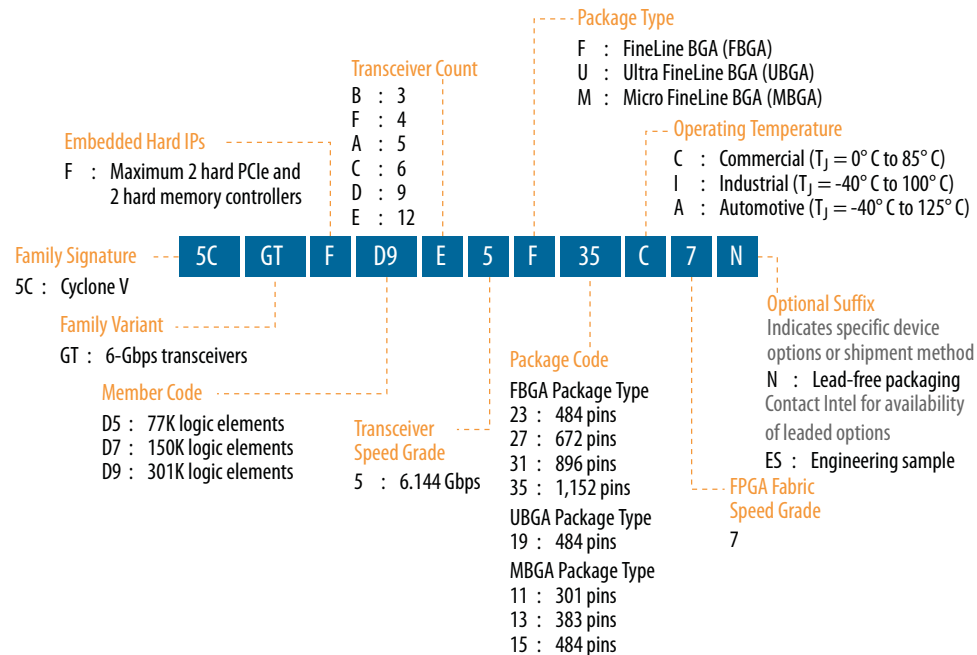
| Resource | | Member Code | | | | |
|------------------------------|------|-------------|--------|---------|---------|---------|
| | | C3 | C4 | C5 | C7 | C9 |
| Logic Elements (LE) (K) | | 36 | 50 | 77 | 150 | 301 |
| ALM | | 13,460 | 18,860 | 29,080 | 56,480 | 113,560 |
| Register | | 53,840 | 75,440 | 116,320 | 225,920 | 454,240 |
| Memory (Kb) | M10K | 1,350 | 2,500 | 4,460 | 6,860 | 12,200 |
| | MLAB | 182 | 424 | 424 | 836 | 1,717 |
| Variable-precision DSP Block | | 57 | 70 | 150 | 156 | 342 |
| 18 x 18 Multiplier | | 114 | 140 | 300 | 312 | 684 |
| PLL | | 4 | 6 | 6 | 7 | 8 |
| 3 Gbps Transceiver | | 3 | 6 | 6 | 9 | 12 |
| GPIO ⁽⁴⁾ | | 208 | 336 | 336 | 480 | 560 |
| continued... | | | | | | |

⁽⁴⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus® Prime software, the number of user I/Os includes transceiver I/Os.



Available Options

Figure 3. Sample Ordering Code and Available Options for Cyclone V GT Devices



Maximum Resources

Table 8. Maximum Resource Counts for Cyclone V GT Devices

| Resource | | Member Code | | |
|------------------------------|-------------|-------------|---------|---------|
| | | D5 | D7 | D9 |
| Logic Elements (LE) (K) | | 77 | 150 | 301 |
| ALM | | 29,080 | 56,480 | 113,560 |
| Register | | 116,320 | 225,920 | 454,240 |
| Memory (Kb) | M10K | 4,460 | 6,860 | 12,200 |
| | MLAB | 424 | 836 | 1,717 |
| Variable-precision DSP Block | | 150 | 156 | 342 |
| 18 x 18 Multiplier | | 300 | 312 | 684 |
| PLL | | 6 | 7 | 8 |
| 6 Gbps Transceiver | | 6 | 9 | 12 |
| GPIO ⁽⁵⁾ | | 336 | 480 | 560 |
| LVDS | Transmitter | 84 | 120 | 140 |

continued...

⁽⁵⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



| Resource | | Member Code | | |
|------------------------|----------|-------------|-----|-----|
| | | D5 | D7 | D9 |
| | Receiver | 84 | 120 | 140 |
| PCIe Hard IP Block | | 2 | 2 | 2 |
| Hard Memory Controller | | 2 | 2 | 2 |

Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

Package Plan

Table 9. Package Plan for Cyclone V GT Devices

Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

| Member Code | M301 (11 mm) | | M383 (13 mm) | | M484 (15 mm) | | U484 (19 mm) | |
|-------------|-----------------|------|-----------------|------|-----------------|------|-----------------|------|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| D5 | 129 | 4 | 175 | 6 | — | — | 224 | 6 |
| D7 | — | — | — | — | 240 | 3 | 240 | 6 |
| D9 | — | — | — | — | — | — | 240 | 5 |

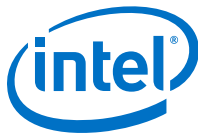
| Member Code | F484 (23 mm) | | F672 (27 mm) | | F896 (31 mm) | | F1152 (35 mm) | |
|-------------|-----------------|------|-----------------|------------------|-----------------|-------------------|------------------|-------------------|
| | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR | GPIO | XCVR |
| D5 | 240 | 6 | 336 | 6 | — | — | — | — |
| D7 | 240 | 6 | 336 | 9 ⁽⁶⁾ | 480 | 9 ⁽⁶⁾ | — | — |
| D9 | 224 | 6 | 336 | 9 ⁽⁶⁾ | 480 | 12 ⁽⁷⁾ | 560 | 12 ⁽⁷⁾ |

Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

-
- ⁽⁶⁾ If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.
- ⁽⁷⁾ If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.



Cyclone V SE

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SE devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 4. Sample Ordering Code and Available Options for Cyclone V SE Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.





Maximum Resources

Table 10. Maximum Resource Counts for Cyclone V SE Devices

| Resource | | Member Code | | | |
|--------------------------------|-------------|----------------------|----------------------|----------------------|----------------------|
| | | A2 | A4 | A5 | A6 |
| Logic Elements (LE) (K) | | 25 | 40 | 85 | 110 |
| ALM | | 9,430 | 15,880 | 32,070 | 41,910 |
| Register | | 37,736 | 60,376 | 128,300 | 166,036 |
| Memory (Kb) | M10K | 1,400 | 2,700 | 3,970 | 5,570 |
| | MLAB | 138 | 231 | 480 | 621 |
| Variable-precision DSP Block | | 36 | 84 | 87 | 112 |
| 18 x 18 Multiplier | | 72 | 168 | 174 | 224 |
| FPGA PLL | | 5 | 5 | 6 | 6 |
| HPS PLL | | 3 | 3 | 3 | 3 |
| FPGA GPIO | | 145 | 145 | 288 | 288 |
| HPS I/O | | 181 | 181 | 181 | 181 |
| LVDS | Transmitter | 32 | 32 | 72 | 72 |
| | Receiver | 37 | 37 | 72 | 72 |
| FPGA Hard Memory Controller | | 1 | 1 | 1 | 1 |
| HPS Hard Memory Controller | | 1 | 1 | 1 | 1 |
| Arm Cortex-A9 MPCore Processor | | Single- or dual-core | Single- or dual-core | Single- or dual-core | Single- or dual-core |

Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

Package Plan

Table 11. Package Plan for Cyclone V SE Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

| Member Code | U484 (19 mm) | | U672 (23 mm) | | F896 (31 mm) | |
|-------------|-----------------|---------|-----------------|---------|-----------------|---------|
| | FPGA GPIO | HPS I/O | FPGA GPIO | HPS I/O | FPGA GPIO | HPS I/O |
| A2 | 66 | 151 | 145 | 181 | — | — |
| A4 | 66 | 151 | 145 | 181 | — | — |
| A5 | 66 | 151 | 145 | 181 | 288 | 181 |
| A6 | 66 | 151 | 145 | 181 | 288 | 181 |



Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

Related Information

[Product Selector Guide](#)

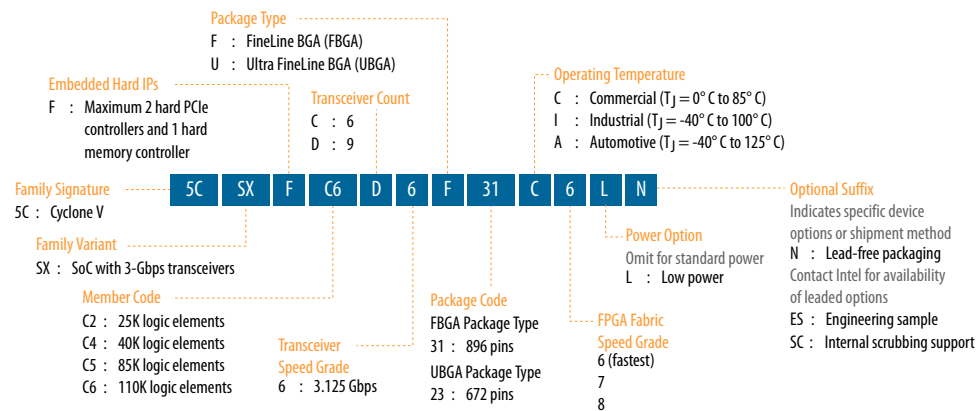
Provides the latest information about Intel products.

Available Options

Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



Maximum Resources

Table 12. Maximum Resource Counts for Cyclone V SX Devices

| Resource | | Member Code | | | |
|------------------------------|------|-------------|--------|---------|---------|
| | | C2 | C4 | C5 | C6 |
| Logic Elements (LE) (K) | | 25 | 40 | 85 | 110 |
| ALM | | 9,430 | 15,880 | 32,070 | 41,910 |
| Register | | 37,736 | 60,376 | 128,300 | 166,036 |
| Memory (Kb) | M10K | 1,400 | 2,700 | 3,970 | 5,570 |
| | MLAB | 138 | 231 | 480 | 621 |
| Variable-precision DSP Block | | 36 | 84 | 87 | 112 |
| 18 x 18 Multiplier | | 72 | 168 | 174 | 224 |
| FPGA PLL | | 5 | 5 | 6 | 6 |

continued...



| Resource | | Member Code | | | |
|--------------------------------|-------------|-------------|-----------|------------------|------------------|
| | | C2 | C4 | C5 | C6 |
| HPS PLL | | 3 | 3 | 3 | 3 |
| 3 Gbps Transceiver | | 6 | 6 | 9 | 9 |
| FPGA GPIO ⁽⁸⁾ | | 145 | 145 | 288 | 288 |
| HPS I/O | | 181 | 181 | 181 | 181 |
| LVDS | Transmitter | 32 | 32 | 72 | 72 |
| | Receiver | 37 | 37 | 72 | 72 |
| PCIe Hard IP Block | | 2 | 2 | 2 ⁽⁹⁾ | 2 ⁽⁹⁾ |
| FPGA Hard Memory Controller | | 1 | 1 | 1 | 1 |
| HPS Hard Memory Controller | | 1 | 1 | 1 | 1 |
| Arm Cortex-A9 MPCore Processor | | Dual-core | Dual-core | Dual-core | Dual-core |

Related Information

True LVDS Buffers in Devices, I/O Features in Cyclone V Devices

Provides the number of LVDS channels in each device package.

Package Plan

Table 13. Package Plan for Cyclone V SX Devices

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

| Member Code | U672 (23 mm) | | | F896 (31 mm) | | |
|-------------|-----------------|---------|------|-----------------|---------|------|
| | FPGA GPIO | HPS I/O | XCVR | FPGA GPIO | HPS I/O | XCVR |
| C2 | 145 | 181 | 6 | — | — | — |
| C4 | 145 | 181 | 6 | — | — | — |
| C5 | 145 | 181 | 6 | 288 | 181 | 9 |
| C6 | 145 | 181 | 6 | 288 | 181 | 9 |

Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ 1 PCIe Hard IP Block in U672 package.



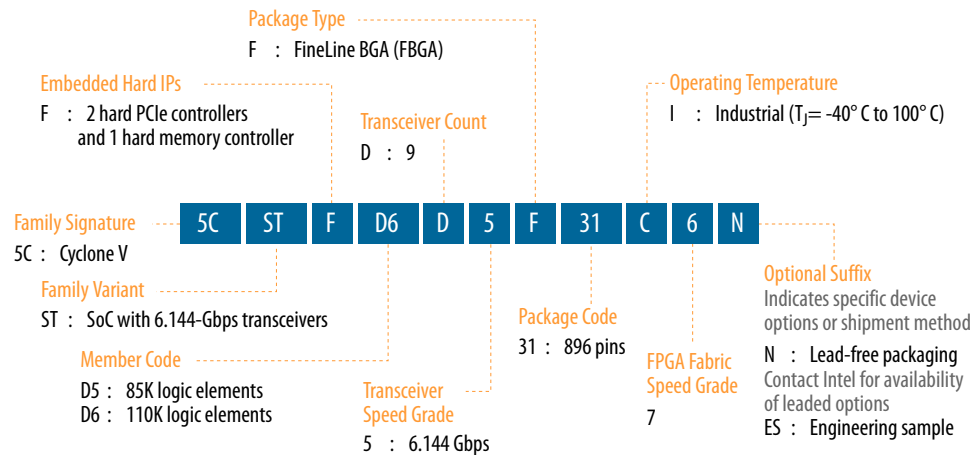
Related Information

Product Selector Guide

Provides the latest information about Intel products.

Available Options

Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices



Maximum Resources

Table 14. Maximum Resource Counts for Cyclone V ST Devices

| Resource | | Member Code | |
|------------------------------|-------------|-------------|---------|
| | | D5 | D6 |
| Logic Elements (LE) (K) | | 85 | 110 |
| ALM | | 32,070 | 41,910 |
| Register | | 128,300 | 166,036 |
| Memory (Kb) | M10K | 3,970 | 5,570 |
| | MLAB | 480 | 621 |
| Variable-precision DSP Block | | 87 | 112 |
| 18 x 18 Multiplier | | 174 | 224 |
| FPGA PLL | | 6 | 6 |
| HPS PLL | | 3 | 3 |
| 6.144 Gbps Transceiver | | 9 | 9 |
| FPGA GPIO ⁽¹⁰⁾ | | 288 | 288 |
| HPS I/O | | 181 | 181 |
| LVDS | Transmitter | 72 | 72 |
| continued... | | | |

⁽¹⁰⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



| Resource | | Member Code | |
|--------------------------------|----------|-------------|-----------|
| | | D5 | D6 |
| | Receiver | 72 | 72 |
| PCIe Hard IP Block | | 2 | 2 |
| FPGA Hard Memory Controller | | 1 | 1 |
| HPS Hard Memory Controller | | 1 | 1 |
| Arm Cortex-A9 MPCore Processor | | Dual-core | Dual-core |

Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

Package Plan

Table 15. Package Plan for Cyclone V ST Devices

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver ≤ 5 Gbps. 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

| Member Code | F896 (31 mm) | | |
|-------------|-----------------|---------|-------------------|
| | FPGA GPIO | HPS I/O | XCVR |
| D5 | 288 | 181 | 9 ⁽¹¹⁾ |
| D6 | 288 | 181 | 9 ⁽¹¹⁾ |

Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

⁽¹¹⁾ If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices

| Usage Example | Multiplier Size (Bit) | DSP Block Resource |
|---|-----------------------------|--------------------|
| Low precision fixed point for video applications | Three 9 x 9 | 1 |
| Medium precision fixed point in FIR filters | Two 18 x 18 | 1 |
| FIR filters and general DSP usage | Two 18 x 18 with accumulate | 1 |
| High precision fixed- or floating-point implementations | One 27 x 27 with accumulate | 1 |

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

Table 17. Number of Multipliers in Cyclone V Devices

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

| Variant | Member Code | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | | 18 x 18 Multiplier Adder Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|--------------|-------------|------------------------------|---|--------------------|--------------------|-------------------------------|---|
| | | | 9 x 9 Multiplier | 18 x 18 Multiplier | 27 x 27 Multiplier | | |
| Cyclone V E | A2 | 25 | 75 | 50 | 25 | 25 | 25 |
| | A4 | 66 | 198 | 132 | 66 | 66 | 66 |
| | A5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | A7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | A9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V GX | C3 | 57 | 171 | 114 | 57 | 57 | 57 |
| | C4 | 70 | 210 | 140 | 70 | 70 | 70 |
| | C5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | C7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | C9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V GT | D5 | 150 | 450 | 300 | 150 | 150 | 150 |
| | D7 | 156 | 468 | 312 | 156 | 156 | 156 |
| | D9 | 342 | 1,026 | 684 | 342 | 342 | 342 |
| Cyclone V SE | A2 | 36 | 108 | 72 | 36 | 36 | 36 |
| | A4 | 84 | 252 | 168 | 84 | 84 | 84 |
| | A5 | 87 | 261 | 174 | 87 | 87 | 87 |
| | A6 | 112 | 336 | 224 | 112 | 112 | 112 |
| Cyclone V SX | C2 | 36 | 108 | 72 | 36 | 36 | 36 |
| | C4 | 84 | 252 | 168 | 84 | 84 | 84 |
| | C5 | 87 | 261 | 174 | 87 | 87 | 87 |
| continued... | | | | | | | |



PLL Features

The PLLs in the Cyclone V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- User-mode reconfiguration of PLLs
- Low power mode for each fractional PLL
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation modes

Fractional PLL

In addition to integer PLLs, the Cyclone V devices use a fractional PLL architecture. The devices have up to eight PLLs, each with nine output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

FPGA General Purpose I/O

Cyclone V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- On-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture



External Memory Performance

Table 20. External Memory Interface Performance in Cyclone V Devices

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

| Interface | Voltage (V) | Maximum Frequency (MHz) | | Minimum Frequency (MHz) |
|--------------|-------------|-------------------------|-----------------|-------------------------|
| | | Hard Controller | Soft Controller | |
| DDR3 SDRAM | 1.5 | 400 | 303 | 303 |
| | 1.35 | 400 | 303 | 303 |
| DDR2 SDRAM | 1.8 | 400 | 300 | 167 |
| LPDDR2 SDRAM | 1.2 | 333 | 300 | 167 |

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

HPS External Memory Performance

Table 21. HPS External Memory Interface Performance

The hard processor system (HPS) is available in Cyclone V SoC devices only.

| Interface | Voltage (V) | HPS Hard Controller (MHz) |
|--------------|-------------|---------------------------|
| DDR3 SDRAM | 1.5 | 400 |
| | 1.35 | 400 |
| DDR2 SDRAM | 1.8 | 400 |
| LPDDR2 SDRAM | 1.2 | 333 |

Related Information

External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

Low-Power Serial Transceivers

Cyclone V devices deliver the industry's lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.



PCS Features

The Cyclone V core logic connects to the PCS through an 8, 10, 16, 20, 32, or 40 bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO® (SRIO), and Common Public Radio Interface (CPRI).

Most of the standard and proprietary protocols from 614 Mbps to 6.144 Gbps are supported.

Table 23. Transceiver PCS Features for Cyclone V Devices

| PCS Support | Data Rates (Gbps) | Transmitter Data Path Feature | Receiver Data Path Feature |
|--|--|--|--|
| 3-Gbps and 6-Gbps Basic | 0.614 to 6.144 | <ul style="list-style-type: none"> Phase compensation FIFO Byte serializer 8B/10B encoder Transmitter bit-slip | <ul style="list-style-type: none"> Word aligner Deskew FIFO Rate-match FIFO 8B/10B decoder Byte deserializer Byte ordering Receiver phase compensation FIFO |
| PCIe Gen1 (x1, x2, x4) | 2.5 and 5.0 | <ul style="list-style-type: none"> Dedicated PCIe PHY IP core PIPE 2.0 interface to the core logic | <ul style="list-style-type: none"> Dedicated PCIe PHY IP core PIPE 2.0 interface to the core logic |
| PCIe Gen2 (x1, x2, x4) ⁽¹²⁾ | | | |
| GbE | 1.25 | <ul style="list-style-type: none"> Custom PHY IP core with preset feature GbE transmitter synchronization state machine | <ul style="list-style-type: none"> Custom PHY IP core with preset feature GbE receiver synchronization state machine |
| XAUI ⁽¹³⁾ | 3.125 | <ul style="list-style-type: none"> Dedicated XAUI PHY IP core XAUI synchronization state machine for bonding four channels | <ul style="list-style-type: none"> Dedicated XAUI PHY IP core XAUI synchronization state machine for realigning four channels |
| HiGig | 3.75 | | |
| SRIO 1.3 and 2.1 | 1.25 to 3.125 | <ul style="list-style-type: none"> Custom PHY IP core with preset feature SRIO version 2.1-compliant x2 and x4 channel bonding | <ul style="list-style-type: none"> Custom PHY IP core with preset feature SRIO version 2.1-compliant x2 and x4 deskew state machine |
| SDI, SD/HD, and 3G-SDI | 0.27 ⁽¹⁴⁾ , 1.485, and 2.97 | Custom PHY IP core with preset feature | Custom PHY IP core with preset feature |
| JESD204A | 0.3125 ⁽¹⁵⁾ to 3.125 | | |

continued...

⁽¹²⁾ PCIe Gen2 is supported for Cyclone V GT and ST devices. The PCIe Gen2 x4 support is PCIe-compatible.

⁽¹³⁾ XAUI is supported through the soft PCS.

⁽¹⁴⁾ The 0.27-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

⁽¹⁵⁾ The 0.3125-Gbps data rate is supported using oversampling user logic that you must implement in the FPGA fabric.

Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor



System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 400 MHz (800 Mbps data rate).

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Intel simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Intel Quartus Prime design software. With the Intel solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.

Table 24. Configuration Schemes and Features Supported by Cyclone V Devices

| Mode | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) | Decompression | Design Security | Partial Reconfiguration ⁽¹⁸⁾ | Remote System Update |
|--|----------------------|----------------------|----------------------|---------------|-----------------|---|-----------------------|
| AS through the EPCS and EPCQ serial configuration device | 1 bit, 4 bits | 100 | — | Yes | Yes | — | Yes |
| PS through CPLD or external microcontroller | 1 bit | 125 | 125 | Yes | Yes | — | — |
| FPP | 8 bits | 125 | — | Yes | Yes | — | Parallel flash loader |
| | 16 bits | 125 | — | Yes | Yes | Yes | |
| CvP (PCIe) | x1, x2, and x4 lanes | — | — | Yes | Yes | Yes | — |
| JTAG | 1 bit | 33 | 33 | — | — | — | — |

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

Related Information

[Configuration via Protocol \(CvP\) Implementation in Intel FPGAs User Guide](#)

Provides more information about CvP.

⁽¹⁸⁾ The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



| Date | Version | Changes |
|---------------|------------|---|
| July 2014 | 2014.07.07 | Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices. |
| December 2013 | 2013.12.26 | <ul style="list-style-type: none"> Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz. Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables. Removed the note "The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE. Added link to Altera Product Selector for each device variant. Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers. Added leaded package options. Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table. Corrected max LVDS counts for transmitter and receiver for Cyclone V E A5 device from 84 to 60. Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 140 to 120. Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 58 to 84. Corrected 18 x 18 multiplier for Cyclone V SE devices from 116 to 168. Corrected 9 x 9 multiplier for Cyclone V SE devices from 174 to 252. Corrected LVDS transmitter for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32. Corrected LVDS receiver for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 35 to 37. Corrected transceiver speed grade for Cyclone V ST devices ordering code from 4 to 5. Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency from 300 to 303 for voltage 1.35V. Added links to Altera's External Memory Spec Estimator tool to the topics listing the external memory interface performance. Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V. Added decompression support for the CvP configuration mode. |
| May 2013 | 2013.05.06 | <ul style="list-style-type: none"> Added link to the known document issues in the Knowledge Base. Moved all links to the Related Information section of respective topics for easy reference. Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2. Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'. Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'. Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'. Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3. Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'. Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values. Updated the package plan with M383 for the Cyclone V E device. Removed the M301 and M383 packages from the Cyclone V GX C4 device. Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device. Updated 5 Gbps to '6.144 Gbps' for Cyclone V GT device. |

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