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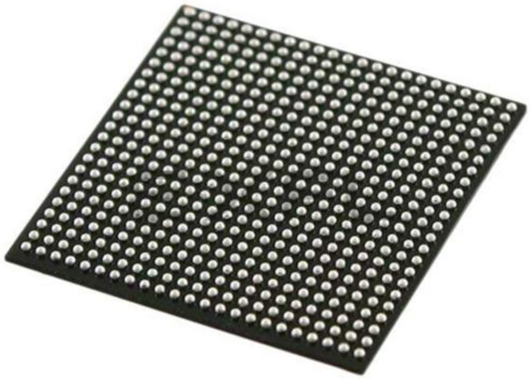
Intel - 5CGTFD5C5F23I7 Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	29080
Number of Logic Elements/Cells	77000
Total RAM Bits	5001216
Number of I/O	240
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cgtfd5c5f23i7

Cyclone V Device Overview

The Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

Related Information

Cyclone V Device Handbook: Known Issues
Lists the planned updates to the Cyclone V Device Handbook chapters.

Key Advantages of Cyclone V Devices

Table 1. Key Advantages of the Cyclone V Device Family

Advantage	Supporting Feature
Lower power consumption	• Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks • Up to 40% lower power consumption than the previous generation device
Improved logic integration and differentiation capabilities	• 8-input adaptive logic module (ALM) • Up to 13.59 megabits (Mb) of embedded memory • Variable-precision digital signal processing (DSP) blocks
Increased bandwidth capacity	• 3.125 gigabits per second (Gbps) and 6.144 Gbps transceivers • Hard memory controllers
Hard processor system (HPS) with integrated Arm* Cortex*-A9 MPCore* processor	• Tight integration of a dual-core Arm Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC) • Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric
Lowest system cost	• Requires only two core voltages to operate • Available in low-cost wirebond packaging • Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration

Summary of Cyclone V Features

Table 2. Summary of Features for Cyclone V Devices

Feature	Description	
Technology	• TSMC's 28-nm low-power (28LP) process technology • 1.1 V core voltage	
Packaging	• Wirebond low-halogen packages • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS-compliant and leaded(1)options	
High-performance FPGA fabric	Enhanced 8-input ALM with four registers	
Internal memory blocks	• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC) • Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory	
Embedded Hard IP blocks	Variable-precision DSP	• Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block • 64-bit accumulator and cascade • Embedded internal coefficient memory • Preadder/subtractor for improved efficiency
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support
	Embedded transceiver I/O	PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
Clock networks	• Up to 550 MHz global clock network • Global, quadrant, and peripheral clock networks • Clock networks that are not used can be powered down to reduce dynamic power	
Phase-locked loops (PLLs)	• Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) • Integer mode and fractional mode	
FPGA General-purpose I/Os (GPIOs)	• 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter • 400 MHz/800 Mbps external memory interface • On-chip termination (OCT) • 3.3 V support with up to 16 mA drive strength	
Low-power high-speed serial interface	• 614 Mbps to 6.144 Gbps integrated transceiver speed • Transmit pre-emphasis and receiver equalization • Dynamic partial reconfiguration of individual channels	
HPS (Cyclone V SE, SX, and ST devices only)	• Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing • Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I^2C interface, and up to 85 HPS GPIO interfaces • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • On-chip RAM and boot ROM	

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(1) Contact Intel for availability.