

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

Product Status	Active
Number of LABs/CLBs	29080
Number of Logic Elements/Cells	77000
Total RAM Bits	5001216
Number of I/O	175
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	383-TFBGA
Supplier Device Package	383-MBGA (13x13)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5cgtf5c5m13c7n">https://www.e-xfl.com/product-detail/intel/5cgtf5c5m13c7n</a>



## Cyclone V Device Overview

The Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

### Related Information

[Cyclone V Device Handbook: Known Issues](#)

Lists the planned updates to the Cyclone V Device Handbook chapters.

## Key Advantages of Cyclone V Devices

**Table 1. Key Advantages of the Cyclone V Device Family**

Advantage	Supporting Feature
Lower power consumption	<ul style="list-style-type: none"> <li>Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks</li> <li>Up to 40% lower power consumption than the previous generation device</li> </ul>
Improved logic integration and differentiation capabilities	<ul style="list-style-type: none"> <li>8-input adaptive logic module (ALM)</li> <li>Up to 13.59 megabits (Mb) of embedded memory</li> <li>Variable-precision digital signal processing (DSP) blocks</li> </ul>
Increased bandwidth capacity	<ul style="list-style-type: none"> <li>3.125 gigabits per second (Gbps) and 6.144 Gbps transceivers</li> <li>Hard memory controllers</li> </ul>
Hard processor system (HPS) with integrated Arm* Cortex*-A9 MPCore* processor	<ul style="list-style-type: none"> <li>Tight integration of a dual-core Arm Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC)</li> <li>Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric</li> </ul>
Lowest system cost	<ul style="list-style-type: none"> <li>Requires only two core voltages to operate</li> <li>Available in low-cost wirebond packaging</li> <li>Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration</li> </ul>

Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

\*Other names and brands may be claimed as the property of others.

**ISO  
9001:2008  
Registered**



## Summary of Cyclone V Features

Table 2. Summary of Features for Cyclone V Devices

Feature	Description	
Technology	<ul style="list-style-type: none"><li>• TSMC's 28-nm low-power (28LP) process technology</li><li>• 1.1 V core voltage</li></ul>	
Packaging	<ul style="list-style-type: none"><li>• Wirebond low-halogen packages</li><li>• Multiple device densities with compatible package footprints for seamless migration between different device densities</li><li>• RoHS-compliant and leaded<sup>(1)</sup> options</li></ul>	
High-performance FPGA fabric	Enhanced 8-input ALM with four registers	
Internal memory blocks	<ul style="list-style-type: none"><li>• M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC)</li><li>• Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory</li></ul>	
Embedded Hard IP blocks	Variable-precision DSP	<ul style="list-style-type: none"><li>• Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block</li><li>• 64-bit accumulator and cascade</li><li>• Embedded internal coefficient memory</li><li>• Padder/subtractor for improved efficiency</li></ul>
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support
	Embedded transceiver I/O	PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
Clock networks	<ul style="list-style-type: none"><li>• Up to 550 MHz global clock network</li><li>• Global, quadrant, and peripheral clock networks</li><li>• Clock networks that are not used can be powered down to reduce dynamic power</li></ul>	
Phase-locked loops (PLLs)	<ul style="list-style-type: none"><li>• Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)</li><li>• Integer mode and fractional mode</li></ul>	
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"><li>• 875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter</li><li>• 400 MHz/800 Mbps external memory interface</li><li>• On-chip termination (OCT)</li><li>• 3.3 V support with up to 16 mA drive strength</li></ul>	
Low-power high-speed serial interface	<ul style="list-style-type: none"><li>• 614 Mbps to 6.144 Gbps integrated transceiver speed</li><li>• Transmit pre-emphasis and receiver equalization</li><li>• Dynamic partial reconfiguration of individual channels</li></ul>	
HPS (Cyclone V SE, SX, and ST devices only)	<ul style="list-style-type: none"><li>• Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing</li><li>• Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-GO (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I<sup>2</sup>C interface, and up to 85 HPS GPIO interfaces</li><li>• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li><li>• On-chip RAM and boot ROM</li></ul>	
continued...		

<sup>(1)</sup> Contact Intel for availability.



Feature	Description
	<ul style="list-style-type: none"> <li>HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li> <li>FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller</li> <li>Arm CoreSight™ JTAG debug access port, trace port, and on-chip trace storage</li> </ul>
Configuration	<ul style="list-style-type: none"> <li>Tamper protection—comprehensive design protection to protect your valuable IP investments</li> <li>Enhanced advanced encryption standard (AES) design security features</li> <li>CvP</li> <li>Dynamic reconfiguration of the FPGA</li> <li>Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8 and x16 configuration options</li> <li>Internal scrubbing <sup>(2)</sup></li> <li>Partial reconfiguration <sup>(3)</sup></li> </ul>

## Cyclone V Device Variants and Packages

**Table 3. Device Variants for the Cyclone V Device Family**

Variant	Description
Cyclone V E	Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications
Cyclone V GX	Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications
Cyclone V GT	The FPGA industry's lowest cost and lowest power requirement for 6.144 Gbps transceiver applications
Cyclone V SE	SoC with integrated Arm-based HPS
Cyclone V SX	SoC with integrated Arm-based HPS and 3.125 Gbps transceivers
Cyclone V ST	SoC with integrated Arm-based HPS and 6.144 Gbps transceivers

## Cyclone V E

This section provides the available options, maximum resource counts, and package plan for the Cyclone V E devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Product Selector Guide.

### Related Information

#### Product Selector Guide

Provides the latest information about Intel products.

- 
- <sup>(2)</sup> The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.
- <sup>(3)</sup> The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel® sales representatives.



## Available Options

**Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices**

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



## Maximum Resources

**Table 4. Maximum Resource Counts for Cyclone V E Devices**

Resource		Member Code				
		A2	A4	A5	A7	A9
Logic Elements (LE) (K)		25	49	77	150	301
ALM		9,430	18,480	29,080	56,480	113,560
Register		37,736	73,920	116,320	225,920	454,240
Memory (Kb)	M10K	1,760	3,080	4,460	6,860	12,200
	MLAB	196	303	424	836	1,717
Variable-precision DSP Block		25	66	150	156	342
18 x 18 Multiplier		50	132	300	312	684
PLL		4	4	6	7	8
GPIO		224	224	240	480	480
LVDS	Transmitter	56	56	60	120	120
	Receiver	56	56	60	120	120
Hard Memory Controller		1	1	2	2	2



## Available Options

**Figure 3. Sample Ordering Code and Available Options for Cyclone V GT Devices**



## Maximum Resources

**Table 8. Maximum Resource Counts for Cyclone V GT Devices**

Resource		Member Code		
		D5	D7	D9
Logic Elements (LE) (K)		77	150	301
ALM		29,080	56,480	113,560
Register		116,320	225,920	454,240
Memory (Kb)	M10K	4,460	6,860	12,200
	MLAB	424	836	1,717
Variable-precision DSP Block		150	156	342
18 x 18 Multiplier		300	312	684
PLL		6	7	8
6 Gbps Transceiver		6	9	12
GPIO <sup>(5)</sup>		336	480	560
LVDS	Transmitter	84	120	140

**continued...**

<sup>(5)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



## Cyclone V SE

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SE devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

#### Product Selector Guide

Provides the latest information about Intel products.

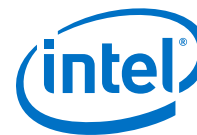
## Available Options

### Figure 4. Sample Ordering Code and Available Options for Cyclone V SE Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.





## Maximum Resources

**Table 10. Maximum Resource Counts for Cyclone V SE Devices**

Resource		Member Code			
		A2	A4	A5	A6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,430	15,880	32,070	41,910
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6
HPS PLL		3	3	3	3
FPGA GPIO		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 11. Package Plan for Cyclone V SE Devices**

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U484 (19 mm)		U672 (23 mm)		F896 (31 mm)	
	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O	FPGA GPIO	HPS I/O
A2	66	151	145	181	—	—
A4	66	151	145	181	—	—
A5	66	151	145	181	288	181
A6	66	151	145	181	288	181





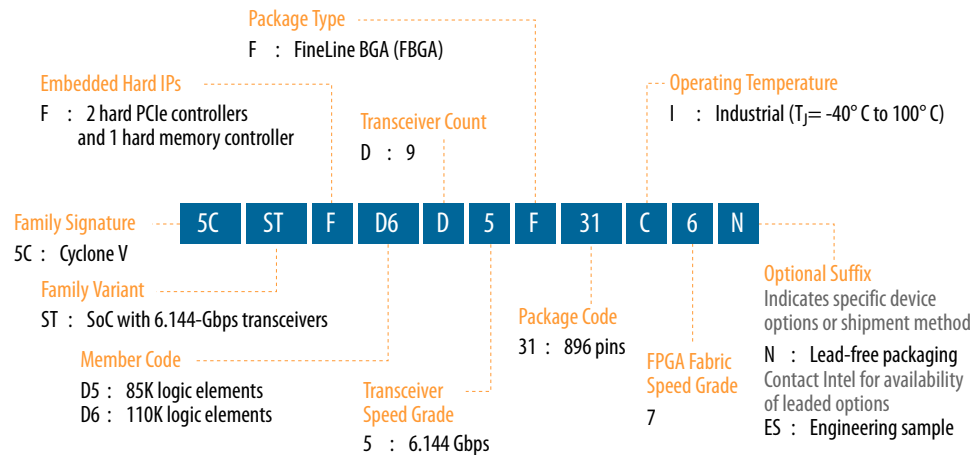
## Related Information

### Product Selector Guide

Provides the latest information about Intel products.

## Available Options

**Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices**



## Maximum Resources

**Table 14. Maximum Resource Counts for Cyclone V ST Devices**

Resource		Member Code	
		D5	D6
Logic Elements (LE) (K)		85	110
ALM		32,070	41,910
Register		128,300	166,036
Memory (Kb)	M10K	3,970	5,570
	MLAB	480	621
Variable-precision DSP Block		87	112
18 x 18 Multiplier		174	224
FPGA PLL		6	6
HPS PLL		3	3
6.144 Gbps Transceiver		9	9
FPGA GPIO <sup>(10)</sup>		288	288
HPS I/O		181	181
LVDS	Transmitter	72	72
continued...			

<sup>(10)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



Resource		Member Code	
		D5	D6
	Receiver	72	72
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		1	1
HPS Hard Memory Controller		1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core

### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 15. Package Plan for Cyclone V ST Devices**

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver  $\leq 5$  Gbps. 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR
D5	288	181	9 <sup>(11)</sup>
D6	288	181	9 <sup>(11)</sup>

### Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

<sup>(11)</sup> If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

## I/O Vertical Migration for Cyclone V Devices

**Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities**

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

Variant	Member Code	Package										
		M301	M383	M484	F256	U324	U484	F484	U672	F672	F896	F1152
Cyclone V E	A2		↕	↕		↕	↕	↕				
	A4		↕		↕	↕	↕	↕				
	A5		↕									
	A7									↕	↕	
	A9						↕	↕		↕	↕	
Cyclone V GX	C3						↕	↕		↕	↕	
	C4	↕	↕							↕		
	C5	↕	↕									
	C7										↕	
	C9						↕	↕		↕	↕	
Cyclone V GT	D5						↕	↕		↕		
	D7									↕	↕	
	D9						↕	↕		↕	↕	
Cyclone V SE	A2						↕		↕	↕		
	A4								↕	↕		
	A5										↕	
	A6						↕		↕	↕	↕	
Cyclone V SX	C2								↕	↕		
	C4								↕	↕		
	C5										↕	
	C6								↕	↕	↕	
Cyclone V ST	D5										↕	
	D6										↕	

You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

**Note:** To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

## Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.



Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier		
	C6	112	336	224	112	112	112
Cyclone V ST	D5	87	261	174	87	87	87
	D6	112	336	224	112	112	112

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

## Types of Embedded Memory

The Cyclone V devices contain two types of memory blocks:

- 10 Kb M10K blocks—blocks of dedicated memory resources. The M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Cyclone V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Cyclone V Devices

**Table 18. Embedded Memory Capacity and Distribution in Cyclone V Devices**

Variant	Member Code	M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Cyclone V E	A2	176	1,760	314	196	1,956
	A4	308	3,080	485	303	3,383
	A5	446	4,460	679	424	4,884
	A7	686	6,860	1338	836	7,696
	A9	1,220	12,200	2748	1,717	13,917
Cyclone V GX	C3	135	1,350	291	182	1,532
	C4	250	2,500	678	424	2,924
	C5	446	4,460	678	424	4,884
	C7	686	6,860	1338	836	7,696
	C9	1,220	12,200	2748	1,717	13,917
continued...						



## PLL Features

The PLLs in the Cyclone V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- User-mode reconfiguration of PLLs
- Low power mode for each fractional PLL
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation modes

## Fractional PLL

In addition to integer PLLs, the Cyclone V devices use a fractional PLL architecture. The devices have up to eight PLLs, each with nine output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

## FPGA General Purpose I/O

Cyclone V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis
- On-chip parallel termination ( $R_T$  OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture



## External Memory Performance

**Table 20. External Memory Interface Performance in Cyclone V Devices**

The maximum and minimum operating frequencies depend on the memory interface standards and the supported delay-locked loop (DLL) frequency listed in the device datasheet.

Interface	Voltage (V)	Maximum Frequency (MHz)		Minimum Frequency (MHz)
		Hard Controller	Soft Controller	
DDR3 SDRAM	1.5	400	303	303
	1.35	400	303	303
DDR2 SDRAM	1.8	400	300	167
LPDDR2 SDRAM	1.2	333	300	167

### Related Information

#### External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

## HPS External Memory Performance

**Table 21. HPS External Memory Interface Performance**

The hard processor system (HPS) is available in Cyclone V SoC devices only.

Interface	Voltage (V)	HPS Hard Controller (MHz)
DDR3 SDRAM	1.5	400
	1.35	400
DDR2 SDRAM	1.8	400
LPDDR2 SDRAM	1.2	333

### Related Information

#### External Memory Interface Spec Estimator

For the latest information and to estimate the external memory system performance specification, use Intel's External Memory Interface Spec Estimator tool.

## Low-Power Serial Transceivers

Cyclone V devices deliver the industry's lowest power 6.144 Gbps transceivers at an estimated 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant with a wide range of protocols and data rates.

## Transceiver Channels

The transceivers are positioned on the left outer edge of the device. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks.

**Figure 10. Device Chip Overview for Cyclone V GX and GT Devices**

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.



## PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

**Table 22. PMA Features of the Transceivers in Cyclone V Devices**

Features	Capability
Backplane support	Driving capability up to 6.144 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	<ul style="list-style-type: none"> <li>Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization</li> <li>No decision feedback equalizer (DFE)</li> </ul>
Ring oscillator transmit PLLs	614 Mbps to 6.144 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

**Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor**



## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.



## HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to slaves in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The SDRAM controller subsystem supports DDR2, DDR3, or LPDDR2 devices up to 4 Gb in density operating at up to 400 MHz (800 Mbps data rate).

## FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Intel simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Intel Quartus Prime design software. With the Intel solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

## Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.

**Table 24. Configuration Schemes and Features Supported by Cyclone V Devices**

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(18)</sup>	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes	
CvP (PCIe)	x1, x2, and x4 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

### Related Information

[Configuration via Protocol \(CvP\) Implementation in Intel FPGAs User Guide](#)

Provides more information about CvP.

<sup>(18)</sup> The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



Date	Version	Changes
		<ul style="list-style-type: none"> <li>Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: <ul style="list-style-type: none"> <li>Cyclone V GX C3: Updated from 181 to 182</li> <li>Cyclone V GX C4: Updated from 295 to 424</li> </ul> </li> <li>Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: <ul style="list-style-type: none"> <li>Cyclone V GX C3: Updated from 1,531 to 1,532</li> <li>Cyclone V GX C4: Updated from 2,795 to 2,924</li> </ul> </li> <li>Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: <ul style="list-style-type: none"> <li>Cyclone V GX C4: Updated from 472 to 678</li> <li>Cyclone V GX C5: Updated from 679 to 678</li> </ul> </li> </ul>
March 2015	2015.03.31	<ul style="list-style-type: none"> <li>Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table.</li> <li>Added optional suffix "SC: Internal scrubbing support" to the following diagrams: <ul style="list-style-type: none"> <li>Sample Ordering Code and Available Options for Cyclone V E Devices</li> <li>Sample Ordering Code and Available Options for Cyclone V GX Devices</li> <li>Sample Ordering Code and Available Options for Cyclone V SE Devices</li> <li>Sample Ordering Code and Available Options for Cyclone V SX Devices</li> </ul> </li> </ul>
January 2015	2015.01.23	<ul style="list-style-type: none"> <li>Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and -7 speed grade. <ul style="list-style-type: none"> <li>Operating Temperature: Removed C and A temperature grades</li> <li>FPGA Fabric Speed Grade: Removed -6 and -8 speed grades</li> </ul> </li> <li>Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps: <ul style="list-style-type: none"> <li>Device Variants for the Cyclone V Device Family table</li> <li>Sample Ordering Code and Available Options for Cyclone V ST Devices figure</li> <li>Maximum Resource Counts for Cyclone V ST Devices</li> </ul> </li> <li>Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices. <ul style="list-style-type: none"> <li>Logic elements (LE) (K): Updated from 35.7 to 35.5</li> <li>Variable-precision DSP block: Updated from 51 to 57</li> <li>18 x 18 multiplier: Updated from 102 to 114</li> </ul> </li> <li>Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices. <ul style="list-style-type: none"> <li>Variableprecision DSP Block: Updated from 51 to 57</li> <li>9 x 9 Multiplier: Updated from 153 to 171</li> <li>18 x 18 Multiplier: Updated from 102 to 114</li> <li>27 x 27 Multiplier: Updated from 51 to 57</li> <li>18 x 18 Multiplier Adder Mode: Updated from 51 to 57</li> <li>18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57</li> </ul> </li> <li>Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices. <ul style="list-style-type: none"> <li>M10K block: Updated from 119 to 135</li> <li>M10K RAM bit (Kb): Updated from 1,190 to 1,350</li> <li>MLAB block: Updated from 255 to 291</li> <li>MLAB RAM bit (Kb): Updated from 159 to 181</li> <li>Total RAM bit (Kb): Updated from 1,349 to 1,531</li> </ul> </li> </ul>
October 2014	2014.10.06	Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices.
<b>continued...</b>		



Date	Version	Changes
July 2014	2014.07.07	Updated the I/O vertical migration figure to clarify the migration capability of Cyclone V SE and SX devices.
December 2013	2013.12.26	<ul style="list-style-type: none"> <li>Corrected single or dual-core ARM Cortex-A9 MPCore processor-up to 925 MHz from 800 MHz.</li> <li>Removed "Preliminary" texts from Ordering Code figures, Maximum Resources, Package Plan and I/O Vertical Migration tables.</li> <li>Removed the note "The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os." for GPIOs in the Maximum Resource Counts table for Cyclone V E and SE.</li> <li>Added link to <a href="#">Altera Product Selector</a> for each device variant.</li> <li>Updated Embedded Hard IPs for Cyclone V GT devices to indicate Maximum 2 hard PCIe and 2 hard memory controllers.</li> <li>Added leaded package options.</li> <li>Removed the note "The number of PLLs includes general-purpose fractional PLLs and transceiver fractional PLLs." for all PLLs in the Maximum Resource Counts table.</li> <li>Corrected max LVDS counts for transmitter and receiver for Cyclone V E A5 device from 84 to 60.</li> <li>Corrected max LVDS counts for transmitter and receiver for Cyclone V E A9 device from 140 to 120.</li> <li>Corrected variable-precision DSP block, 27 x 27 multiplier, 18 x 18 multiplier adder mode and 18 x 18 multiplier adder summed with 36 bit input for Cyclone V SE devices from 58 to 84.</li> <li>Corrected 18 x 18 multiplier for Cyclone V SE devices from 116 to 168.</li> <li>Corrected 9 x 9 multiplier for Cyclone V SE devices from 174 to 252.</li> <li>Corrected LVDS transmitter for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 31 to 32.</li> <li>Corrected LVDS receiver for Cyclone V SE A2 and A4 as well as SX C2 and C4 devices from 35 to 37.</li> <li>Corrected transceiver speed grade for Cyclone V ST devices ordering code from 4 to 5.</li> <li>Updated the DDR3 SDRAM for the maximum frequency's soft controller and the minimum frequency from 300 to 303 for voltage 1.35V.</li> <li>Added links to Altera's <a href="#">External Memory Spec Estimator</a> tool to the topics listing the external memory interface performance.</li> <li>Corrected XAUI is supported through the soft PCS in the PCS features for Cyclone V.</li> <li>Added decompression support for the CvP configuration mode.</li> </ul>
May 2013	2013.05.06	<ul style="list-style-type: none"> <li>Added link to the known document issues in the Knowledge Base.</li> <li>Moved all links to the Related Information section of respective topics for easy reference.</li> <li>Corrected the title to the PCIe hard IP topic. Cyclone V devices support only PCIe Gen1 and Gen2.</li> <li>Updated Supporting Feature in Table 1 of Increased bandwidth capacity to '6.144 Gbps'.</li> <li>Updated Description in Table 2 of Low-power high-speed serial interface to '6.144 Gbps'.</li> <li>Updated Description in Table 3 of Cyclone V GT to '6.144 Gbps'.</li> <li>Updated the M386 package to M383 for Figure 1, Figure 2 and Figure 3.</li> <li>Updated Figure 2 and Figure 3 for Transceiver Count by adding 'F : 4'.</li> <li>Updated LVDS in the Maximum Resource Counts tables to include Transmitter and Receiver values.</li> <li>Updated the package plan with M383 for the Cyclone V E device.</li> <li>Removed the M301 and M383 packages from the Cyclone V GX C4 device.</li> <li>Updated the GPIO count to '129' for the M301 package of the Cyclone V GX C5 device.</li> <li>Updated 5 Gbps to '6.144 Gbps' for Cyclone V GT device.</li> </ul>

continued...



Date	Version	Changes
		<ul style="list-style-type: none"> <li>Updated HPS I/O for U484 (19 mm) in Table 11 with '151' for A2, A4, A5 and A6.</li> <li>Updated Memory (Kb) for Maximum Resource Counts for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices.</li> <li>Updated FPGA PLL for Maximum Resource Counts for Cyclone V SE A2, SX C2, devices.</li> <li>Removed '36 x 36' from the Variable-Precision DSP Block.</li> <li>Updated Variable-precision DSP Blocks and 18 x 18 Multiplier for Maximum Resource Counts for Cyclone V SX C4 device.</li> <li>Updated the HPS I/O counts for Cyclone V SE, SX, and ST devices.</li> <li>Updated Figure 7 which shows the I/O vertical migration table.</li> <li>Updated Table 17 for Cyclone V SX C4 device.</li> <li>Updated Embedded Memory Capacity and Distribution table for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices.</li> <li>Removed 'Counter reconfiguration' from the PLL Features.</li> <li>Updated Low-Power Serial Transceivers by replacing 5 Gbps with 6.144 Gbps.</li> <li>Removed 'Distributed Memory' symbol.</li> <li>Updated the Capability in Table 22 of Backplane support to '6.144 Gbps'.</li> <li>Updated Capability in Table 22 of Ring oscillator transmit PLLs with 6.144 Gbps.</li> <li>Updated the PCS Support in Table 23 from 5 Gbps to '6 Gbps'.</li> <li>Updated the Data Rates (Gbps) in Table 23 of 3 Gbps and 6 Gbps Basic to '6.144 Gbps'.</li> <li>Updated the Data Rates (Gbps) in Table 23 of CPRI 4.1 to '6.144 Gbps'.</li> <li>Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.</li> </ul>
December 2012	2012.12.28	<ul style="list-style-type: none"> <li>Updated the pin counts for the MBGA packages.</li> <li>Updated the GPIO and transceiver counts for the MBGA packages.</li> <li>Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices.</li> <li>Updated the vertical migration table for vertical migration of the U484 packages.</li> <li>Updated the MLAB supported programmable widths at 32 bits depth.</li> </ul>
November 2012	2012.11.19	<ul style="list-style-type: none"> <li>Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT.</li> <li>Added ordering code for five-transceiver devices for Cyclone V GT and ST.</li> <li>Updated the vertical migration table to add MBGA packages.</li> <li>Added performance information for HPS memory controller.</li> <li>Removed DDR3U support.</li> <li>Updated Cyclone V ST speed grade information.</li> <li>Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance.</li> <li>Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software.</li> <li>Updated template.</li> </ul>
July 2012	2.1	Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible)
June 2012	2.0	<ul style="list-style-type: none"> <li>Restructured the document.</li> <li>Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections.</li> <li>Added Table 1, Table 3, Table 16, Table 19, and Table 20.</li> <li>Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18.</li> </ul>

**continued...**