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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Active  |
| Number of LABs/CLBs            | 56480   |
| Number of Logic Elements/Cells | 149500  |
| Total RAM Bits                 | 7880704   |
| Number of I/O                  | 240   |
| Number of Gates                | -   |
| Voltage - Supply               | 1.07V ~ 1.13V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | 0°C ~ 85°C (TJ)   |
| Package / Case                 | 484-FBGA  |
| Supplier Device Package        | 484-UBGA (19x19)  |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/5cgtfd7c5u19c7n">https://www.e-xfl.com/product-detail/intel/5cgtfd7c5u19c7n</a> |



| Feature       | Description   |
|---------------|---|
|               | <ul style="list-style-type: none"> <li>HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li> <li>FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end (MPFE) of the HPS SDRAM controller</li> <li>Arm CoreSight™ JTAG debug access port, trace port, and on-chip trace storage</li> </ul>  |
| Configuration | <ul style="list-style-type: none"> <li>Tamper protection—comprehensive design protection to protect your valuable IP investments</li> <li>Enhanced advanced encryption standard (AES) design security features</li> <li>CvP</li> <li>Dynamic reconfiguration of the FPGA</li> <li>Active serial (AS) x1 and x4, passive serial (PS), JTAG, and fast passive parallel (FPP) x8 and x16 configuration options</li> <li>Internal scrubbing <sup>(2)</sup></li> <li>Partial reconfiguration <sup>(3)</sup></li> </ul> |

## Cyclone V Device Variants and Packages

**Table 3. Device Variants for the Cyclone V Device Family**

| Variant      | Description  |
|--------------|--|
| Cyclone V E  | Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications |
| Cyclone V GX | Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications              |
| Cyclone V GT | The FPGA industry's lowest cost and lowest power requirement for 6.144 Gbps transceiver applications                 |
| Cyclone V SE | SoC with integrated Arm-based HPS  |
| Cyclone V SX | SoC with integrated Arm-based HPS and 3.125 Gbps transceivers  |
| Cyclone V ST | SoC with integrated Arm-based HPS and 6.144 Gbps transceivers  |

## Cyclone V E

This section provides the available options, maximum resource counts, and package plan for the Cyclone V E devices.

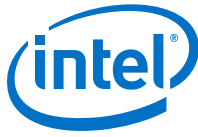
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Product Selector Guide.

### Related Information

#### [Product Selector Guide](#)

Provides the latest information about Intel products.

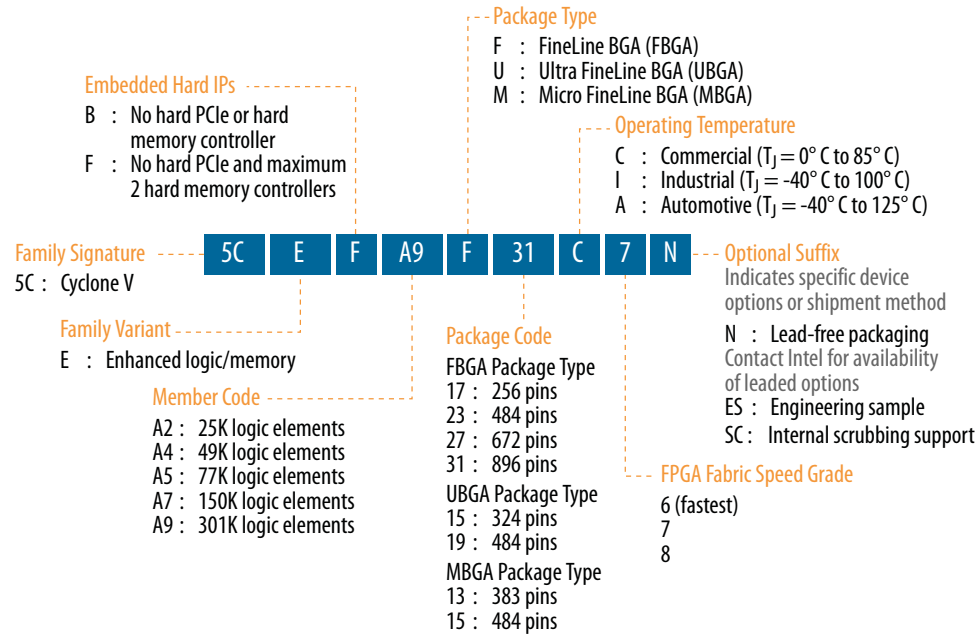
- 
- <sup>(2)</sup> The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.
- <sup>(3)</sup> The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel® sales representatives.



## Available Options

**Figure 1. Sample Ordering Code and Available Options for Cyclone V E Devices**

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



## Maximum Resources

**Table 4. Maximum Resource Counts for Cyclone V E Devices**

| Resource                     |             | Member Code |        |         |         |         |
|------------------------------|-------------|-------------|--------|---------|---------|---------|
|                              |             | A2          | A4     | A5      | A7      | A9      |
| Logic Elements (LE) (K)      |             | 25          | 49     | 77      | 150     | 301     |
| ALM                          |             | 9,430       | 18,480 | 29,080  | 56,480  | 113,560 |
| Register                     |             | 37,736      | 73,920 | 116,320 | 225,920 | 454,240 |
| Memory (Kb)                  | M10K        | 1,760       | 3,080  | 4,460   | 6,860   | 12,200  |
|                              | MLAB        | 196         | 303    | 424     | 836     | 1,717   |
| Variable-precision DSP Block |             | 25          | 66     | 150     | 156     | 342     |
| 18 x 18 Multiplier           |             | 50          | 132    | 300     | 312     | 684     |
| PLL                          |             | 4           | 4      | 6       | 7       | 8       |
| GPIO                         |             | 224         | 224    | 240     | 480     | 480     |
| LVDS                         | Transmitter | 56          | 56     | 60      | 120     | 120     |
|                              | Receiver    | 56          | 56     | 60      | 120     | 120     |
| Hard Memory Controller       |             | 1           | 1      | 2       | 2       | 2       |



### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

### Package Plan

**Table 5. Package Plan for Cyclone V E Devices**

| Member Code | M383<br>(13 mm) | M484<br>(15 mm) | U324<br>(15 mm) | F256<br>(17 mm) | U484<br>(19 mm) | F484<br>(23 mm) | F672<br>(27 mm) | F896<br>(31 mm) |
|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
|             | GPIO            | GPIO            | GPIO            | GPIO            | GPIO            | GPIO            | GPIO            | GPIO            |
| A2          | 223             | —               | 176             | 128             | 224             | 224             | —               | —               |
| A4          | 223             | —               | 176             | 128             | 224             | 224             | —               | —               |
| A5          | 175             | —               | —               | —               | 224             | 240             | —               | —               |
| A7          | —               | 240             | —               | —               | 240             | 240             | 336             | 480             |
| A9          | —               | —               | —               | —               | 240             | 224             | 336             | 480             |

### Cyclone V GX

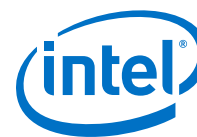
This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

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Provides the latest information about Intel products.



| Resource               |             | Member Code |    |    |     |     |
|------------------------|-------------|-------------|----|----|-----|-----|
|                        |             | C3          | C4 | C5 | C7  | C9  |
| LVDS                   | Transmitter | 52          | 84 | 84 | 120 | 140 |
|                        | Receiver    | 52          | 84 | 84 | 120 | 140 |
| PCIe Hard IP Block     |             | 1           | 2  | 2  | 2   | 2   |
| Hard Memory Controller |             | 1           | 2  | 2  | 2   | 2   |

### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 7. Package Plan for Cyclone V GX Devices**

| Member Code | M301<br>(11 mm) |      | M383<br>(13 mm) |      | M484<br>(15 mm) |      | U324<br>(15 mm) |      | U484<br>(19 mm) |      |
|-------------|-----------------|------|-----------------|------|-----------------|------|-----------------|------|-----------------|------|
|             | GPIO            | XCVR | GPIO            | XCVR | GPIO            | XCVR | GPIO            | XCVR | GPIO            | XCVR |
| C3          | —               | —    | —               | —    | —               | —    | 144             | 3    | 208             | 3    |
| C4          | 129             | 4    | 175             | 6    | —               | —    | —               | —    | 224             | 6    |
| C5          | 129             | 4    | 175             | 6    | —               | —    | —               | —    | 224             | 6    |
| C7          | —               | —    | —               | —    | 240             | 3    | —               | —    | 240             | 6    |
| C9          | —               | —    | —               | —    | —               | —    | —               | —    | 240             | 5    |

| Member Code | F484<br>(23 mm) |      | F672<br>(27 mm) |      | F896<br>(31 mm) |      | F1152<br>(35 mm) |      |
|-------------|-----------------|------|-----------------|------|-----------------|------|------------------|------|
|             | GPIO            | XCVR | GPIO            | XCVR | GPIO            | XCVR | GPIO             | XCVR |
| C3          | 208             | 3    | —               | —    | —               | —    | —                | —    |
| C4          | 240             | 6    | 336             | 6    | —               | —    | —                | —    |
| C5          | 240             | 6    | 336             | 6    | —               | —    | —                | —    |
| C7          | 240             | 6    | 336             | 9    | 480             | 9    | —                | —    |
| C9          | 224             | 6    | 336             | 9    | 480             | 12   | 560              | 12   |

## Cyclone V GT

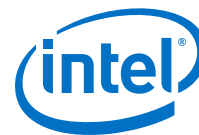
This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

[Product Selector Guide](#)

Provides the latest information about Intel products.



| Resource               |          | Member Code |     |     |
|------------------------|----------|-------------|-----|-----|
|                        |          | D5          | D7  | D9  |
|                        | Receiver | 84          | 120 | 140 |
| PCIe Hard IP Block     |          | 2           | 2   | 2   |
| Hard Memory Controller |          | 2           | 2   | 2   |

### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 9. Package Plan for Cyclone V GT Devices**

Transceiver counts shown are for transceiver ≤5 Gbps . 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

| Member Code | M301<br>(11 mm) |      | M383<br>(13 mm) |      | M484<br>(15 mm) |      | U484<br>(19 mm) |      |
|-------------|-----------------|------|-----------------|------|-----------------|------|-----------------|------|
|             | GPIO            | XCVR | GPIO            | XCVR | GPIO            | XCVR | GPIO            | XCVR |
| D5          | 129             | 4    | 175             | 6    | —               | —    | 224             | 6    |
| D7          | —               | —    | —               | —    | 240             | 3    | 240             | 6    |
| D9          | —               | —    | —               | —    | —               | —    | 240             | 5    |

| Member Code | F484<br>(23 mm) |      | F672<br>(27 mm) |                  | F896<br>(31 mm) |                   | F1152<br>(35 mm) |                   |
|-------------|-----------------|------|-----------------|------------------|-----------------|-------------------|------------------|-------------------|
|             | GPIO            | XCVR | GPIO            | XCVR             | GPIO            | XCVR              | GPIO             | XCVR              |
| D5          | 240             | 6    | 336             | 6                | —               | —                 | —                | —                 |
| D7          | 240             | 6    | 336             | 9 <sup>(6)</sup> | 480             | 9 <sup>(6)</sup>  | —                | —                 |
| D9          | 224             | 6    | 336             | 9 <sup>(6)</sup> | 480             | 12 <sup>(7)</sup> | 560              | 12 <sup>(7)</sup> |

### Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

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- <sup>(6)</sup> If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.
- <sup>(7)</sup> If you require CPRI (at 6.144 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to three full-duplex transceiver channels for CPRI, and up to eight full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.



## Cyclone V SX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

#### Product Selector Guide

Provides the latest information about Intel products.

## Available Options

### Figure 5. Sample Ordering Code and Available Options for Cyclone V SX Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Cyclone V SE and SX low-power devices (L power option) offer 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE.



## Maximum Resources

**Table 12. Maximum Resource Counts for Cyclone V SX Devices**

| Resource                     |      | Member Code |        |         |         |
|------------------------------|------|-------------|--------|---------|---------|
|                              |      | C2          | C4     | C5      | C6      |
| Logic Elements (LE) (K)      |      | 25          | 40     | 85      | 110     |
| ALM                          |      | 9,430       | 15,880 | 32,070  | 41,910  |
| Register                     |      | 37,736      | 60,376 | 128,300 | 166,036 |
| Memory (Kb)                  | M10K | 1,400       | 2,700  | 3,970   | 5,570   |
|                              | MLAB | 138         | 231    | 480     | 621     |
| Variable-precision DSP Block |      | 36          | 84     | 87      | 112     |
| 18 x 18 Multiplier           |      | 72          | 168    | 174     | 224     |
| FPGA PLL                     |      | 5           | 5      | 6       | 6       |

*continued...*



| Resource                       |             | Member Code |           |                  |                  |
|--------------------------------|-------------|-------------|-----------|------------------|------------------|
|                                |             | C2          | C4        | C5               | C6               |
| HPS PLL                        |             | 3           | 3         | 3                | 3                |
| 3 Gbps Transceiver             |             | 6           | 6         | 9                | 9                |
| FPGA GPIO <sup>(8)</sup>       |             | 145         | 145       | 288              | 288              |
| HPS I/O                        |             | 181         | 181       | 181              | 181              |
| LVDS                           | Transmitter | 32          | 32        | 72               | 72               |
|                                | Receiver    | 37          | 37        | 72               | 72               |
| PCIe Hard IP Block             |             | 2           | 2         | 2 <sup>(9)</sup> | 2 <sup>(9)</sup> |
| FPGA Hard Memory Controller    |             | 1           | 1         | 1                | 1                |
| HPS Hard Memory Controller     |             | 1           | 1         | 1                | 1                |
| Arm Cortex-A9 MPCore Processor |             | Dual-core   | Dual-core | Dual-core        | Dual-core        |

### Related Information

#### True LVDS Buffers in Devices, I/O Features in Cyclone V Devices

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 13. Package Plan for Cyclone V SX Devices**

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

| Member Code | U672<br>(23 mm) |         |      | F896<br>(31 mm) |         |      |
|-------------|-----------------|---------|------|-----------------|---------|------|
|             | FPGA GPIO       | HPS I/O | XCVR | FPGA GPIO       | HPS I/O | XCVR |
| C2          | 145             | 181     | 6    | —               | —       | —    |
| C4          | 145             | 181     | 6    | —               | —       | —    |
| C5          | 145             | 181     | 6    | 288             | 181     | 9    |
| C6          | 145             | 181     | 6    | 288             | 181     | 9    |

## Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(9)</sup> 1 PCIe Hard IP Block in U672 package.





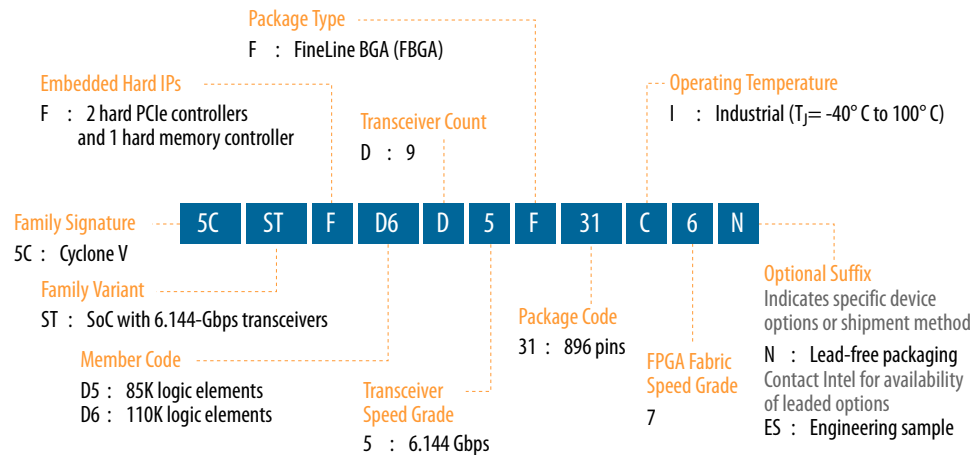
## Related Information

### Product Selector Guide

Provides the latest information about Intel products.

## Available Options

**Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices**



## Maximum Resources

**Table 14. Maximum Resource Counts for Cyclone V ST Devices**

| Resource                     |             | Member Code |         |
|------------------------------|-------------|-------------|---------|
|                              |             | D5          | D6      |
| Logic Elements (LE) (K)      |             | 85          | 110     |
| ALM                          |             | 32,070      | 41,910  |
| Register                     |             | 128,300     | 166,036 |
| Memory (Kb)                  | M10K        | 3,970       | 5,570   |
|                              | MLAB        | 480         | 621     |
| Variable-precision DSP Block |             | 87          | 112     |
| 18 x 18 Multiplier           |             | 174         | 224     |
| FPGA PLL                     |             | 6           | 6       |
| HPS PLL                      |             | 3           | 3       |
| 6.144 Gbps Transceiver       |             | 9           | 9       |
| FPGA GPIO <sup>(10)</sup>    |             | 288         | 288     |
| HPS I/O                      |             | 181         | 181     |
| LVDS                         | Transmitter | 72          | 72      |
| continued...                 |             |             |         |

<sup>(10)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.



| Resource                       |          | Member Code |           |
|--------------------------------|----------|-------------|-----------|
|                                |          | D5          | D6        |
|                                | Receiver | 72          | 72        |
| PCIe Hard IP Block             |          | 2           | 2         |
| FPGA Hard Memory Controller    |          | 1           | 1         |
| HPS Hard Memory Controller     |          | 1           | 1         |
| Arm Cortex-A9 MPCore Processor |          | Dual-core   | Dual-core |

### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 15. Package Plan for Cyclone V ST Devices**

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver  $\leq 5$  Gbps. 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

| Member Code | F896<br>(31 mm) |         |                   |
|-------------|-----------------|---------|-------------------|
|             | FPGA GPIO       | HPS I/O | XCVR              |
| D5          | 288             | 181     | 9 <sup>(11)</sup> |
| D6          | 288             | 181     | 9 <sup>(11)</sup> |

### Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

<sup>(11)</sup> If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

## I/O Vertical Migration for Cyclone V Devices

**Figure 7. Vertical Migration Capability Across Cyclone V Device Packages and Densities**

The arrows indicate the vertical migration paths. The devices included in each vertical migration path are shaded. You can also migrate your design across device densities in the same package option if the devices have the same dedicated pins, configuration pins, and power pins.

| Variant      | Member Code | Package                           |                                   |      |                                   |                                   |                                   |                                   |                                   |                                   |                                   |                                   |
|--------------|-------------|-----------------------------------|-----------------------------------|------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
|              |             | M301                              | M383                              | M484 | F256                              | U324                              | U484                              | F484                              | U672                              | F672                              | F896                              | F1152                             |
| Cyclone V E  | A2          |                                   | <div><div></div><div></div></div> |      | <div><div></div><div></div></div> | <div><div></div><div></div></div> | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |                                   |                                   |                                   |
|              | A4          |                                   | <div><div></div><div></div></div> |      | <div><div></div><div></div></div> | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |                                   |                                   |                                   |                                   |
|              | A5          |                                   | <div><div></div><div></div></div> |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |                                   |                                   |                                   |
|              | A7          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
|              | A9          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
| Cyclone V GX | C3          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
|              | C4          | <div><div></div><div></div></div> | <div><div></div><div></div></div> |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> |                                   |                                   |
|              | C5          | <div><div></div><div></div></div> | <div><div></div><div></div></div> |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> |                                   |                                   |
|              | C7          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
|              | C9          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
| Cyclone V GT | D5          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
|              | D7          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
|              | D9          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
| Cyclone V SE | A2          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |                                   |
|              | A4          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> |                                   |                                   |                                   |
|              | A5          |                                   |                                   |      |                                   |                                   |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |                                   |
|              | A6          |                                   |                                   |      |                                   |                                   | <div><div></div><div></div></div> |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
| Cyclone V SX | C2          |                                   |                                   |      |                                   |                                   |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |                                   |
|              | C4          |                                   |                                   |      |                                   |                                   |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |                                   |
|              | C5          |                                   |                                   |      |                                   |                                   |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
|              | C6          |                                   |                                   |      |                                   |                                   |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> | <div><div></div><div></div></div> | <div><div></div><div></div></div> |
| Cyclone V ST | D5          |                                   |                                   |      |                                   |                                   |                                   |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |
|              | D6          |                                   |                                   |      |                                   |                                   |                                   |                                   |                                   | <div><div></div><div></div></div> | <div><div></div><div></div></div> |                                   |

You can achieve the vertical migration shaded in red if you use only up to 175 GPIOs for the M383 package, and 138 GPIOs for the U672 package. These migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

**Note:** To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime software Pin Planner.

## Adaptive Logic Module

Cyclone V devices use a 28 nm ALM as the basic building block of the logic fabric.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

**Figure 8. ALM for Cyclone V Devices**



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

#### Related Information

[Embedded Memory Capacity in Cyclone V Devices](#) on page 21  
Lists the embedded memory capacity for each device.

## Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software

**Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices**

| Usage Example   | Multiplier Size (Bit)       | DSP Block Resource |
|---|-----------------------------|--------------------|
| Low precision fixed point for video applications        | Three 9 x 9                 | 1                  |
| Medium precision fixed point in FIR filters             | Two 18 x 18                 | 1                  |
| FIR filters and general DSP usage                       | Two 18 x 18 with accumulate | 1                  |
| High precision fixed- or floating-point implementations | One 27 x 27 with accumulate | 1                  |

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

**Table 17. Number of Multipliers in Cyclone V Devices**

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

| Variant      | Member Code | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    |                    | 18 x 18 Multiplier Adder Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|--------------|-------------|------------------------------|---|--------------------|--------------------|-------------------------------|---|
|              |             |                              | 9 x 9 Multiplier                                      | 18 x 18 Multiplier | 27 x 27 Multiplier |                               |   |
| Cyclone V E  | A2          | 25                           | 75  | 50                 | 25                 | 25                            | 25  |
|              | A4          | 66                           | 198   | 132                | 66                 | 66                            | 66  |
|              | A5          | 150                          | 450   | 300                | 150                | 150                           | 150   |
|              | A7          | 156                          | 468   | 312                | 156                | 156                           | 156   |
|              | A9          | 342                          | 1,026   | 684                | 342                | 342                           | 342   |
| Cyclone V GX | C3          | 57                           | 171   | 114                | 57                 | 57                            | 57  |
|              | C4          | 70                           | 210   | 140                | 70                 | 70                            | 70  |
|              | C5          | 150                          | 450   | 300                | 150                | 150                           | 150   |
|              | C7          | 156                          | 468   | 312                | 156                | 156                           | 156   |
|              | C9          | 342                          | 1,026   | 684                | 342                | 342                           | 342   |
| Cyclone V GT | D5          | 150                          | 450   | 300                | 150                | 150                           | 150   |
|              | D7          | 156                          | 468   | 312                | 156                | 156                           | 156   |
|              | D9          | 342                          | 1,026   | 684                | 342                | 342                           | 342   |
| Cyclone V SE | A2          | 36                           | 108   | 72                 | 36                 | 36                            | 36  |
|              | A4          | 84                           | 252   | 168                | 84                 | 84                            | 84  |
|              | A5          | 87                           | 261   | 174                | 87                 | 87                            | 87  |
|              | A6          | 112                          | 336   | 224                | 112                | 112                           | 112   |
| Cyclone V SX | C2          | 36                           | 108   | 72                 | 36                 | 36                            | 36  |
|              | C4          | 84                           | 252   | 168                | 84                 | 84                            | 84  |
|              | C5          | 87                           | 261   | 174                | 87                 | 87                            | 87  |
| continued... |             |                              |   |                    |                    |                               |   |



| Variant      | Member Code | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    |                    | 18 x 18 Multiplier Adder Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|--------------|-------------|------------------------------|---|--------------------|--------------------|-------------------------------|---|
|              |             |                              | 9 x 9 Multiplier                                      | 18 x 18 Multiplier | 27 x 27 Multiplier |                               |   |
|              | C6          | 112                          | 336   | 224                | 112                | 112                           | 112   |
| Cyclone V ST | D5          | 87                           | 261   | 174                | 87                 | 87                            | 87  |
|              | D6          | 112                          | 336   | 224                | 112                | 112                           | 112   |

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

## Types of Embedded Memory

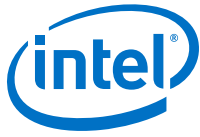
The Cyclone V devices contain two types of memory blocks:

- 10 Kb M10K blocks—blocks of dedicated memory resources. The M10K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Cyclone V devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Cyclone V Devices

**Table 18. Embedded Memory Capacity and Distribution in Cyclone V Devices**

| Variant      | Member Code | M10K  |              | MLAB  |              | Total RAM Bit (Kb) |
|--------------|-------------|-------|--------------|-------|--------------|--------------------|
|              |             | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) |                    |
| Cyclone V E  | A2          | 176   | 1,760        | 314   | 196          | 1,956              |
|              | A4          | 308   | 3,080        | 485   | 303          | 3,383              |
|              | A5          | 446   | 4,460        | 679   | 424          | 4,884              |
|              | A7          | 686   | 6,860        | 1338  | 836          | 7,696              |
|              | A9          | 1,220 | 12,200       | 2748  | 1,717        | 13,917             |
| Cyclone V GX | C3          | 135   | 1,350        | 291   | 182          | 1,532              |
|              | C4          | 250   | 2,500        | 678   | 424          | 2,924              |
|              | C5          | 446   | 4,460        | 678   | 424          | 4,884              |
|              | C7          | 686   | 6,860        | 1338  | 836          | 7,696              |
|              | C9          | 1,220 | 12,200       | 2748  | 1,717        | 13,917             |
| continued... |             |       |              |       |              |                    |



| Variant      | Member Code | M10K  |              | MLAB  |              | Total RAM Bit (Kb) |
|--------------|-------------|-------|--------------|-------|--------------|--------------------|
|              |             | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) |                    |
| Cyclone V GT | D5          | 446   | 4,460        | 679   | 424          | 4,884              |
|              | D7          | 686   | 6,860        | 1338  | 836          | 7,696              |
|              | D9          | 1,220 | 12,200       | 2748  | 1,717        | 13,917             |
| Cyclone V SE | A2          | 140   | 1,400        | 221   | 138          | 1,538              |
|              | A4          | 270   | 2,700        | 370   | 231          | 2,460              |
|              | A5          | 397   | 3,970        | 768   | 480          | 4,450              |
|              | A6          | 553   | 5,530        | 994   | 621          | 6,151              |
| Cyclone V SX | C2          | 140   | 1,400        | 221   | 138          | 1,538              |
|              | C4          | 270   | 2,700        | 370   | 231          | 2,460              |
|              | C5          | 397   | 3,970        | 768   | 480          | 4,450              |
|              | C6          | 553   | 5,530        | 994   | 621          | 6,151              |
| Cyclone V ST | D5          | 397   | 3,970        | 768   | 480          | 4,450              |
|              | D6          | 553   | 5,530        | 994   | 621          | 6,151              |

## Embedded Memory Configurations

**Table 19. Supported Embedded Memory Block Configurations for Cyclone V Devices**

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

| Memory Block | Depth (bits) | Programmable Width |
|--------------|--------------|--------------------|
| MLAB         | 32           | x16, x18, or x20   |
| M10K         | 256          | x40 or x32         |
|              | 512          | x20 or x16         |
|              | 1K           | x10 or x8          |
|              | 2K           | x5 or x4           |
|              | 4K           | x2                 |
|              | 8K           | x1                 |

## Clock Networks and PLL Clock Sources

550 MHz Cyclone V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Intel's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

**Note:** To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.



## PLL Features

The PLLs in the Cyclone V devices support the following features:

- Frequency synthesis
- On-chip clock deskew
- Jitter attenuation
- Programmable output clock duty cycles
- PLL cascading
- Reference clock switchover
- Programmable bandwidth
- User-mode reconfiguration of PLLs
- Low power mode for each fractional PLL
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation modes

## Fractional PLL

In addition to integer PLLs, the Cyclone V devices use a fractional PLL architecture. The devices have up to eight PLLs, each with nine output counters. You can use the output counters to reduce PLL usage in two ways:

- Reduce the number of oscillators that are required on your board by using fractional PLLs
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

If you use the fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for off-chip reference clock sources in your design.

The transceiver fractional PLLs that are not used by the transceiver I/Os can be used as general purpose fractional PLLs by the FPGA fabric.

## FPGA General Purpose I/O

Cyclone V devices offer highly configurable GPIOs. The following list describes the features of the GPIOs:

- Programmable bus hold and weak pull-up
- LVDS output buffer with programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis
- On-chip parallel termination ( $R_T$  OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture





| PCS Support                     | Data Rates (Gbps) | Transmitter Data Path Feature   | Receiver Data Path Feature  |
|---------------------------------|-------------------|---|---|
| Serial ATA Gen1 and Gen2        | 1.5 and 3.0       | <ul style="list-style-type: none"><li>Custom PHY IP core with preset feature</li><li>Electrical idle</li></ul>                            | <ul style="list-style-type: none"><li>Custom PHY IP core with preset feature</li><li>Signal detect</li><li>Wider spread of asynchronous SSC</li></ul> |
| CPRI 4.1 <sup>(16)</sup>        | 0.6144 to 6.144   | <ul style="list-style-type: none"><li>Dedicated deterministic latency PHY IP core</li><li>Transmitter (TX) manual bit-slip mode</li></ul> | <ul style="list-style-type: none"><li>Dedicated deterministic latency PHY IP core</li><li>Receiver (RX) deterministic latency state machine</li></ul> |
| OBSAI RP3                       | 0.768 to 3.072    |   |   |
| V-by-One HS                     | Up to 3.75        | Custom PHY IP core  | <ul style="list-style-type: none"><li>Custom PHY IP core</li><li>Wider spread of asynchronous SSC</li></ul>   |
| DisplayPort 1.2 <sup>(17)</sup> | 1.62 and 2.7      |   |   |

## SoC with HPS

Each SoC combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

## HPS Features

The HPS consists of a dual-core Arm Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in the following figure.

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<sup>(16)</sup> High-voltage output mode (1000-BASE-CX) is not supported.

<sup>(17)</sup> Pending characterization.

**Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor**



## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.



## Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

## Document Revision History for Cyclone V Device Overview

| Document Version | Changes   |
|------------------|---|
| 2018.05.07       | <ul style="list-style-type: none"> <li>• Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the <i>Sample Ordering Code and Available Options</i> diagrams.</li> <li>• Rebranded as Intel.</li> </ul> |

| Date          | Version    | Changes  |
|---------------|------------|--|
| December 2017 | 2017.12.18 | <ul style="list-style-type: none"> <li>• Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices.</li> </ul>   |
| June 2016     | 2016.06.10 | Updated Cyclone V GT speed grade to -7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram.   |
| December 2015 | 2015.12.21 | <ul style="list-style-type: none"> <li>• Added descriptions to package plan tables for Cyclone V GT and ST devices.</li> <li>• Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li> </ul>  |
| June 2015     | 2015.06.12 | <ul style="list-style-type: none"> <li>• Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives.</li> <li>• Updated logic elements (LE) (K) for the following devices: <ul style="list-style-type: none"> <li>— Cyclone V E A7: Updated from 149.5 to 150</li> <li>— Cyclone V GX C3: Updated from 35.5 to 36</li> <li>— Cyclone V GX C7: Updated from 149.7 to 150</li> <li>— Cyclone V GT D7: Updated from 149.5 to 150</li> </ul> </li> <li>• Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows: <ul style="list-style-type: none"> <li>— Cyclone V GX C3: Updated from 291 to 182</li> <li>— Cyclone V GX C4: Updated from 678 to 424</li> <li>— Cyclone V GX C5: Updated from 678 to 424</li> <li>— Cyclone V GX C7: Updated from 1,338 to 836</li> <li>— Cyclone V GX C9: Updated from 2,748 to 1,717</li> </ul> </li> </ul> |

*continued...*



| Date         | Version    | Changes  |
|--------------|------------|--|
|              |            | <ul style="list-style-type: none"><li>Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<ul style="list-style-type: none"><li>Cyclone V GX C3: Updated from 181 to 182</li><li>Cyclone V GX C4: Updated from 295 to 424</li></ul></li><li>Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<ul style="list-style-type: none"><li>Cyclone V GX C3: Updated from 1,531 to 1,532</li><li>Cyclone V GX C4: Updated from 2,795 to 2,924</li></ul></li><li>Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows:<ul style="list-style-type: none"><li>Cyclone V GX C4: Updated from 472 to 678</li><li>Cyclone V GX C5: Updated from 679 to 678</li></ul></li></ul>   |
| March 2015   | 2015.03.31 | <ul style="list-style-type: none"><li>Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table.</li><li>Added optional suffix "SC: Internal scrubbing support" to the following diagrams:<ul style="list-style-type: none"><li>Sample Ordering Code and Available Options for Cyclone V E Devices</li><li>Sample Ordering Code and Available Options for Cyclone V GX Devices</li><li>Sample Ordering Code and Available Options for Cyclone V SE Devices</li><li>Sample Ordering Code and Available Options for Cyclone V SX Devices</li></ul></li></ul>   |
| January 2015 | 2015.01.23 | <ul style="list-style-type: none"><li>Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and -7 speed grade.<ul style="list-style-type: none"><li>Operating Temperature: Removed C and A temperature grades</li><li>FPGA Fabric Speed Grade: Removed -6 and -8 speed grades</li></ul></li><li>Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps:<ul style="list-style-type: none"><li>Device Variants for the Cyclone V Device Family table</li><li>Sample Ordering Code and Available Options for Cyclone V ST Devices figure</li><li>Maximum Resource Counts for Cyclone V ST Devices</li></ul></li><li>Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices.<ul style="list-style-type: none"><li>Logic elements (LE) (K): Updated from 35.7 to 35.5</li><li>Variable-precision DSP block: Updated from 51 to 57</li><li>18 x 18 multiplier: Updated from 102 to 114</li></ul></li><li>Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices.<ul style="list-style-type: none"><li>Variableprecision DSP Block: Updated from 51 to 57</li><li>9 x 9 Multiplier: Updated from 153 to 171</li><li>18 x 18 Multiplier: Updated from 102 to 114</li><li>27 x 27 Multiplier: Updated from 51 to 57</li><li>18 x 18 Multiplier Adder Mode: Updated from 51 to 57</li><li>18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57</li></ul></li><li>Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices.<ul style="list-style-type: none"><li>M10K block: Updated from 119 to 135</li><li>M10K RAM bit (Kb): Updated from 1,190 to 1,350</li><li>MLAB block: Updated from 255 to 291</li><li>MLAB RAM bit (Kb): Updated from 159 to 181</li><li>Total RAM bit (Kb): Updated from 1,349 to 1,531</li></ul></li></ul> |
| October 2014 | 2014.10.06 | Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices.  |
| continued... |            |  |



| Date          | Version | Changes  |
|---------------|---------|--|
|               |         | <ul style="list-style-type: none"> <li>Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10.</li> <li>Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections.</li> <li>Text edits throughout the document.</li> </ul>  |
| February 2012 | 1.2     | <ul style="list-style-type: none"> <li>Updated Table 1-2, Table 1-3, and Table 1-6.</li> <li>Updated "Cyclone V Family Plan" on page 1-4 and "Clock Networks and PLL Clock Sources" on page 1-15.</li> <li>Updated Figure 1-1 and Figure 1-6.</li> </ul>   |
| November 2011 | 1.1     | <ul style="list-style-type: none"> <li>Updated Table 1-1, Table 1-2, Table 1-3, Table 1-4, Table 1-5, and Table 1-6.</li> <li>Updated Figure 1-4, Figure 1-5, Figure 1-6, Figure 1-7, and Figure 1-8.</li> <li>Updated "System Peripherals" on page 1-18, "HPS-FPGA AXI Bridges" on page 1-19, "HPS SDRAM Controller Subsystem" on page 1-19, "FPGA Configuration and Processor Booting" on page 1-19, and "Hardware and Software Development" on page 1-20.</li> <li>Minor text edits.</li> </ul> |
| October 2011  | 1.0     | Initial release.   |