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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	11900
Number of Logic Elements/Cells	31500
Total RAM Bits	1381376
Number of I/O	208
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5cgxfc3b6f23c6n">https://www.e-xfl.com/product-detail/intel/5cgxfc3b6f23c6n</a>



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## Cyclone V Device Overview

The Cyclone® V devices are designed to simultaneously accommodate the shrinking power consumption, cost, and time-to-market requirements; and the increasing bandwidth requirements for high-volume and cost-sensitive applications.

Enhanced with integrated transceivers and hard memory controllers, the Cyclone V devices are suitable for applications in the industrial, wireless and wireline, military, and automotive markets.

### Related Information

[Cyclone V Device Handbook: Known Issues](#)

Lists the planned updates to the Cyclone V Device Handbook chapters.

## Key Advantages of Cyclone V Devices

**Table 1. Key Advantages of the Cyclone V Device Family**

Advantage	Supporting Feature
Lower power consumption	<ul style="list-style-type: none"> <li>Built on TSMC's 28 nm low-power (28LP) process technology and includes an abundance of hard intellectual property (IP) blocks</li> <li>Up to 40% lower power consumption than the previous generation device</li> </ul>
Improved logic integration and differentiation capabilities	<ul style="list-style-type: none"> <li>8-input adaptive logic module (ALM)</li> <li>Up to 13.59 megabits (Mb) of embedded memory</li> <li>Variable-precision digital signal processing (DSP) blocks</li> </ul>
Increased bandwidth capacity	<ul style="list-style-type: none"> <li>3.125 gigabits per second (Gbps) and 6.144 Gbps transceivers</li> <li>Hard memory controllers</li> </ul>
Hard processor system (HPS) with integrated Arm* Cortex*-A9 MPCore* processor	<ul style="list-style-type: none"> <li>Tight integration of a dual-core Arm Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Cyclone V system-on-a-chip (SoC)</li> <li>Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric</li> </ul>
Lowest system cost	<ul style="list-style-type: none"> <li>Requires only two core voltages to operate</li> <li>Available in low-cost wirebond packaging</li> <li>Includes innovative features such as Configuration via Protocol (CvP) and partial reconfiguration</li> </ul>

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\*Other names and brands may be claimed as the property of others.

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## Summary of Cyclone V Features

**Table 2. Summary of Features for Cyclone V Devices**

Feature	Description	
Technology	<ul style="list-style-type: none"> <li>TSMC's 28-nm low-power (28LP) process technology</li> <li>1.1 V core voltage</li> </ul>	
Packaging	<ul style="list-style-type: none"> <li>Wirebond low-halogen packages</li> <li>Multiple device densities with compatible package footprints for seamless migration between different device densities</li> <li>RoHS-compliant and leaded<sup>(1)</sup> options</li> </ul>	
High-performance FPGA fabric	Enhanced 8-input ALM with four registers	
Internal memory blocks	<ul style="list-style-type: none"> <li>M10K—10-kilobits (Kb) memory blocks with soft error correction code (ECC)</li> <li>Memory logic array block (MLAB)—640-bit distributed LUTRAM where you can use up to 25% of the ALMs as MLAB memory</li> </ul>	
Embedded Hard IP blocks	Variable-precision DSP	<ul style="list-style-type: none"> <li>Native support for up to three signal processing precision levels (three 9 x 9, two 18 x 18, or one 27 x 27 multiplier) in the same variable-precision DSP block</li> <li>64-bit accumulator and cascade</li> <li>Embedded internal coefficient memory</li> <li>Padder/subtractor for improved efficiency</li> </ul>
	Memory controller	DDR3, DDR2, and LPDDR2 with 16 and 32 bit ECC support
	Embedded transceiver I/O	PCI Express* (PCIe*) Gen2 and Gen1 (x1, x2, or x4) hard IP with multifunction support, endpoint, and root port
Clock networks	<ul style="list-style-type: none"> <li>Up to 550 MHz global clock network</li> <li>Global, quadrant, and peripheral clock networks</li> <li>Clock networks that are not used can be powered down to reduce dynamic power</li> </ul>	
Phase-locked loops (PLLs)	<ul style="list-style-type: none"> <li>Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)</li> <li>Integer mode and fractional mode</li> </ul>	
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"> <li>875 megabits per second (Mbps) LVDS receiver and 840 Mbps LVDS transmitter</li> <li>400 MHz/800 Mbps external memory interface</li> <li>On-chip termination (OCT)</li> <li>3.3 V support with up to 16 mA drive strength</li> </ul>	
Low-power high-speed serial interface	<ul style="list-style-type: none"> <li>614 Mbps to 6.144 Gbps integrated transceiver speed</li> <li>Transmit pre-emphasis and receiver equalization</li> <li>Dynamic partial reconfiguration of individual channels</li> </ul>	
HPS (Cyclone V SE, SX, and ST devices only)	<ul style="list-style-type: none"> <li>Single or dual-core Arm Cortex-A9 MPCore processor-up to 925 MHz maximum frequency with support for symmetric and asymmetric multiprocessing</li> <li>Interface peripherals—10/100/1000 Ethernet media access control (EMAC), USB 2.0 On-The-Go (OTG) controller, quad serial peripheral interface (QSPI) flash controller, NAND flash controller, Secure Digital/MultiMediaCard (SD/MMC) controller, UART, controller area network (CAN), serial peripheral interface (SPI), I<sup>2</sup>C interface, and up to 85 HPS GPIO interfaces</li> <li>System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li> <li>On-chip RAM and boot ROM</li> </ul>	

*continued...*

<sup>(1)</sup> Contact Intel for availability.



### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

### Package Plan

**Table 5. Package Plan for Cyclone V E Devices**

Member Code	M383 (13 mm)	M484 (15 mm)	U324 (15 mm)	F256 (17 mm)	U484 (19 mm)	F484 (23 mm)	F672 (27 mm)	F896 (31 mm)
	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
A2	223	—	176	128	224	224	—	—
A4	223	—	176	128	224	224	—	—
A5	175	—	—	—	224	240	—	—
A7	—	240	—	—	240	240	336	480
A9	—	—	—	—	240	224	336	480

### Cyclone V GX

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

[Product Selector Guide](#)

Provides the latest information about Intel products.



Resource		Member Code				
		C3	C4	C5	C7	C9
LVDS	Transmitter	52	84	84	120	140
	Receiver	52	84	84	120	140
PCIe Hard IP Block		1	2	2	2	2
Hard Memory Controller		1	2	2	2	2

### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 7. Package Plan for Cyclone V GX Devices**

Member Code	M301 (11 mm)		M383 (13 mm)		M484 (15 mm)		U324 (15 mm)		U484 (19 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	—	—	—	—	—	—	144	3	208	3
C4	129	4	175	6	—	—	—	—	224	6
C5	129	4	175	6	—	—	—	—	224	6
C7	—	—	—	—	240	3	—	—	240	6
C9	—	—	—	—	—	—	—	—	240	5

Member Code	F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
C3	208	3	—	—	—	—	—	—
C4	240	6	336	6	—	—	—	—
C5	240	6	336	6	—	—	—	—
C7	240	6	336	9	480	9	—	—
C9	224	6	336	9	480	12	560	12

## Cyclone V GT

This section provides the available options, maximum resource counts, and package plan for the Cyclone V GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

### Related Information

[Product Selector Guide](#)

Provides the latest information about Intel products.



Resource		Member Code			
		C2	C4	C5	C6
HPS PLL		3	3	3	3
3 Gbps Transceiver		6	6	9	9
FPGA GPIO <sup>(8)</sup>		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
PCIe Hard IP Block		2	2	2 <sup>(9)</sup>	2 <sup>(9)</sup>
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core	Dual-core	Dual-core

### Related Information

#### True LVDS Buffers in Devices, I/O Features in Cyclone V Devices

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 13. Package Plan for Cyclone V SX Devices**

The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.

Member Code	U672 (23 mm)			F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR	FPGA GPIO	HPS I/O	XCVR
C2	145	181	6	—	—	—
C4	145	181	6	—	—	—
C5	145	181	6	288	181	9
C6	145	181	6	288	181	9

## Cyclone V ST

This section provides the available options, maximum resource counts, and package plan for the Cyclone V ST devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the *Product Selector Guide*.

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(9)</sup> 1 PCIe Hard IP Block in U672 package.



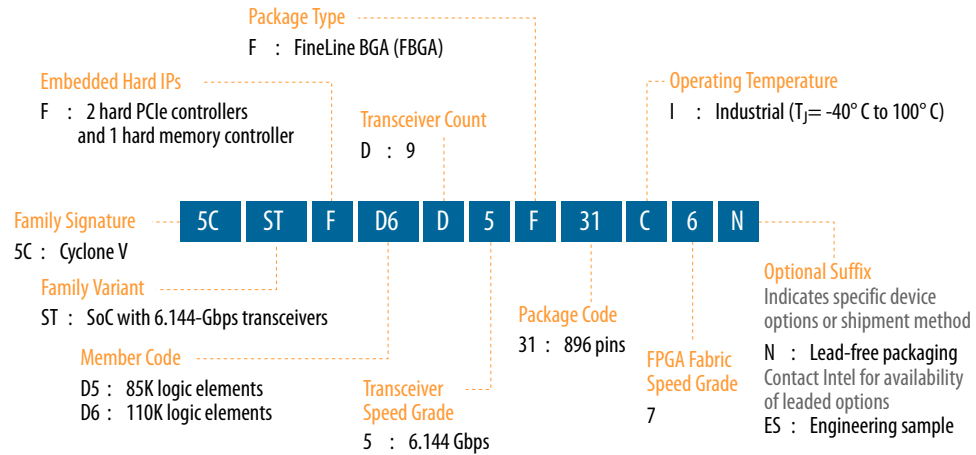
## Related Information

### Product Selector Guide

Provides the latest information about Intel products.

## Available Options

**Figure 6. Sample Ordering Code and Available Options for Cyclone V ST Devices**



## Maximum Resources

**Table 14. Maximum Resource Counts for Cyclone V ST Devices**

Resource		Member Code	
		D5	D6
Logic Elements (LE) (K)		85	110
ALM		32,070	41,910
Register		128,300	166,036
Memory (Kb)	M10K	3,970	5,570
	MLAB	480	621
Variable-precision DSP Block		87	112
18 x 18 Multiplier		174	224
FPGA PLL		6	6
HPS PLL		3	3
6.144 Gbps Transceiver		9	9
FPGA GPIO <sup>(10)</sup>		288	288
HPS I/O		181	181
LVDS	Transmitter	72	72
continued...			

<sup>(10)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.





Resource		Member Code	
		D5	D6
	Receiver	72	72
PCIe Hard IP Block		2	2
FPGA Hard Memory Controller		1	1
HPS Hard Memory Controller		1	1
Arm Cortex-A9 MPCore Processor		Dual-core	Dual-core

### Related Information

[True LVDS Buffers in Devices, I/O Features in Cyclone V Devices](#)

Provides the number of LVDS channels in each device package.

## Package Plan

**Table 15. Package Plan for Cyclone V ST Devices**

- The HPS I/O counts are the number of I/Os in the HPS and does not correlate with the number of HPS-specific I/O pins in the FPGA. Each HPS-specific pin in the FPGA may be mapped to several HPS I/Os.
- Transceiver counts shown are for transceiver  $\leq 5$  Gbps. 6 Gbps transceiver channel count support depends on the package and channel usage. For more information about the 6 Gbps transceiver channel count, refer to the *Cyclone V Device Handbook Volume 2: Transceivers*.

Member Code	F896 (31 mm)		
	FPGA GPIO	HPS I/O	XCVR
D5	288	181	9 <sup>(11)</sup>
D6	288	181	9 <sup>(11)</sup>

### Related Information

[6.144-Gbps Support Capability in Cyclone V GT Devices, Cyclone V Device Handbook Volume 2: Transceivers](#)

Provides more information about 6 Gbps transceiver channel count.

<sup>(11)</sup> If you require CPRI (at 4.9152 Gbps) and PCIe Gen2 transmit jitter compliance, Intel recommends that you use only up to seven full-duplex transceiver channels for CPRI, and up to six full-duplex channels for PCIe Gen2. The CMU channels are not considered full-duplex channels.

**Figure 8. ALM for Cyclone V Devices**



You can configure up to 25% of the ALMs in the Cyclone V devices as distributed memory using MLABs.

#### Related Information

[Embedded Memory Capacity in Cyclone V Devices](#) on page 21  
Lists the embedded memory capacity for each device.

## Variable-Precision DSP Block

Cyclone V devices feature a variable-precision DSP block that supports these features:

- Configurable to support signal processing precisions ranging from 9 x 9, 18 x 18 and 27 x 27 bits natively
- A 64-bit accumulator
- A hard preadder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic finite impulse response (FIR) filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18- or 27-bit mode
- Fully independent multiplier operation
- A second accumulator feedback register to accommodate complex multiply-accumulate functions
- Fully independent Efficient support for single-precision floating point arithmetic
- The inferability of all modes by the Intel Quartus Prime design software

**Table 16. Variable-Precision DSP Block Configurations for Cyclone V Devices**

Usage Example	Multiplier Size (Bit)	DSP Block Resource
Low precision fixed point for video applications	Three 9 x 9	1
Medium precision fixed point in FIR filters	Two 18 x 18	1
FIR filters and general DSP usage	Two 18 x 18 with accumulate	1
High precision fixed- or floating-point implementations	One 27 x 27 with accumulate	1

You can configure each DSP block during compilation as independent three 9 x 9, two 18 x 18, or one 27 x 27 multipliers. With a dedicated 64 bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

**Table 17. Number of Multipliers in Cyclone V Devices**

The table lists the variable-precision DSP resources by bit precision for each Cyclone V device.

Variant	Member Code	Variable-precision DSP Block	Independent Input and Output Multiplications Operator			18 x 18 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			9 x 9 Multiplier	18 x 18 Multiplier	27 x 27 Multiplier		
Cyclone V E	A2	25	75	50	25	25	25
	A4	66	198	132	66	66	66
	A5	150	450	300	150	150	150
	A7	156	468	312	156	156	156
	A9	342	1,026	684	342	342	342
Cyclone V GX	C3	57	171	114	57	57	57
	C4	70	210	140	70	70	70
	C5	150	450	300	150	150	150
	C7	156	468	312	156	156	156
	C9	342	1,026	684	342	342	342
Cyclone V GT	D5	150	450	300	150	150	150
	D7	156	468	312	156	156	156
	D9	342	1,026	684	342	342	342
Cyclone V SE	A2	36	108	72	36	36	36
	A4	84	252	168	84	84	84
	A5	87	261	174	87	87	87
	A6	112	336	224	112	112	112
Cyclone V SX	C2	36	108	72	36	36	36
	C4	84	252	168	84	84	84
	C5	87	261	174	87	87	87
continued...							



Variant	Member Code	M10K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Cyclone V GT	D5	446	4,460	679	424	4,884
	D7	686	6,860	1338	836	7,696
	D9	1,220	12,200	2748	1,717	13,917
Cyclone V SE	A2	140	1,400	221	138	1,538
	A4	270	2,700	370	231	2,460
	A5	397	3,970	768	480	4,450
	A6	553	5,530	994	621	6,151
Cyclone V SX	C2	140	1,400	221	138	1,538
	C4	270	2,700	370	231	2,460
	C5	397	3,970	768	480	4,450
	C6	553	5,530	994	621	6,151
Cyclone V ST	D5	397	3,970	768	480	4,450
	D6	553	5,530	994	621	6,151

## Embedded Memory Configurations

**Table 19. Supported Embedded Memory Block Configurations for Cyclone V Devices**

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

## Clock Networks and PLL Clock Sources

550 MHz Cyclone V devices have 16 global clock networks capable of up to operation. The clock network architecture is based on Intel's global, quadrant, and peripheral clock structure. This clock structure is supported by dedicated clock input pins and fractional PLLs.

**Note:** To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

## PCIe Gen1 and Gen2 Hard IP

Cyclone V GX, GT, SX, and ST devices contain PCIe hard IP that is designed for performance and ease-of-use. The PCIe hard IP consists of the MAC, data link, and transaction layers.

The PCIe hard IP supports PCIe Gen2 and Gen1 end point and root port for up to x4 lane configuration. The PCIe Gen2 x4 support is PCIe-compatible.

The PCIe endpoint support includes multifunction support for up to eight functions, as shown in the following figure. The integrated multifunction support reduces the FPGA logic requirements by up to 20,000 LEs for PCIe designs that require multiple peripherals.

**Figure 9. PCIe Multifunction for Cyclone V Devices**



The Cyclone V PCIe hard IP operates independently from the core logic. This independent operation allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device.

In addition, the PCIe hard IP in the Cyclone V device provides improved end-to-end datapath protection using ECC.

## External Memory Interface

This section provides an overview of the external memory interface in Cyclone V devices.

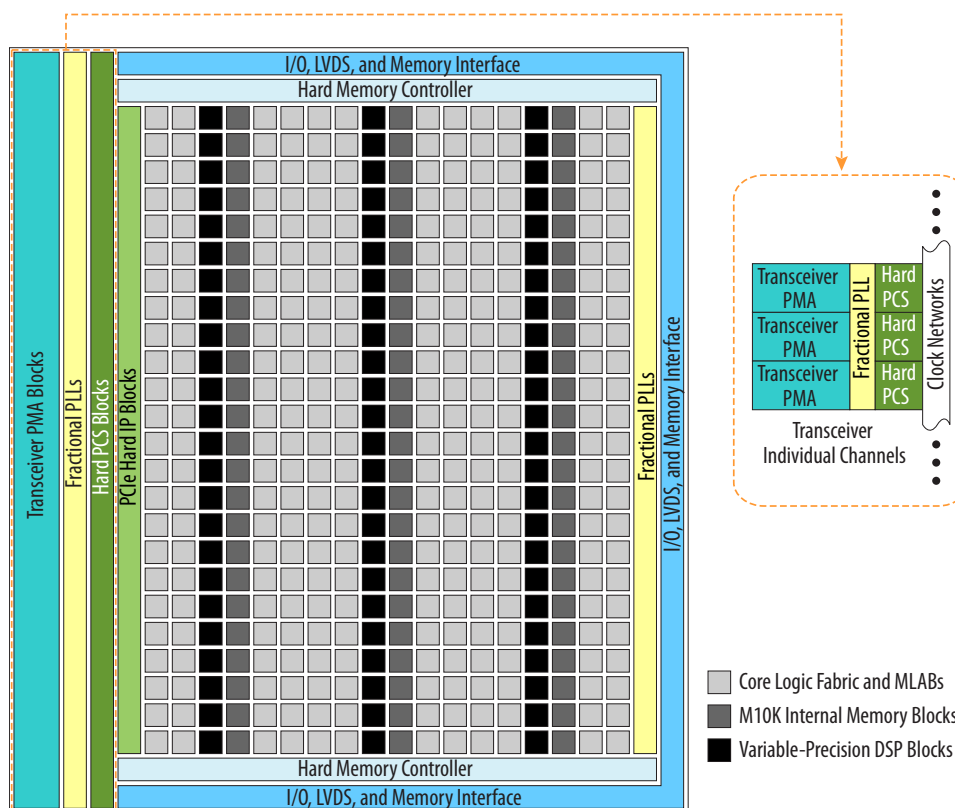
### Hard and Soft Memory Controllers

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices. Each controller supports 8 to 32 bit components of up to 4 gigabits (Gb) in density with two chip selects and optional ECC. For the Cyclone V SoC devices, an additional hard memory controller in the HPS supports DDR3, DDR2, and LPDDR2 SDRAM devices.

All Cyclone V devices support soft memory controllers for DDR3, DDR2, and LPDDR2 SDRAM devices for maximum flexibility.

**Figure 10. Device Chip Overview for Cyclone V GX and GT Devices**

The figure shows a Cyclone V FPGA with transceivers. Different Cyclone V devices may have a different floorplans than the one shown here.



## PMA Features

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip—ensuring optimal signal integrity. For the transceivers, you can use the channel PLL of an unused receiver PMA as an additional transmit PLL.

**Table 22. PMA Features of the Transceivers in Cyclone V Devices**

Features	Capability
Backplane support	Driving capability up to 6.144 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment pattern
Equalization and pre-emphasis	<ul style="list-style-type: none"> <li>Up to 14.37 dB of pre-emphasis and up to 4.7 dB of equalization</li> <li>No decision feedback equalizer (DFE)</li> </ul>
Ring oscillator transmit PLLs	614 Mbps to 6.144 Gbps
Input reference clock range	20 MHz to 400 MHz
Transceiver dynamic reconfiguration	Allows the reconfiguration of a single channel without affecting the operation of other channels

**Figure 11. HPS with Dual-Core Arm Cortex-A9 MPCore Processor**



## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals to interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports Arm CoreSight debug and core traces to facilitate software development.



**Note:** Although the FPGA fabric and HPS are on separate power domains, the HPS must remain powered up during operation while the FPGA fabric can be powered up or down as required.

#### **Related Information**

##### [Cyclone V Device Family Pin Connection Guidelines](#)

Provides detailed information about power supply pin connection guidelines and power regulator sharing.

## **Hardware and Software Development**

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer (Standard) system integration tool in the Intel Quartus Prime software.

For software development, the Arm-based SoC devices inherit the rich software development ecosystem available for the Arm Cortex-A9 MPCore processor. The software development process for Intel SoCs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems is available for the SoCs. For more information on the operating systems support availability, contact the Intel sales team.

You can begin device-specific firmware and software development on the Intel SoC Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

#### **Related Information**

##### [International Altera Sales Support Offices](#)

## **Dynamic and Partial Reconfiguration**

The Cyclone V devices support dynamic reconfiguration and partial reconfiguration.

### **Dynamic Reconfiguration**

The dynamic reconfiguration feature allows you to dynamically change the transceiver data rates, PMA settings, or protocols of a channel, without affecting data transfer on adjacent channels. This feature is ideal for applications that require on-the-fly multiprotocol or multirate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

### **Partial Reconfiguration**

**Note:** The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

Partial reconfiguration allows you to reconfigure part of the device while other sections of the device remain operational. This capability is important in systems with critical uptime requirements because it allows you to make updates or adjust functionality without disrupting services.



Apart from lowering cost and power consumption, partial reconfiguration increases the effective logic density of the device because placing device functions that do not operate simultaneously is not necessary. Instead, you can store these functions in external memory and load them whenever the functions are required. This capability reduces the size of the device because it allows multiple applications on a single device—saving the board space and reducing the power consumption.

Intel simplifies the time-intensive task of partial reconfiguration by building this capability on top of the proven incremental compile and design flow in the Intel Quartus Prime design software. With the Intel solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable simultaneous partial reconfiguration of both the device core and transceivers.

## Enhanced Configuration and Configuration via Protocol

Cyclone V devices support 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.

**Table 24. Configuration Schemes and Features Supported by Cyclone V Devices**

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)	Decompression	Design Security	Partial Reconfiguration <sup>(18)</sup>	Remote System Update
AS through the EPCS and EPCQ serial configuration device	1 bit, 4 bits	100	—	Yes	Yes	—	Yes
PS through CPLD or external microcontroller	1 bit	125	125	Yes	Yes	—	—
FPP	8 bits	125	—	Yes	Yes	—	Parallel flash loader
	16 bits	125	—	Yes	Yes	Yes	
CvP (PCIe)	x1, x2, and x4 lanes	—	—	Yes	Yes	Yes	—
JTAG	1 bit	33	33	—	—	—	—

Instead of using an external flash or ROM, you can configure the Cyclone V devices through PCIe using CvP. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Cyclone V CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

### Related Information

[Configuration via Protocol \(CvP\) Implementation in Intel FPGAs User Guide](#)

Provides more information about CvP.

<sup>(18)</sup> The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.



## Power Management

Leveraging the FPGA architectural features, process technology advancements, and transceivers that are designed for power efficiency, the Cyclone V devices consume less power than previous generation Cyclone FPGAs:

- Total device core power consumption—less by up to 40%.
- Transceiver channel power consumption—less by up to 50%.

Additionally, Cyclone V devices contain several hard IP blocks that reduce logic resources and deliver substantial power savings of up to 25% less power than equivalent soft implementations.

## Document Revision History for Cyclone V Device Overview

Document Version	Changes
2018.05.07	<ul style="list-style-type: none"> <li>• Added the low power option ("L" suffix) for Cyclone V SE and Cyclone V SX devices in the <i>Sample Ordering Code and Available Options</i> diagrams.</li> <li>• Rebranded as Intel.</li> </ul>

Date	Version	Changes
December 2017	2017.12.18	<ul style="list-style-type: none"> <li>• Updated ALM resources for Cyclone V E, Cyclone V SE, Cyclone V SX, and Cyclone V ST devices.</li> </ul>
June 2016	2016.06.10	Updated Cyclone V GT speed grade to -7 in Sample Ordering Code and Available Options for Cyclone V GT Devices diagram.
December 2015	2015.12.21	<ul style="list-style-type: none"> <li>• Added descriptions to package plan tables for Cyclone V GT and ST devices.</li> <li>• Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li> </ul>
June 2015	2015.06.12	<ul style="list-style-type: none"> <li>• Replaced a note to partial reconfiguration feature. Note: The partial reconfiguration feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives.</li> <li>• Updated logic elements (LE) (K) for the following devices: <ul style="list-style-type: none"> <li>— Cyclone V E A7: Updated from 149.5 to 150</li> <li>— Cyclone V GX C3: Updated from 35.5 to 36</li> <li>— Cyclone V GX C7: Updated from 149.7 to 150</li> <li>— Cyclone V GT D7: Updated from 149.5 to 150</li> </ul> </li> <li>• Updated MLAB (Kb) in Maximum Resource Counts for Cyclone V GX Devices table as follows: <ul style="list-style-type: none"> <li>— Cyclone V GX C3: Updated from 291 to 182</li> <li>— Cyclone V GX C4: Updated from 678 to 424</li> <li>— Cyclone V GX C5: Updated from 678 to 424</li> <li>— Cyclone V GX C7: Updated from 1,338 to 836</li> <li>— Cyclone V GX C9: Updated from 2,748 to 1,717</li> </ul> </li> </ul>

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Date	Version	Changes
		<ul style="list-style-type: none"> <li>Updated MLAB RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: <ul style="list-style-type: none"> <li>Cyclone V GX C3: Updated from 181 to 182</li> <li>Cyclone V GX C4: Updated from 295 to 424</li> </ul> </li> <li>Updated Total RAM Bit (Kb) in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: <ul style="list-style-type: none"> <li>Cyclone V GX C3: Updated from 1,531 to 1,532</li> <li>Cyclone V GX C4: Updated from 2,795 to 2,924</li> </ul> </li> <li>Updated MLAB Block count in Embedded Memory Capacity and Distribution in Cyclone V Devices table as follows: <ul style="list-style-type: none"> <li>Cyclone V GX C4: Updated from 472 to 678</li> <li>Cyclone V GX C5: Updated from 679 to 678</li> </ul> </li> </ul>
March 2015	2015.03.31	<ul style="list-style-type: none"> <li>Added internal scrubbing feature under configuration in Summary of Features for Cyclone V Devices table.</li> <li>Added optional suffix "SC: Internal scrubbing support" to the following diagrams: <ul style="list-style-type: none"> <li>Sample Ordering Code and Available Options for Cyclone V E Devices</li> <li>Sample Ordering Code and Available Options for Cyclone V GX Devices</li> <li>Sample Ordering Code and Available Options for Cyclone V SE Devices</li> <li>Sample Ordering Code and Available Options for Cyclone V SX Devices</li> </ul> </li> </ul>
January 2015	2015.01.23	<ul style="list-style-type: none"> <li>Updated Sample Ordering Code and Available Options for Cyclone V ST Devices figure because Cyclone V ST devices are only available in I temperature grade and -7 speed grade. <ul style="list-style-type: none"> <li>Operating Temperature: Removed C and A temperature grades</li> <li>FPGA Fabric Speed Grade: Removed -6 and -8 speed grades</li> </ul> </li> <li>Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps: <ul style="list-style-type: none"> <li>Device Variants for the Cyclone V Device Family table</li> <li>Sample Ordering Code and Available Options for Cyclone V ST Devices figure</li> <li>Maximum Resource Counts for Cyclone V ST Devices</li> </ul> </li> <li>Updated Maximum Resource Counts for Cyclone V GX Devices table for Cyclone V GX G3 devices. <ul style="list-style-type: none"> <li>Logic elements (LE) (K): Updated from 35.7 to 35.5</li> <li>Variable-precision DSP block: Updated from 51 to 57</li> <li>18 x 18 multiplier: Updated from 102 to 114</li> </ul> </li> <li>Updated Number of Multipliers in Cyclone V Devices table for Cyclone V GX G3 devices. <ul style="list-style-type: none"> <li>Variableprecision DSP Block: Updated from 51 to 57</li> <li>9 x 9 Multiplier: Updated from 153 to 171</li> <li>18 x 18 Multiplier: Updated from 102 to 114</li> <li>27 x 27 Multiplier: Updated from 51 to 57</li> <li>18 x 18 Multiplier Adder Mode: Updated from 51 to 57</li> <li>18 x 18 Multiplier Adder Summed with 36 bit Input: Updated from 51 to 57</li> </ul> </li> <li>Updated Embedded Memory Capacity and Distribution in Cyclone V Devices table for Cyclone V GX G3 devices. <ul style="list-style-type: none"> <li>M10K block: Updated from 119 to 135</li> <li>M10K RAM bit (Kb): Updated from 1,190 to 1,350</li> <li>MLAB block: Updated from 255 to 291</li> <li>MLAB RAM bit (Kb): Updated from 159 to 181</li> <li>Total RAM bit (Kb): Updated from 1,349 to 1,531</li> </ul> </li> </ul>
October 2014	2014.10.06	Added a footnote to the "Transceiver PCS Features for Cyclone V Devices" table to show that PCIe Gen2 is supported for Cyclone V GT and ST devices.
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Date	Version	Changes
		<ul style="list-style-type: none"><li>Updated HPS I/O for U484 (19 mm) in Table 11 with '151' for A2, A4, A5 and A6.</li><li>Updated Memory (Kb) for Maximum Resource Counts for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices.</li><li>Updated FPGA PLL for Maximum Resource Counts for Cyclone V SE A2, SX C2, devices.</li><li>Removed '36 x 36' from the Variable-Precision DSP Block.</li><li>Updated Variable-precision DSP Blocks and 18 x 18 Multiplier for Maximum Resource Counts for Cyclone V SX C4 device.</li><li>Updated the HPS I/O counts for Cyclone V SE, SX, and ST devices.</li><li>Updated Figure 7 which shows the I/O vertical migration table.</li><li>Updated Table 17 for Cyclone V SX C4 device.</li><li>Updated Embedded Memory Capacity and Distribution table for Cyclone V SE A4 and A6, SX C4 and C6, ST D6 devices.</li><li>Removed 'Counter reconfiguration' from the PLL Features.</li><li>Updated Low-Power Serial Transceivers by replacing 5 Gbps with 6.144 Gbps.</li><li>Removed 'Distributed Memory' symbol.</li><li>Updated the Capability in Table 22 of Backplane support to '6.144 Gbps'.</li><li>Updated Capability in Table 22 of Ring oscillator transmit PLLs with 6.144 Gbps.</li><li>Updated the PCS Support in Table 23 from 5 Gbps to '6 Gbps'.</li><li>Updated the Data Rates (Gbps) in Table 23 of 3 Gbps and 6 Gbps Basic to '6.144 Gbps'.</li><li>Updated the Data Rates (Gbps) in Table 23 of CPRI 4.1 to '6.144 Gbps'.</li><li>Clarified that partial reconfiguration is an advanced feature. Contact Altera for support of the feature.</li></ul>
December 2012	2012.12.28	<ul style="list-style-type: none"><li>Updated the pin counts for the MBGA packages.</li><li>Updated the GPIO and transceiver counts for the MBGA packages.</li><li>Updated the GPIO counts for the U484 package of the Cyclone V E A9, GX C9, and GT D9 devices.</li><li>Updated the vertical migration table for vertical migration of the U484 packages.</li><li>Updated the MLAB supported programmable widths at 32 bits depth.</li></ul>
November 2012	2012.11.19	<ul style="list-style-type: none"><li>Added new MBGA packages and additional U484 packages for Cyclone V E, GX, and GT.</li><li>Added ordering code for five-transceiver devices for Cyclone V GT and ST.</li><li>Updated the vertical migration table to add MBGA packages.</li><li>Added performance information for HPS memory controller.</li><li>Removed DDR3U support.</li><li>Updated Cyclone V ST speed grade information.</li><li>Added information on maximum transceiver channel usage restrictions for PCI Gen2 and CPRI at 4.9152 Gbps transmit jitter compliance.</li><li>Added note on the differences between GPIO reported in Overview with User I/O numbers shown in the Quartus II software.</li><li>Updated template.</li></ul>
July 2012	2.1	Added support for PCIe Gen2 x4 lane configuration (PCIe-compatible)
June 2012	2.0	<ul style="list-style-type: none"><li>Restructured the document.</li><li>Added the "Embedded Memory Capacity" and "Embedded Memory Configurations" sections.</li><li>Added Table 1, Table 3, Table 16, Table 19, and Table 20.</li><li>Updated Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 12, Table 13, Table 14, Table 17, and Table 18.</li></ul>
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Date	Version	Changes
		<ul style="list-style-type: none"> <li>Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, and Figure 10.</li> <li>Updated the "FPGA Configuration and Processor Booting" and "Hardware and Software Development" sections.</li> <li>Text edits throughout the document.</li> </ul>
February 2012	1.2	<ul style="list-style-type: none"> <li>Updated Table 1-2, Table 1-3, and Table 1-6.</li> <li>Updated "Cyclone V Family Plan" on page 1-4 and "Clock Networks and PLL Clock Sources" on page 1-15.</li> <li>Updated Figure 1-1 and Figure 1-6.</li> </ul>
November 2011	1.1	<ul style="list-style-type: none"> <li>Updated Table 1-1, Table 1-2, Table 1-3, Table 1-4, Table 1-5, and Table 1-6.</li> <li>Updated Figure 1-4, Figure 1-5, Figure 1-6, Figure 1-7, and Figure 1-8.</li> <li>Updated "System Peripherals" on page 1-18, "HPS-FPGA AXI Bridges" on page 1-19, "HPS SDRAM Controller Subsystem" on page 1-19, "FPGA Configuration and Processor Booting" on page 1-19, and "Hardware and Software Development" on page 1-20.</li> <li>Minor text edits.</li> </ul>
October 2011	1.0	Initial release.